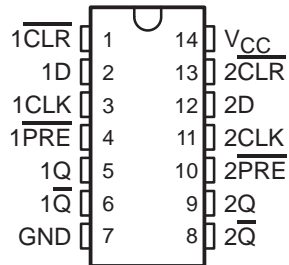


SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

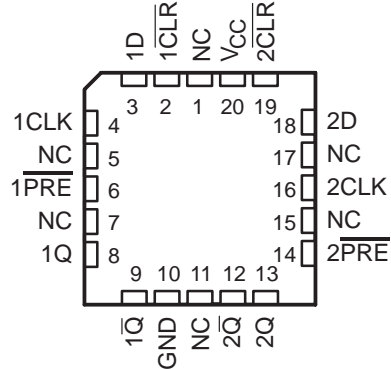
SCAS520H – AUGUST 1995 – REVISED OCTOBER 2003

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 10.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT74 . . . J OR W PACKAGE
SN74ACT74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'ACT74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ACT74N	SN74ACT74N
	SOIC – D	Tube	SN74ACT74D	ACT74
		Tape and reel	SN74ACT74DR	
	SOP – NS	Tape and reel	SN74ACT74NSR	ACT74
	SSOP – DB	Tape and reel	SN74ACT74DBR	AD74
TSSOP – PW	Tube	SN74ACT74PW	AD74	
	Tape and reel	SN74ACT74PWR		
-55°C to 125°C	CDIP – J	Tube	SNJ54ACT74J	SNJ54ACT74J
	CFP – W	Tube	SNJ54ACT74W	SNJ54ACT74W
	LCCC – FK	Tube	SNJ54ACT74FK	SNJ54ACT74FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	SN54ACT74		SN74ACT74		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–24	mA
I_{OL} Low-level output current		24		24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		8		8	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ACT74, SN74ACT74

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54ACT74		SN74ACT74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.49		4.4		4.4	V	
		5.5 V	5.4	5.49		5.4		5.4		
	I _{OH} = -24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I _{OH} = -50 mA†	5.5 V				3.86				
I _{OH} = -75 mA†	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	4.5 V	0.001		0.1		0.1		V	
		5.5 V	0.001		0.1		0.1			
	I _{OL} = 24 mA	4.5 V			0.36		0.5	0.44		
		5.5 V			0.36		0.5	0.44		
	I _{OL} = 50 mA†	5.5 V					1.65			
I _{OL} = 75 mA†	5.5 V						1.65			
I _I	V _I = V _{CC} or GND	5.5 V			±0.1		±1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		40	20	μA	
ΔI _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.6		1.6	1.5	mA	
C _i	V _I = V _{CC} or GND	5 V			3				pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54ACT74		SN74ACT74		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	145		85		125		MHz
t _w	Pulse duration	PRE or CLR low	5	7	6	ns		
		CLK	5	7	6	ns		
t _{su}	Setup time, data before CLK↑	Data	3	4	3.5	ns		
		PRE or CLR inactive	0	0.5	0	ns		
t _h	Hold time, data after CLK↑	1	1	1	ns			

switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT74				UNIT	
			T _A = 25°C			MIN		MAX
			MIN	TYP	MAX			
f _{max}			145	210		85	MHz	
t _{PLH}	PRE or CLR	Q or Q̄	1	5.5	9.5	1	11.5	ns
t _{PHL}			1	6	10	1	12.5	
t _{PLH}	CLK	Q or Q̄	1	7.5	11	1	14	ns
t _{PHL}			1	6	10	1	12	



SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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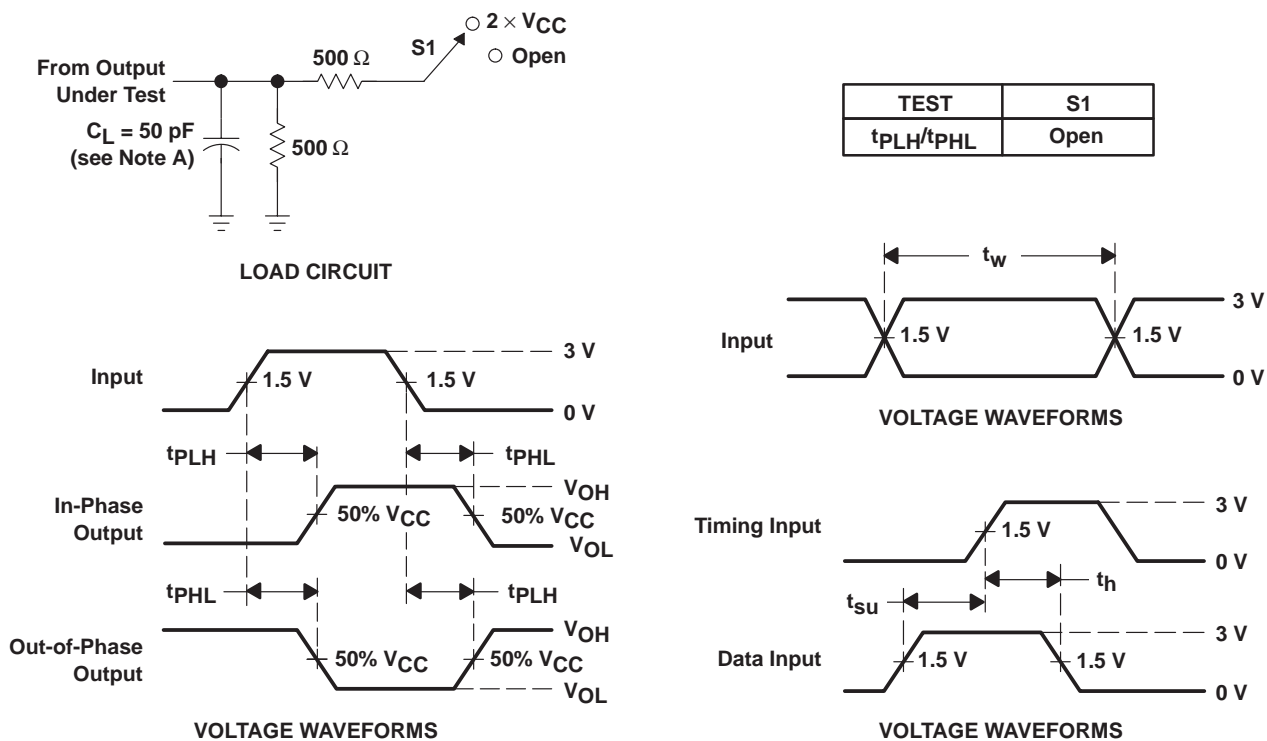
switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ACT74					UNIT
			T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			145	210		125	MHz	
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	5.5	9.5	2.5	10.5	ns
t _{PHL}			3	6	10	3	11.5	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	4	7.5	11	4	13	ns
t _{PHL}			3.5	6	10	3	11.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	45	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

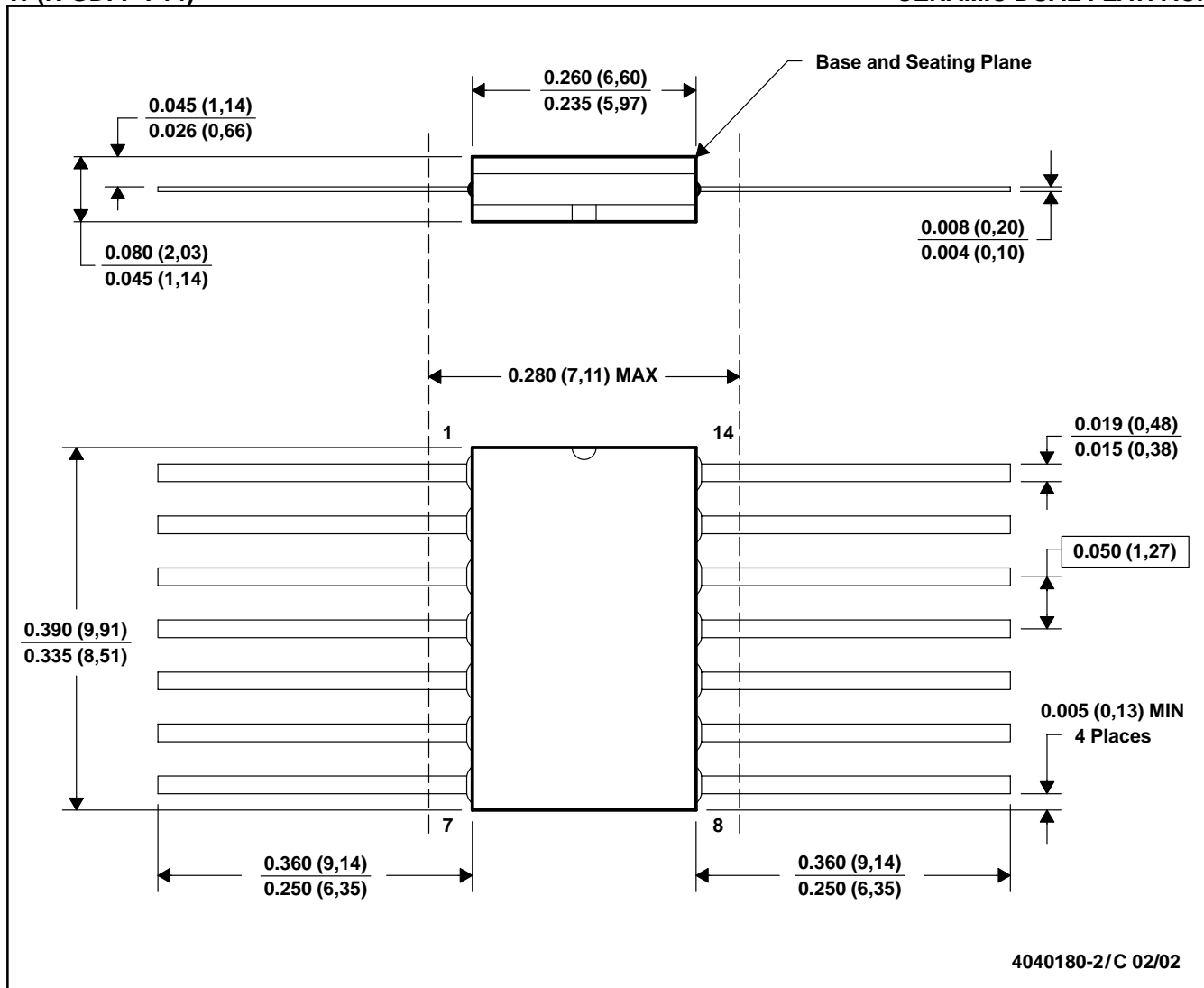


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

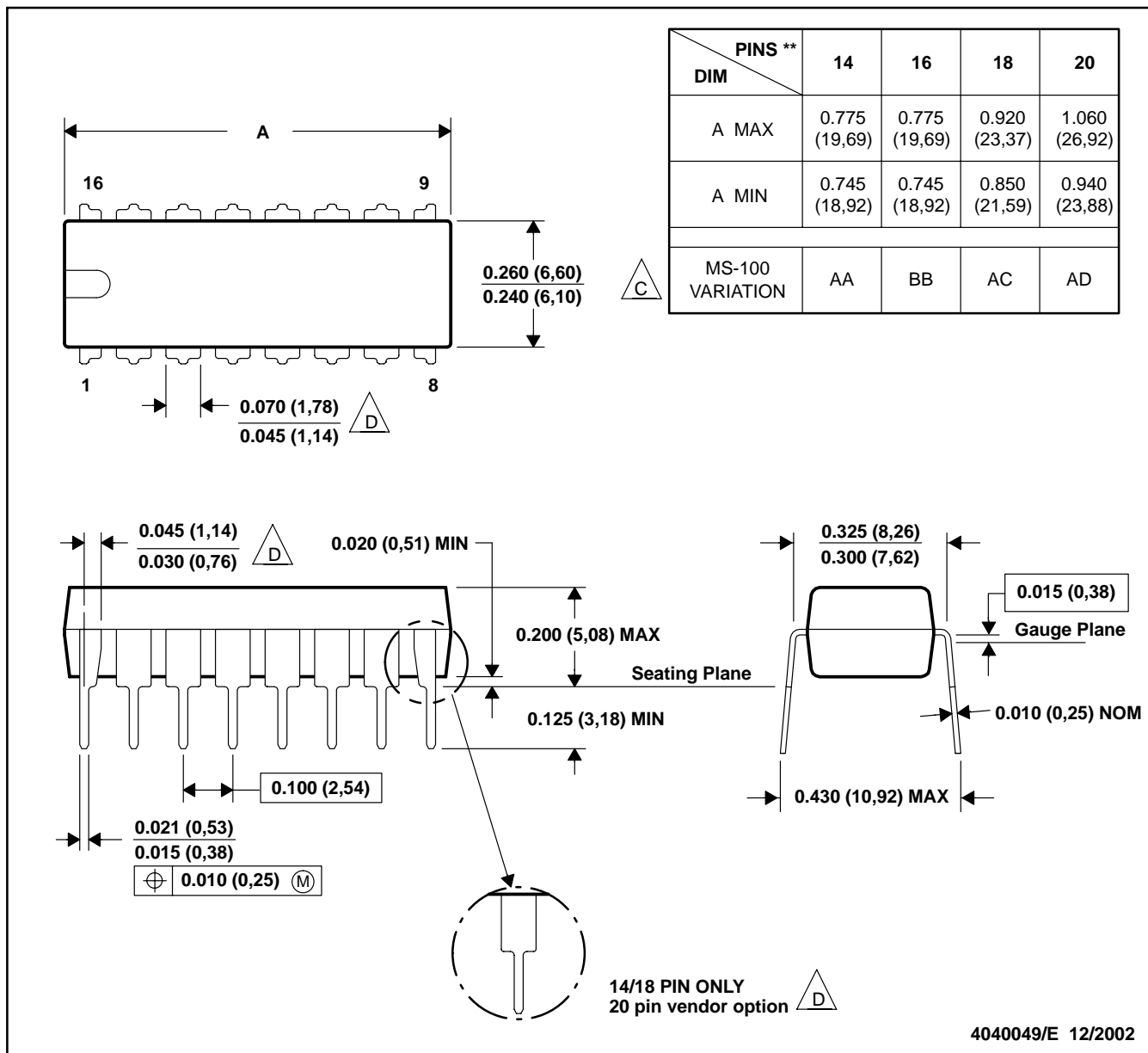


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



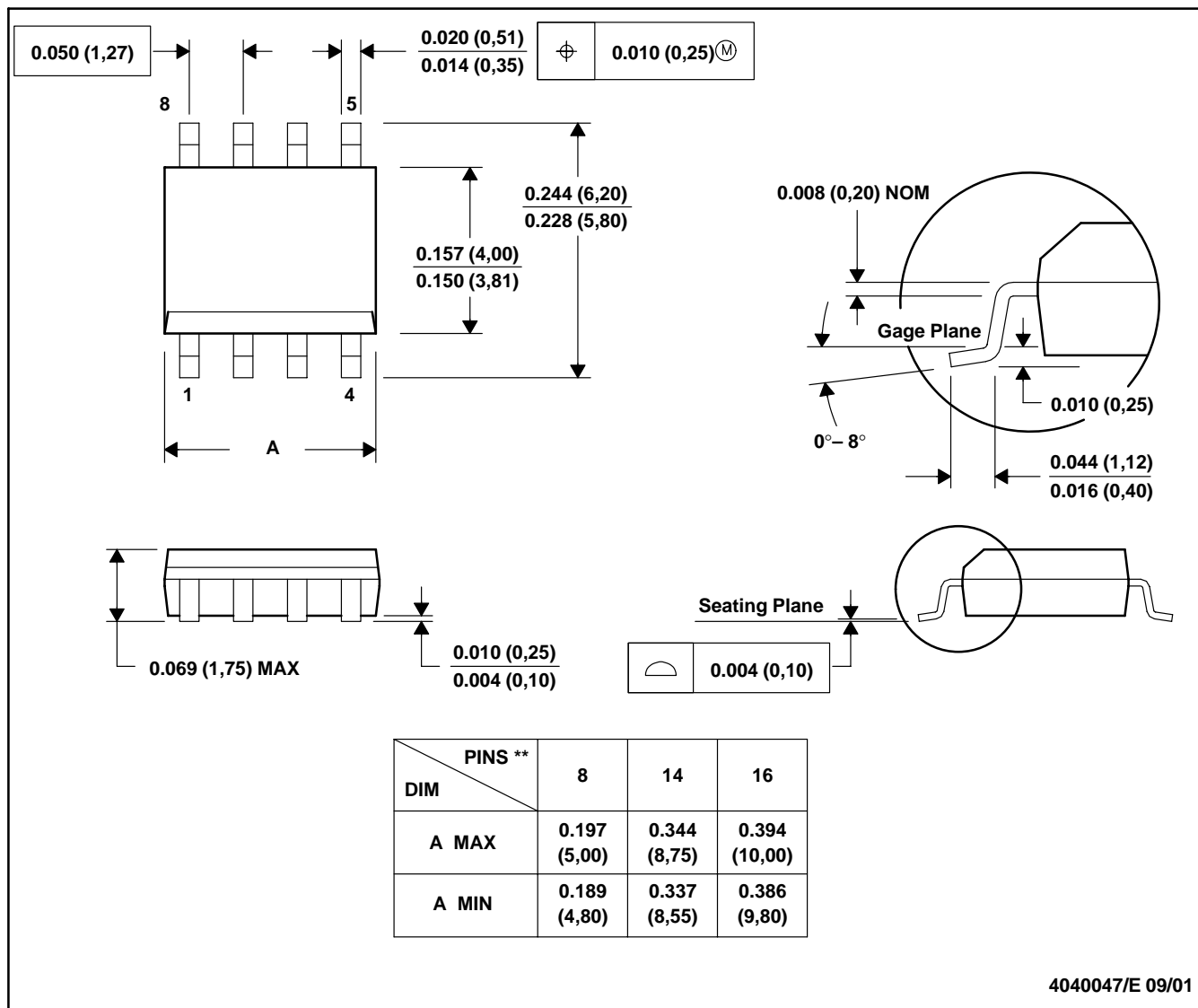
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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