

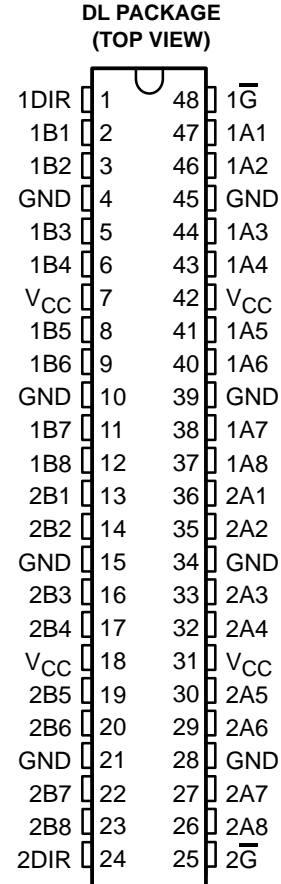
- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Member of the Texas Instruments Widebus™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, highly accelerated stress test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life.

**description**

The SN74ACT16245Q-EP is a 16-bit bus transceiver organized as dual-octal noninverting 3-state transceivers and designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The enable ( $\bar{G}$ ) input can be used to disable the devices so that the buses are effectively isolated.



**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SSOP – DL Tape and reel	SN74ACT16245QDLREP	ACT16245QEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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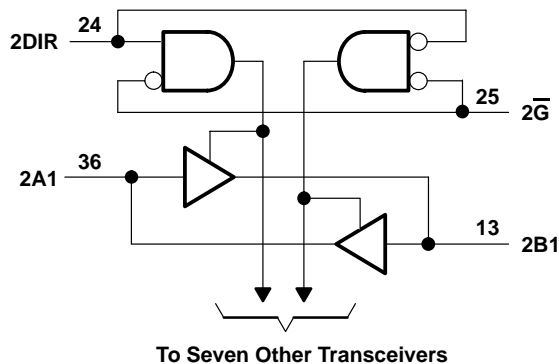
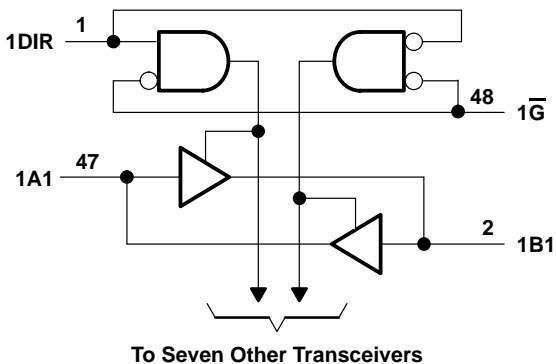
# SN74ACT16245Q-EP 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS677A – MAY 2002 – REVISED JULY 2002

FUNCTION TABLE  
(each section)

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 24$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 24$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 260$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DL package .....	1.2 W
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage (see Note 4)	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-16	mA
I <sub>OL</sub>	Low-level output current		16	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

- NOTES: 3. Unused inputs should be tied to V<sub>CC</sub> through a pullup resistor of approximately 5 kΩ or greater to keep them from floating. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. All V<sub>CC</sub> and GND pins must be connected to the proper-voltage power supply.

**SN74ACT16245Q-EP**  
**16-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

SCAS677A – MAY 2002 – REVISED JULY 2002

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
			MIN	TYP	MAX				
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4			4.4		V	
		5.5 V	5.4			5.4			
	I <sub>OH</sub> = -16 mA	4.5 V	3.94			3.94			
		5.5 V	4.94			4.94			
I <sub>OH</sub> = -24 mA†	5.5 V				3.85				
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V				0.1		V	
		5.5 V				0.1			
	I <sub>OL</sub> = 16 mA	4.5 V				0.36			
		5.5 V				0.36			
I <sub>OL</sub> = 24 mA†	5.5 V				0.5				
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±0.1			±1		μA
I <sub>OZ</sub>	A or B ports‡	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±0.5			±10		μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	8			160		μA
ΔI <sub>CC</sub> §		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V	0.9			1		mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	4.5					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	16					pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current I<sub>I</sub>.

§ This is the increase in supply current for each input that is at one of the specified TTL-voltage levels rather than 0 V or V<sub>CC</sub>.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

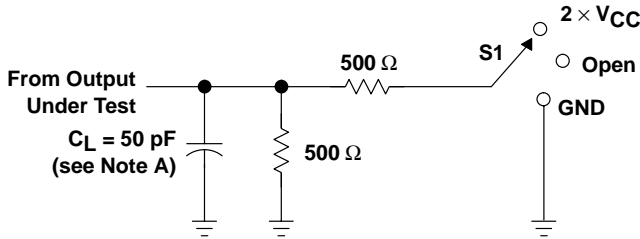
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	3.2	6.9	9.3	3.2	11.5	ns
t <sub>PHL</sub>			2.6	6.4	9.2	2.6	11.1	
t <sub>PZH</sub>	G	B or A	2.7	6.4	9.1	2.7	10.9	ns
t <sub>PZL</sub>			3.4	7.4	10.5	3.4	12.6	
t <sub>PHZ</sub>	G	B or A	5.8	9.2	11.6	5.8	13.4	ns
t <sub>PLZ</sub>			5.5	8.5	10.8	5.5	12.7	

**operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	C <sub>L</sub> = 50 pF, f = 1 MHz	52	pF
			10	

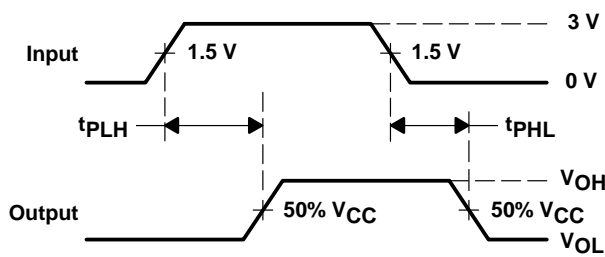


**PARAMETER MEASUREMENT INFORMATION**

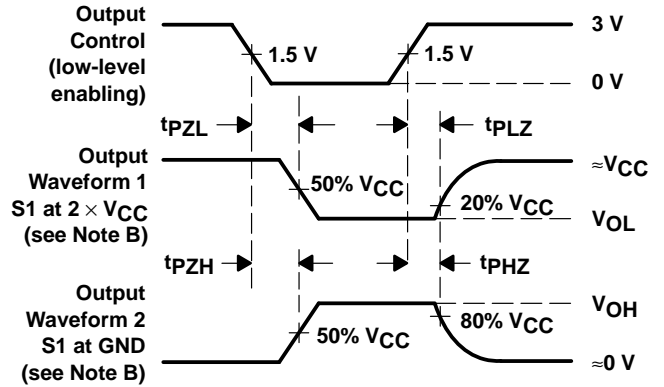


**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



**VOLTAGE WAVEFORMS**



**VOLTAGE WAVEFORMS**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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