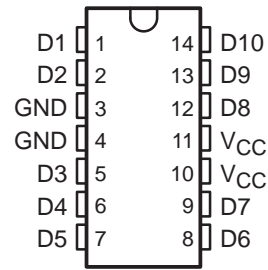


SN74ACT1071 10-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

SCAS192 – D3994, MARCH 1992 – REVISED APRIL 1993

- Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems
- Reduces Undershoot and Overshoot Caused By Line Reflections
- Repetitive Peak Forward Current . . . $I_{FRM} = 100 \text{ mA}$
- Inputs Are TTL-Voltage Compatible
- Low Power Consumption (Like CMOS)
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200 \text{ pF}$, $R = 0$)
- Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise

D PACKAGE
(TOP VIEW)



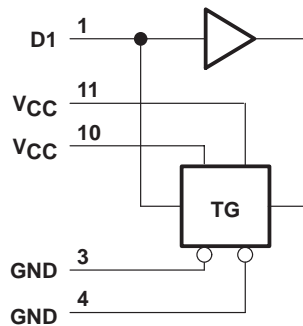
description

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1071 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

The SN74ACT1071 is characterized for operation from -40°C to 85°C .

logic diagram, one of ten channels (positive logic)



SN74ACT1071

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Continuous input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Positive-peak input clamp current, I_{IK} ($V_I > V_{CC}$) ($t_w < 1 \mu s$, duty cycle < 20%)	100 mA
Negative-peak input clamp current, I_{IK} ($V_I < 0$) ($t_w < 1 \mu s$, duty cycle < 20%)	–100 mA
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.5		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
		MIN	TYP†	MAX			
I_{IL}	$V_{CC} = 4.5$ to 5.5 V, $V_I = 0.8$ V	0.15	0.3	0.9	0.1	1	mA
I_{IH}	$V_{CC} = 4.5$ to 5.5 V, $V_I = 2.5$ V	–0.2	–0.5	–1.4	–0.15	–1.5	mA
V_{IKL}	$I_{IN} = -18$ mA			–1.5		–1.5	V
V_{IKH}	$I_{IN} = 18$ mA			$V_{CC}+2$		$V_{CC}+2$	V
I_{CC}^\ddagger	$V_{CC} = 5.5$ V, Inputs open			4		40	μA
ΔI_{CC}^\S	One input at 3.4 V, Other inputs at V_{CC} or GND			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		3				pF

† All typical values are at $V_{CC} = 5$ V.

‡ Inputs may be set high or low prior to the I_{CC} measurement.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

TYPICAL CHARACTERISTICS

FORWARD CURRENT
 vs
 INPUT VOLTAGE
 (UPPER CLAMPING DIODE)

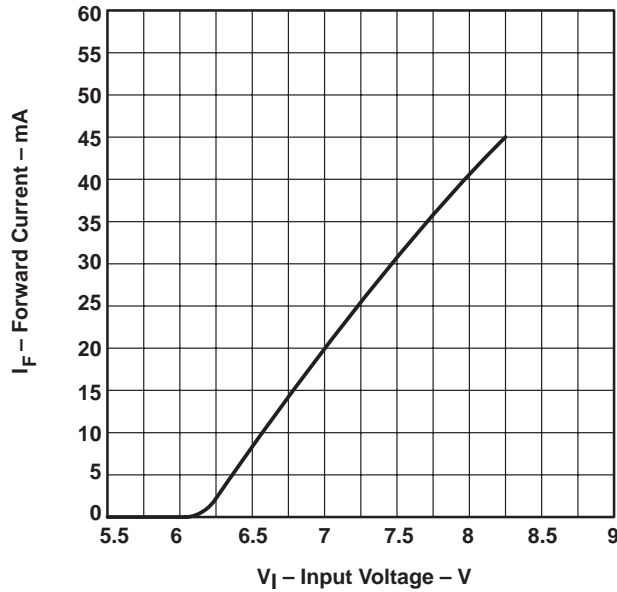


Figure 1

FORWARD CURRENT
 vs
 INPUT VOLTAGE
 (LOWER CLAMPING DIODE)

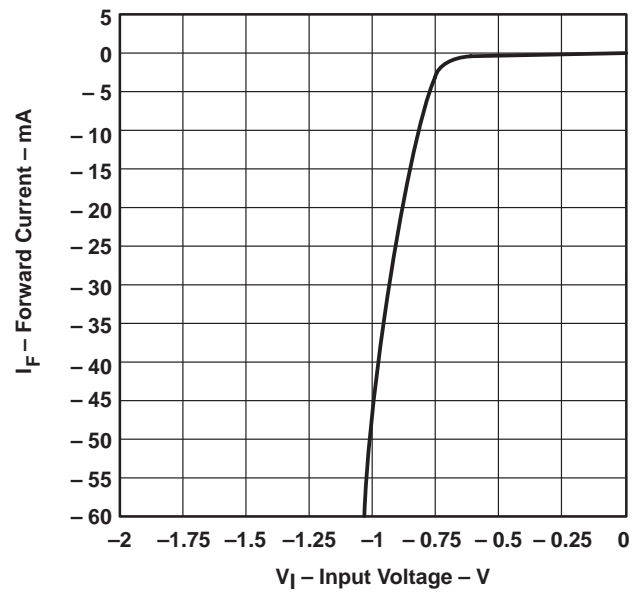


Figure 2

INPUT CURRENT
 vs
 INPUT VOLTAGE

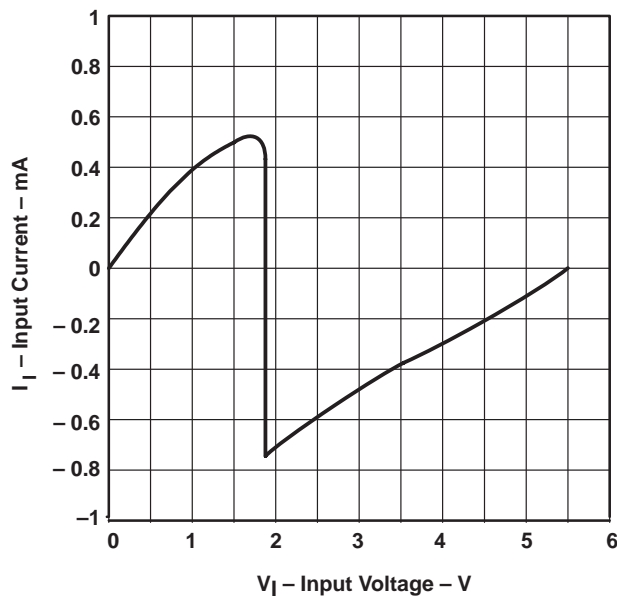


Figure 3

SUPPLY CURRENT
 vs
 INPUT VOLTAGE

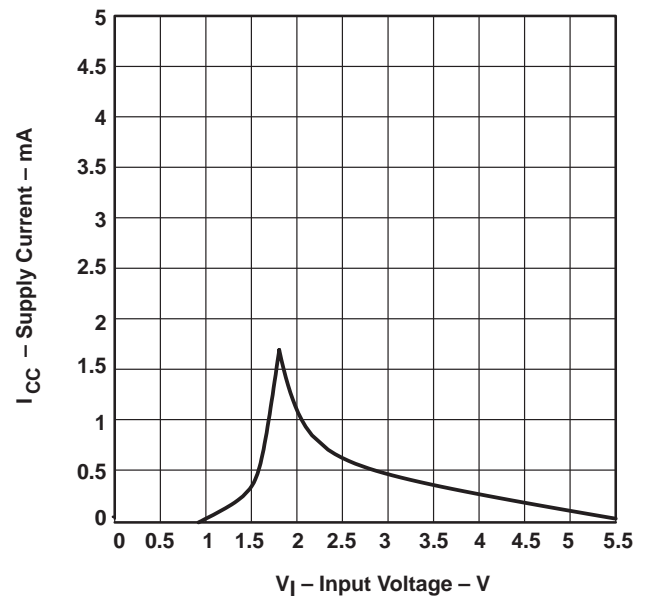


Figure 4

SN74ACT1071 10-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

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APPLICATION INFORMATION

The SN74ACT1071 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

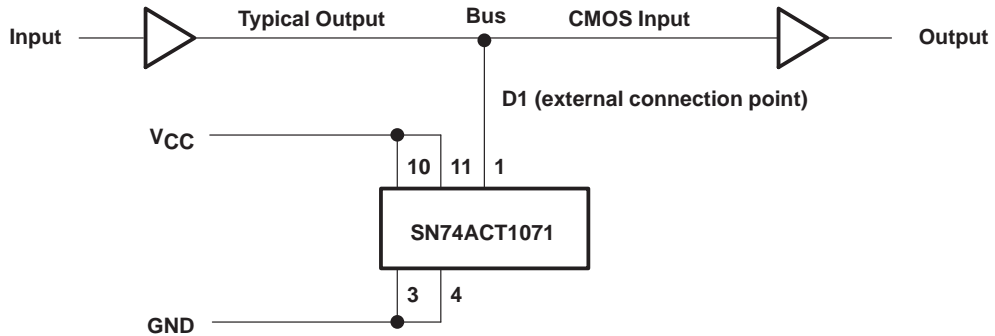


Figure 5. Bus-Hold Application

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ACT1071D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT1071DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT1071DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT1071DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT1071DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT1071DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT1071DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

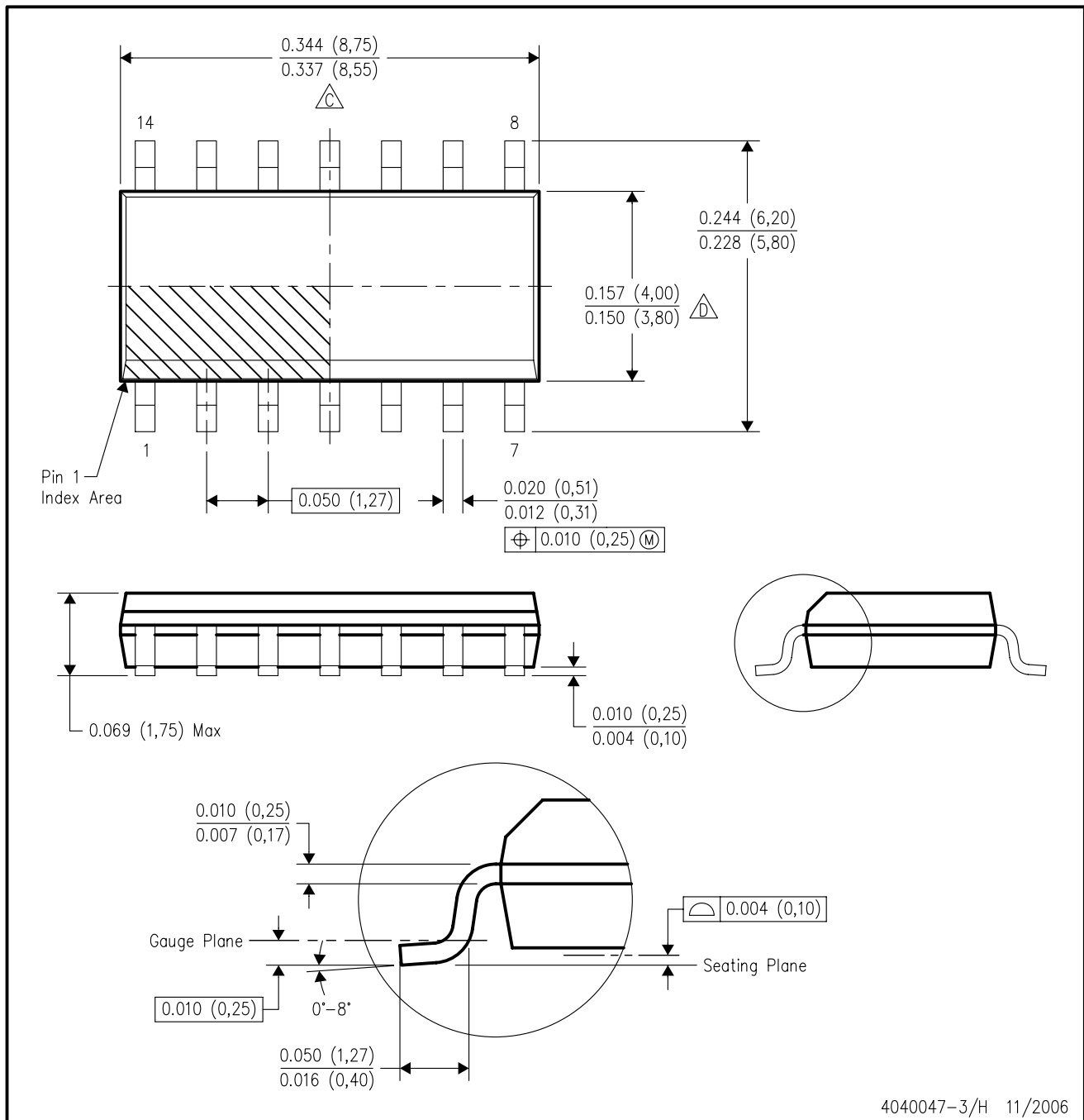


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT1071DR	SOIC	D	14	2500	346.0	346.0	33.0

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.