

# SN54ABT827, SN74ABT827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS159E – JANUARY 1991 – REVISED APRIL 2005

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

## description

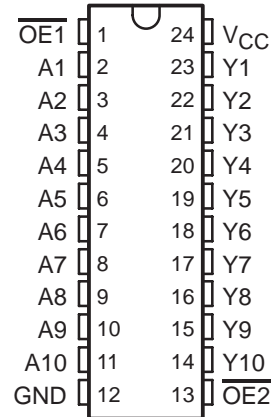
These 10-bit buffers or bus drivers provide a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all ten outputs are in the high-impedance state. The 'ABT827 provides true data at the outputs.

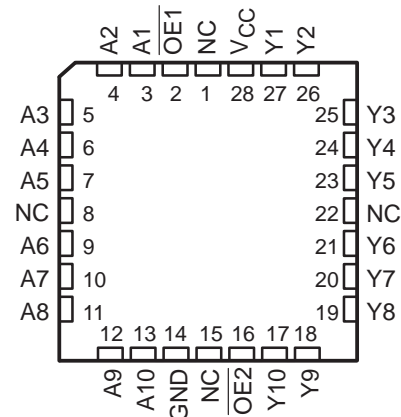
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT827 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT827 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT827 . . . JT PACKAGE  
SN74ABT827 . . . DB, DW, NT, OR PW PACKAGE  
(TOP VIEW)



SN54ABT827 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

| INPUTS           |                  |   | OUTPUT |
|------------------|------------------|---|--------|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y      |
| L                | L                | L | L      |
| L                | L                | H | H      |
| H                | X                | X | Z      |
| X                | H                | X | Z      |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

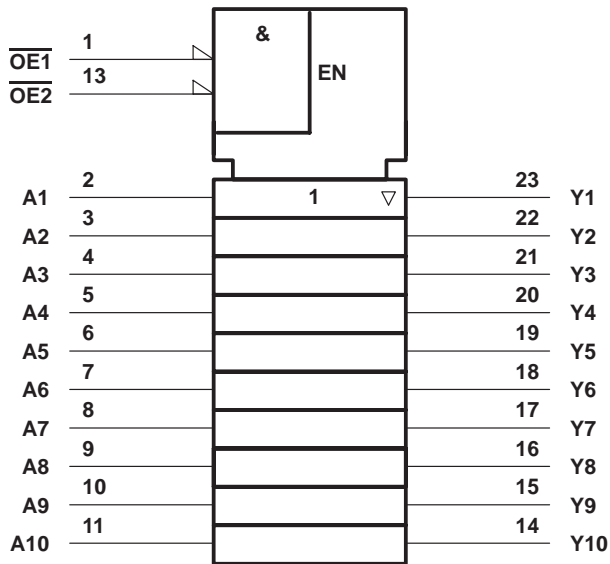
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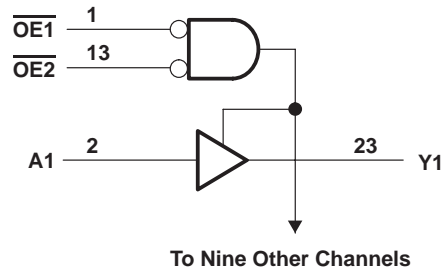
# SN54ABT827, SN74ABT827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$ .....  | -0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1) .....                                   | -0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ ..... | -0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT827 .....              | 96 mA           |
| SN74ABT827 .....  | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....                               | -18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....                              | -50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....         | 104°C/W         |
| DW package .....  | 81°C/W          |
| NT package .....  | 67°C/W          |
| PW package .....  | 120°C/W         |
| Storage temperature range, $T_{stg}$ .....                                      | -65°C to 150°C  |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

# SN54ABT827, SN74ABT827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

|                     |                                    | SN54ABT827 |                 | SN74ABT827 |                 | UNIT |
|---------------------|------------------------------------|------------|-----------------|------------|-----------------|------|
|                     |                                    | MIN        | MAX             | MIN        | MAX             |      |
| V <sub>CC</sub>     | Supply voltage                     | 4.5        | 5.5             | 4.5        | 5.5             | V    |
| V <sub>IH</sub>     | High-level input voltage           | 2          |                 | 2          |                 | V    |
| V <sub>IL</sub>     | Low-level input voltage            |            | 0.8             |            | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      | 0          | V <sub>CC</sub> | 0          | V <sub>CC</sub> | V    |
| I <sub>OH</sub>     | High-level output current          |            | -24             |            | -32             | mA   |
| I <sub>OL</sub>     | Low-level output current           |            | 48              |            | 64              | mA   |
| Δt/Δv               | Input transition rise or fall rate |            | 5               |            | 5               | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 | 200        |                 | 200        |                 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     | -55        | 125             | -40        | 85              | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# SN54ABT827, SN74ABT827 10-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS  | T <sub>A</sub> = 25°C   |      |       | SN54ABT827 |       | SN74ABT827 |       | UNIT |
|---------------------|--|-------------------------|------|-------|------------|-------|------------|-------|------|
|                     |  | MIN                     | TYP† | MAX   | MIN        | MAX   | MIN        | MAX   |      |
| V <sub>IK</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                     |                         |      | -1.2  |            | -1.2  |            | -1.2  | V    |
| V <sub>OH</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                     | 2.5                     |      |       | 2.5        |       | 2.5        |       | V    |
|                     | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                       | 3                       |      |       | 3          |       | 3          |       |      |
|                     | V <sub>CC</sub> = 4.5 V  |                         |      |       |            |       |            | 2     |      |
| V <sub>OL</sub>     | V <sub>CC</sub> = 4.5 V  | I <sub>OL</sub> = 48 mA |      | 0.55  |            | 0.55  |            |       | V    |
|                     |  | I <sub>OL</sub> = 64 mA |      | 0.55* |            |       |            | 0.55  |      |
| V <sub>hys</sub>    |  |                         | 100  |       |            |       |            |       | mV   |
| I <sub>I</sub>      | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                |                         |      | ±1    |            | ±1    |            | ±1    | μA   |
| I <sub>OZPU</sub> ‡ | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                         |      | ±50   |            | ±10   |            | ±50   | μA   |
| I <sub>OZPD</sub> ‡ | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                         |      | ±50   |            | ±10   |            | ±50   | μA   |
| I <sub>OZH</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2 V$   |                         |      | 10§   |            | 10    |            | 10§   | μA   |
| I <sub>OZL</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2 V$   |                         |      | -10§  |            | -10   |            | -10§  | μA   |
| I <sub>off</sub>    | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 5.5 V                        |                         |      | ±100  |            |       |            | ±100  | μA   |
| I <sub>CEX</sub>    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      |                         |      | 50    |            | 50    |            | 50    | μA   |
| I <sub>O</sub> ¶    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      | -50                     | -140 | -225§ | -50        | -225§ | -50        | -225§ | mA   |
| I <sub>CC</sub>     | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | Outputs high            | 80   | 250   |            | 250   |            | 250   | μA   |
|                     |  | Outputs low             | 35   | 40§   |            | 40§   |            | 40§   | mA   |
|                     |  | Outputs disabled        | 80   | 250   |            | 250   |            | 250   | μA   |
| ΔI <sub>CC</sub> #  | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | Outputs enabled         |      | 1.5   |            | 1.5   |            | 1.5   | mA   |
|                     |  | Outputs disabled        |      | 50    |            | 50    |            | 50    | μA   |
|                     |  | Control inputs          |      | 1.5   |            | 1.5   |            | 1.5   | mA   |
| C <sub>i</sub>      | V <sub>I</sub> = 2.5 V or 0.5 V  |                         | 4    |       |            |       |            |       | pF   |
| C <sub>o</sub>      | V <sub>O</sub> = 2.5 V or 0.5 V  |                         | 8    |       |            |       |            |       | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

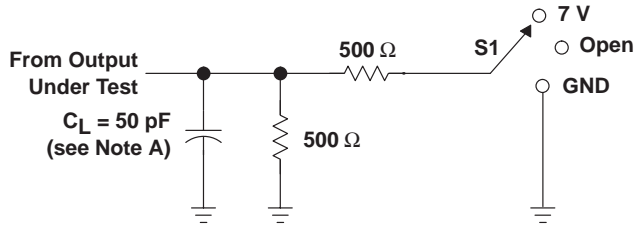
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C |     |     | SN54ABT827 |     | SN74ABT827 |     | UNIT |
|------------------|-----------------|-------------|--|-----|-----|------------|-----|------------|-----|------|
|                  |                 |             | MIN  | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>PLH</sub> | A               | Y           | 1.1  | 2.6 | 4.4 | 1.1        | 4.9 | 1.1        | 4.8 | ns   |
| t <sub>PHL</sub> |                 |             | 1.1  | 2.3 | 4.1 | 1.1        | 4.8 | 1.1        | 4.7 |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Y           | 1§   | 3.2 | 5.1 | 1          | 6   | 1§         | 5.9 | ns   |
| t <sub>PZL</sub> |                 |             | 1§   | 3.3 | 5.9 | 1          | 7.1 | 1§         | 6.9 |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Y           | 2  | 4.9 | 6.3 | 2          | 7   | 2          | 6.8 | ns   |
| t <sub>PLZ</sub> |                 |             | 1.3§   | 4.2 | 6.6 | 1.3        | 7.9 | 1.3§       | 6.9 |      |

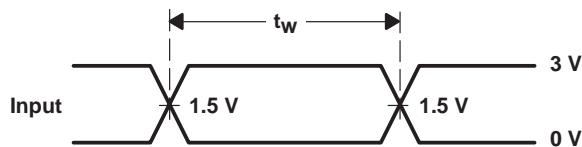
§ This data sheet limit may vary among suppliers.



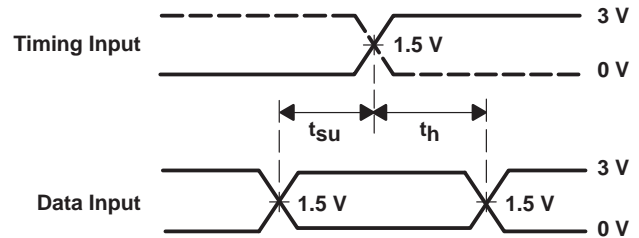
PARAMETER MEASUREMENT INFORMATION



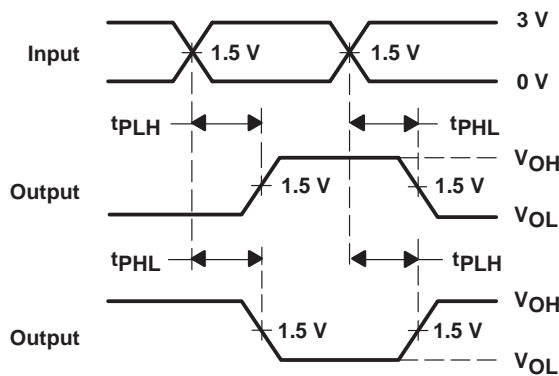
LOAD CIRCUIT



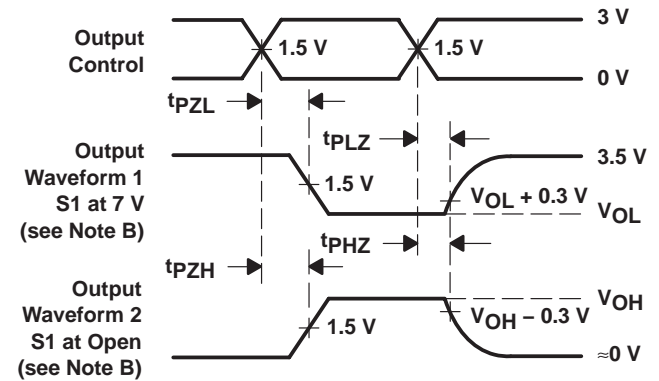
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--|-------------------------|
| 5962-9450901Q3A  | ACTIVE        | LCCC         | FK                 | 28   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9450901Q3A<br>SNJ54<br>ABT827FK | <a href="#">Samples</a> |
| 5962-9450901QKA  | ACTIVE        | CFP          | W                  | 24   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9450901QK<br>A<br>SNJ54ABT827W      | <a href="#">Samples</a> |
| 5962-9450901QLA  | ACTIVE        | CDIP         | JT                 | 24   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9450901QL<br>A<br>SNJ54ABT827JT     | <a href="#">Samples</a> |
| SN74ABT827DBLE   | OBSOLETE      | SSOP         | DB                 | 24   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |  |                         |
| SN74ABT827DBR    | ACTIVE        | SSOP         | DB                 | 24   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB827                                    | <a href="#">Samples</a> |
| SN74ABT827DW     | ACTIVE        | SOIC         | DW                 | 24   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT827                                   | <a href="#">Samples</a> |
| SN74ABT827DWR    | ACTIVE        | SOIC         | DW                 | 24   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | ABT827                                   | <a href="#">Samples</a> |
| SN74ABT827NT     | ACTIVE        | PDIP         | NT                 | 24   | 15             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | SN74ABT827NT                             | <a href="#">Samples</a> |
| SN74ABT827NTE4   | ACTIVE        | PDIP         | NT                 | 24   | 15             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | SN74ABT827NT                             | <a href="#">Samples</a> |
| SN74ABT827PW     | ACTIVE        | TSSOP        | PW                 | 24   | 60             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB827                                    | <a href="#">Samples</a> |
| SN74ABT827PWG4   | ACTIVE        | TSSOP        | PW                 | 24   | 60             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB827                                    | <a href="#">Samples</a> |
| SN74ABT827PWLE   | OBSOLETE      | TSSOP        | PW                 | 24   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |  |                         |
| SN74ABT827PWR    | ACTIVE        | TSSOP        | PW                 | 24   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | AB827                                    | <a href="#">Samples</a> |
| SNJ54ABT827FK    | ACTIVE        | LCCC         | FK                 | 28   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9450901Q3A<br>SNJ54<br>ABT827FK | <a href="#">Samples</a> |
| SNJ54ABT827JT    | ACTIVE        | CDIP         | JT                 | 24   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9450901QL<br>A<br>SNJ54ABT827JT     | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)             | Samples        |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------------------|----------------|
| SNJ54ABT827W     | ACTIVE        | CFP          | W               | 24   | 1           | TBD             | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9450901QK<br>A<br>SNJ54ABT827W | <b>Samples</b> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABT827, SN74ABT827 :**

- Catalog: [SN74ABT827](#)
- Military: [SN54ABT827](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT827DBR | SSOP         | DB              | 24   | 2000 | 330.0              | 16.4               | 8.2     | 8.8     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT827DWR | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ABT827PWR | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

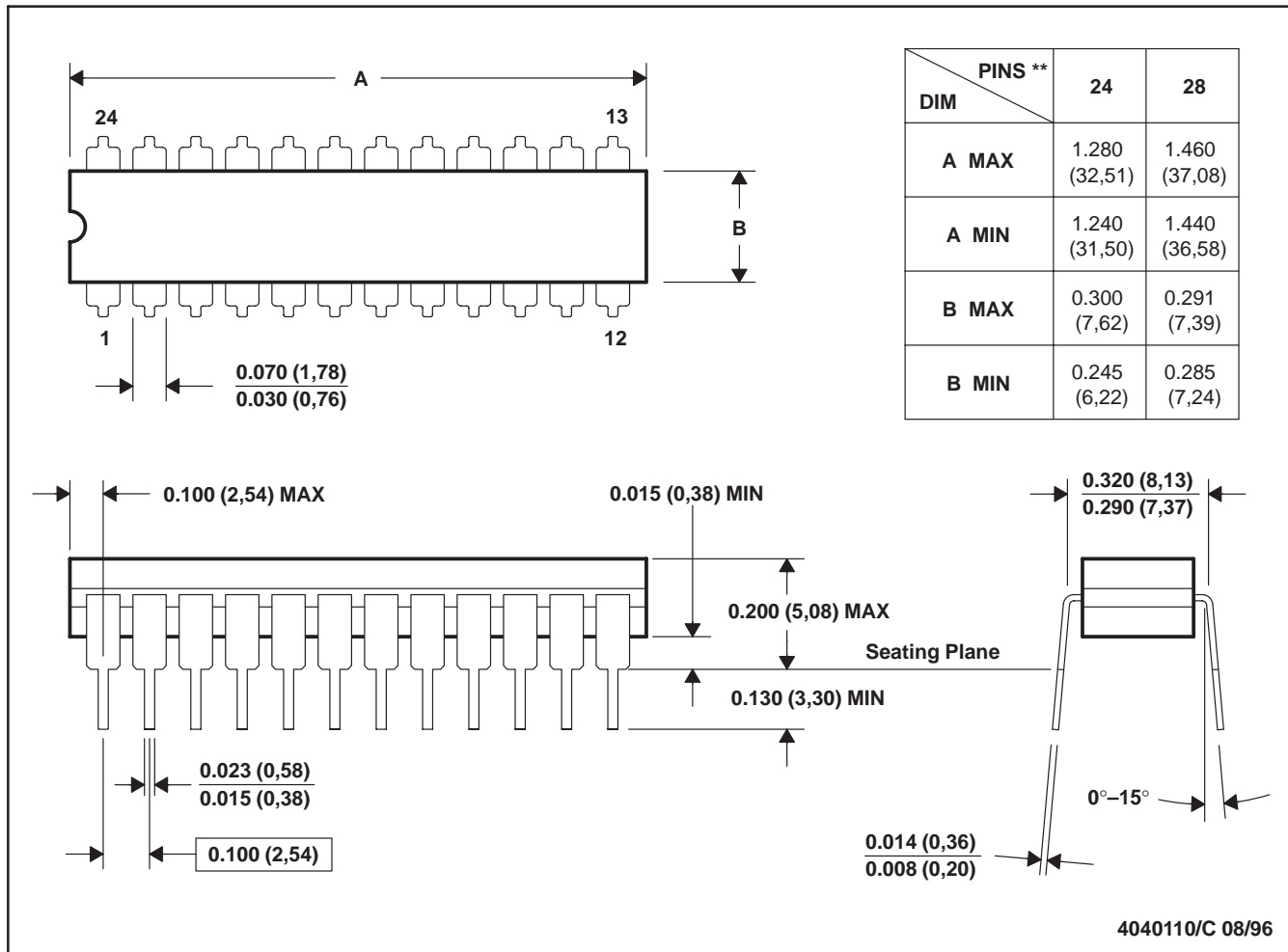

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT827DBR | SSOP         | DB              | 24   | 2000 | 367.0       | 367.0      | 38.0        |
| SN74ABT827DWR | SOIC         | DW              | 24   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74ABT827PWR | TSSOP        | PW              | 24   | 2000 | 367.0       | 367.0      | 38.0        |

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

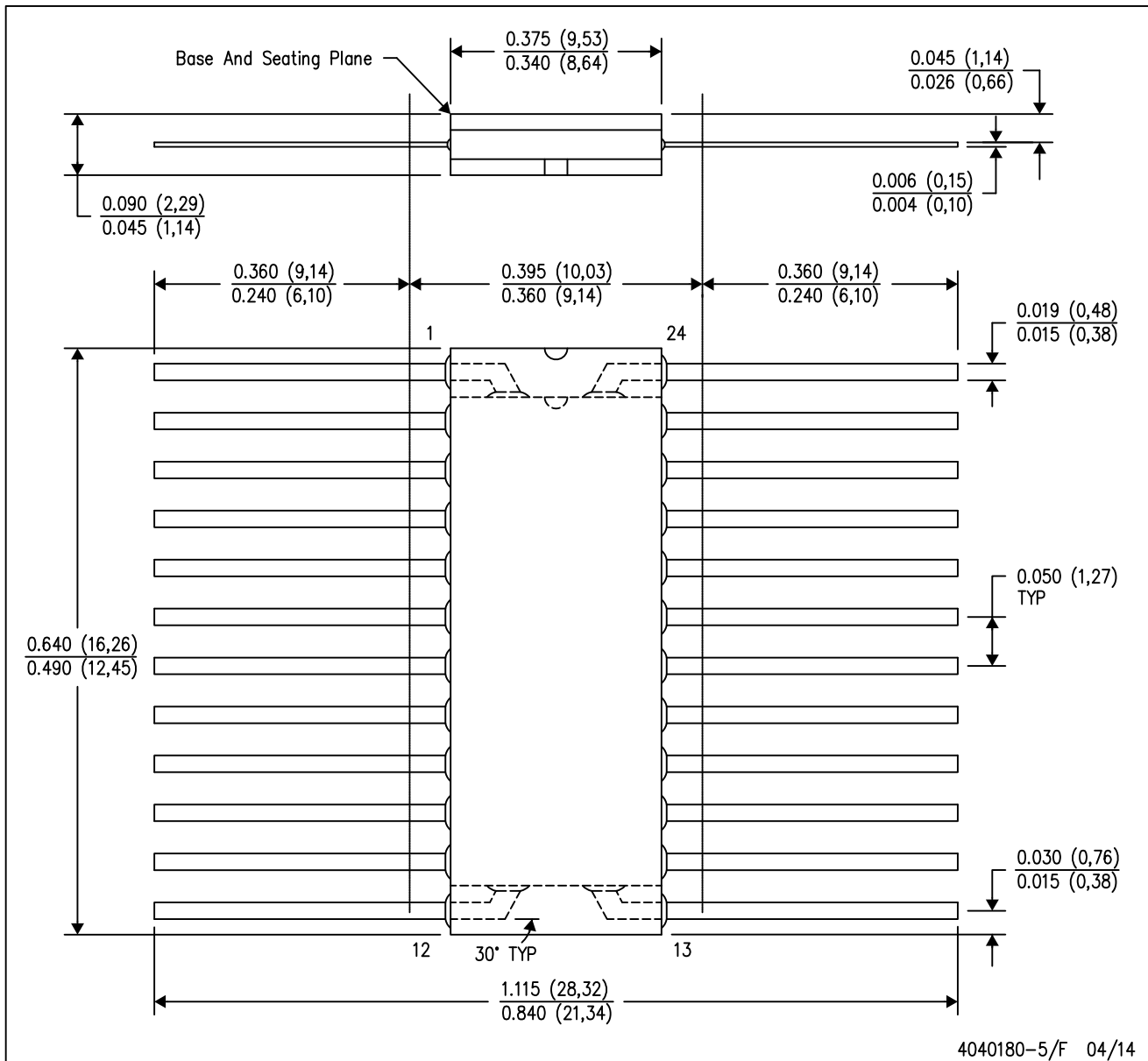
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

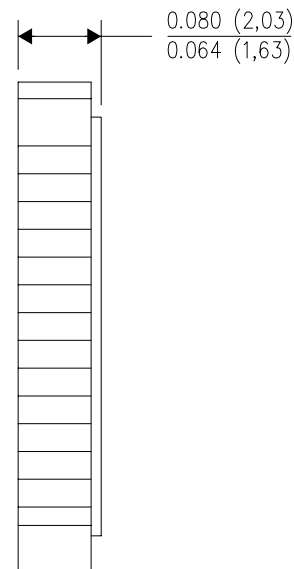
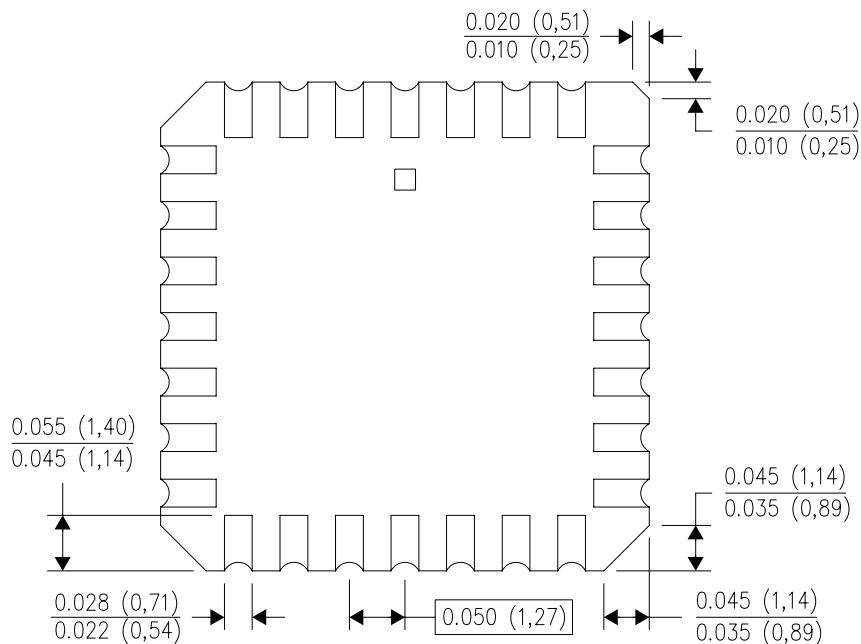
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



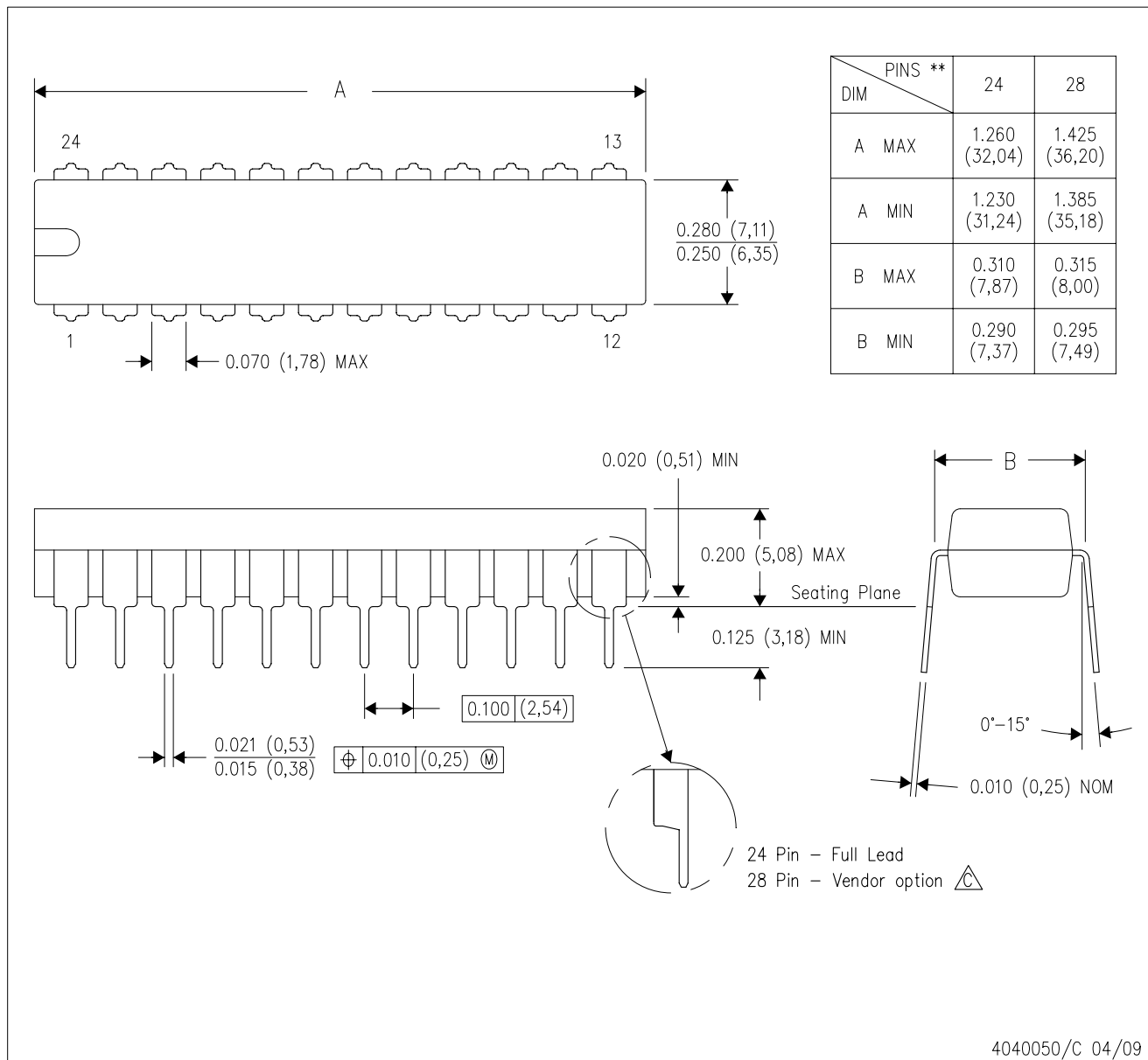
4040140/D 01/11


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

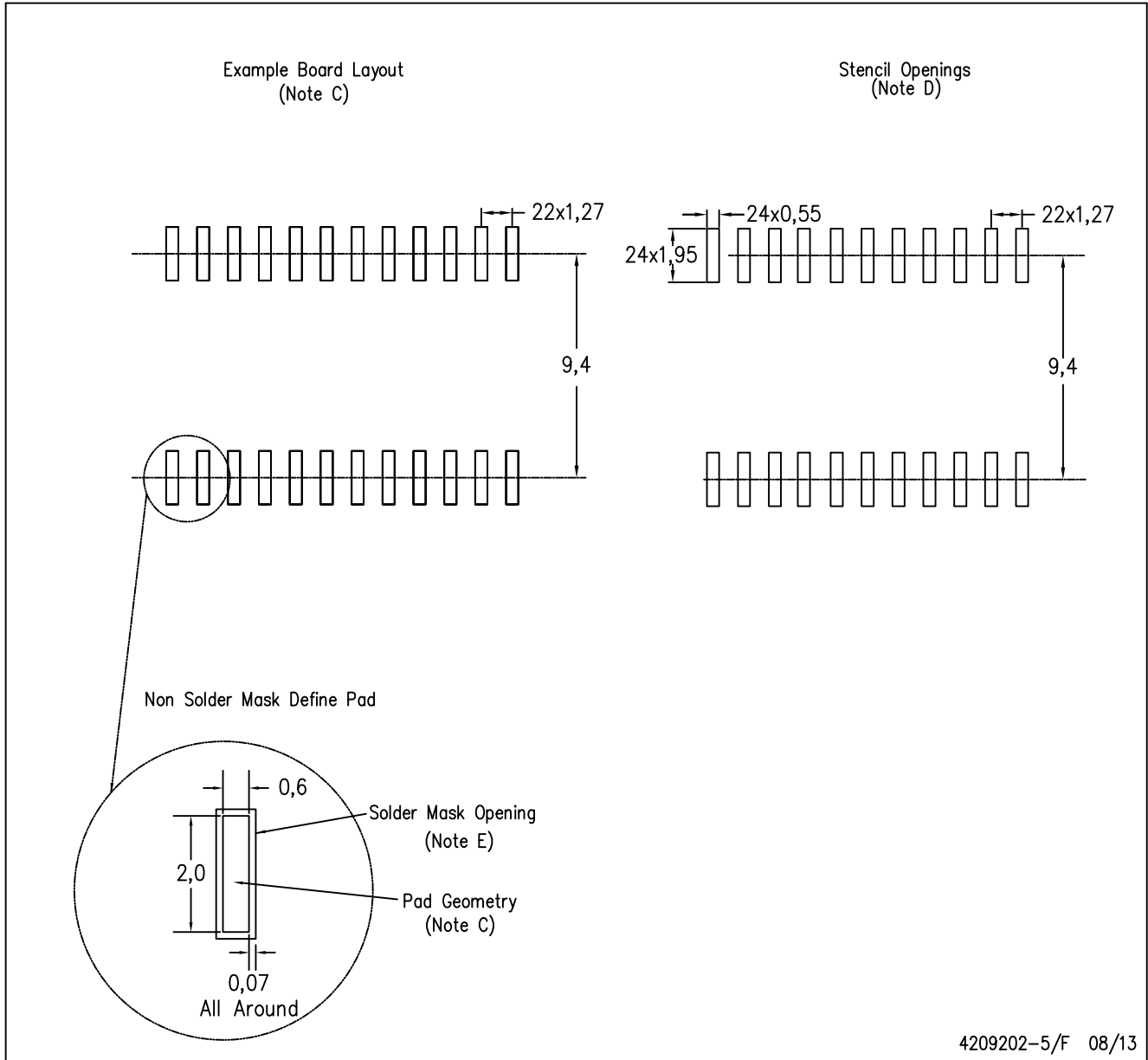
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

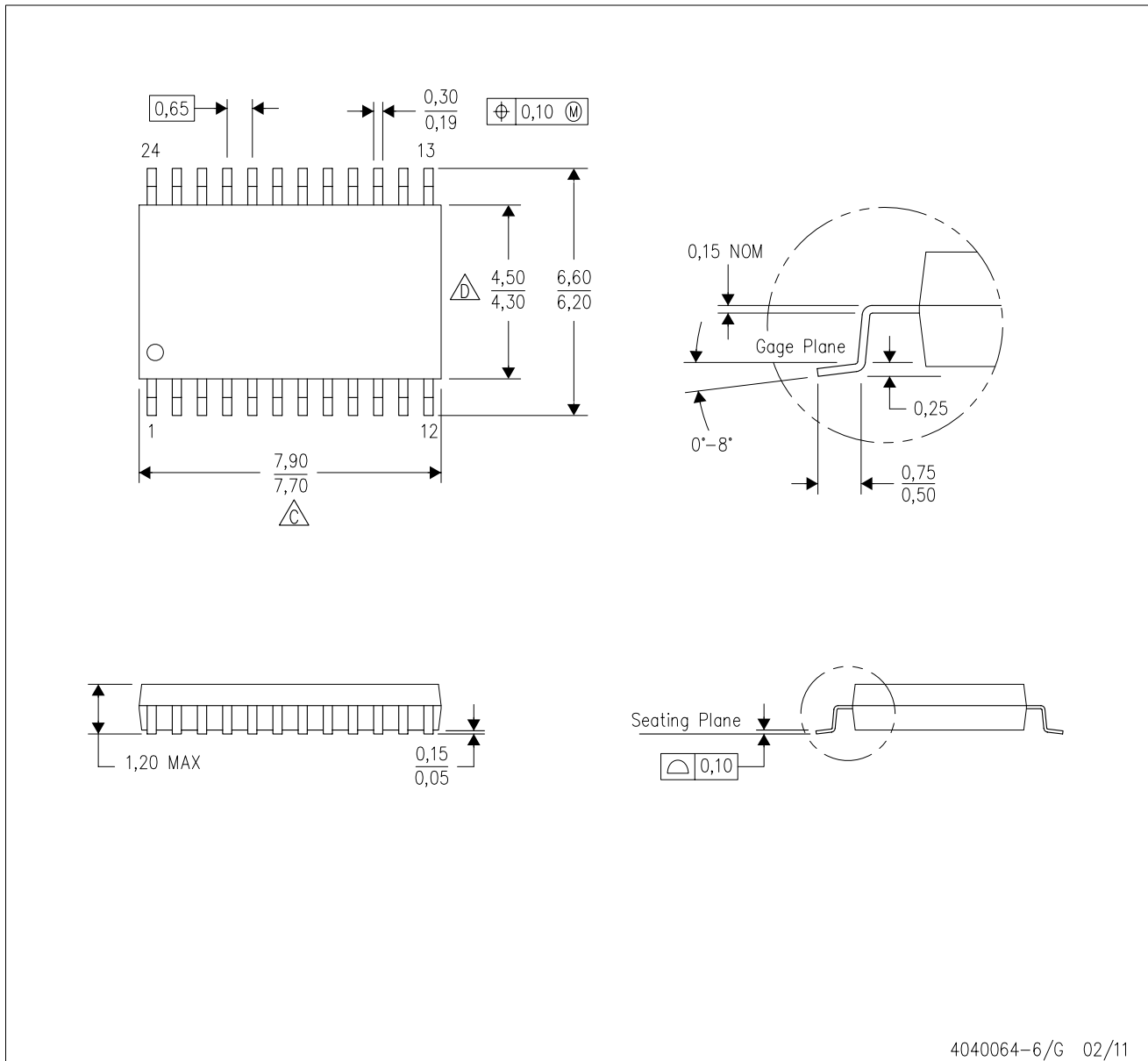
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

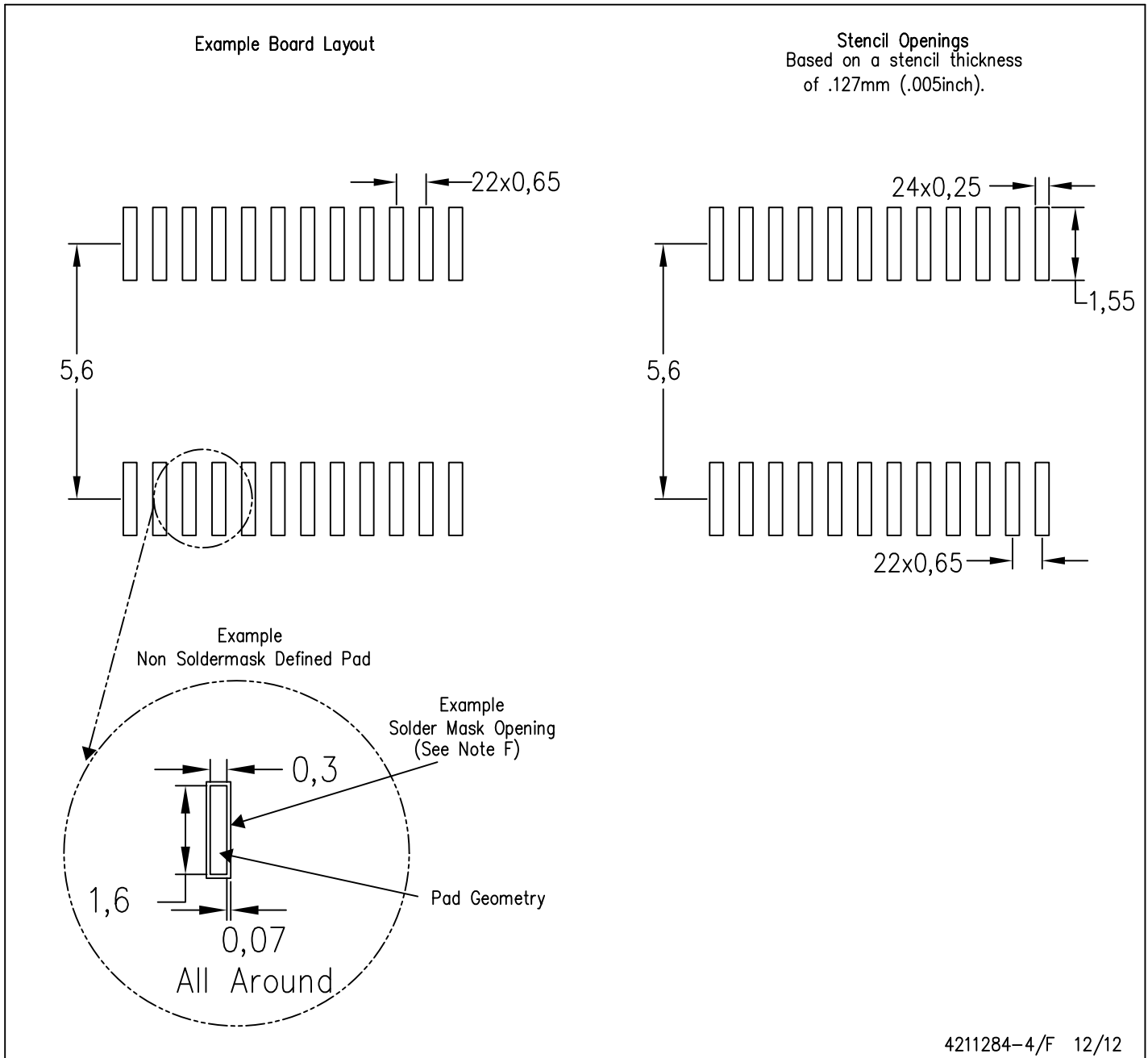


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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|                               |  |
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