

SN54ABT823, SN74ABT823 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS158E – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (NT) and Ceramic (JT) DIPs

description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

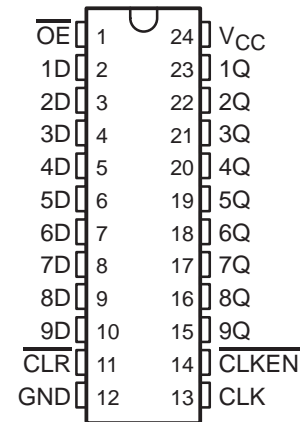
With the clock-enable ($\overline{\text{CLKEN}}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the nine Q outputs to go low, independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

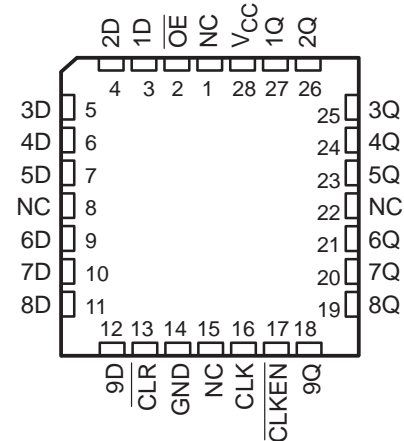
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT823 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT823 is characterized for operation from -40°C to 85°C .

SN54ABT823 . . . JT OR W PACKAGE
SN74ABT823 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT823 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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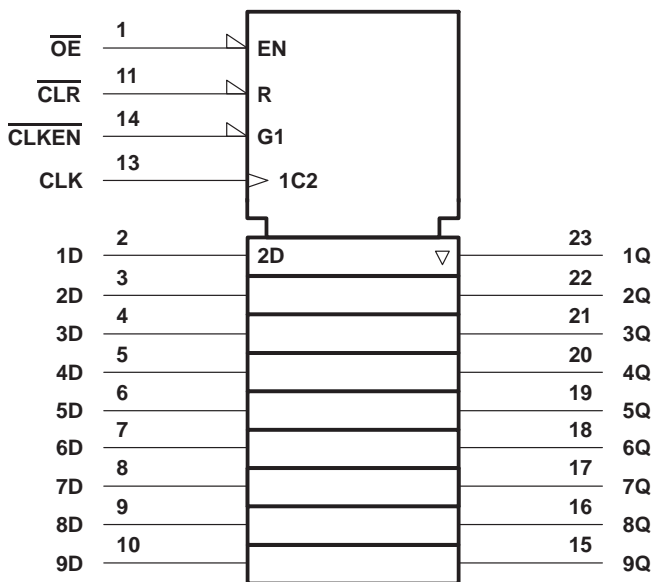
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FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | | OUTPUT |
|-----------------|------------------|--------------------|-----|---|----------------|
| \overline{OE} | \overline{CLR} | \overline{CLKEN} | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | Q ₀ |
| H | X | X | X | X | Z |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, and W packages.

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recommended operating conditions (see Note 3)

| | | SN54ABT823 | | SN74ABT823 | | UNIT |
|---------------------|------------------------------------|------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -24 | | -32 | mA |
| I _{OL} | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | | 5 | | 5 | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = 25°C | | | SN54ABT823 | | SN74ABT823 | | UNIT |
|---------------------|--|-----------------------|------|-------|------------|------|------------|------|------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | -1.2 | | -1.2 | V |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | V _{CC} = 5 V, I _{OH} = -3 mA | 3 | | | 3 | | 3 | | |
| | V _{CC} = 4.5 V, I _{OH} = -24 mA | 2 | | | 2 | | | 2 | |
| V _{OL} | V _{CC} = 4.5 V, I _{OL} = 48 mA | | | 0.55 | | 0.55 | | | V |
| | | | | 0.55* | | | 0.55 | | |
| V _{hys} | | | 100 | | | | | | mV |
| I _I | V _{CC} = 5.5 V, V _I = V _{CC} or GND | | | ±1 | | ±1 | | ±1 | μA |
| I _{OZPU} ‡ | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | ±50 | | ±50 | μA |
| I _{OZPD} ‡ | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | | | ±50 | | ±50 | | ±50 | μA |
| I _{OZH} | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V | | | 10§ | | 10§ | | 10§ | μA |
| I _{OZL} | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V | | | -10§ | | -10§ | | -10§ | μA |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | ±100 | | | | ±100 | μA |
| I _{CEX} | V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high | | | 50 | | 50 | | 50 | μA |
| I _O ¶ | V _{CC} = 5.5 V, V _O = 2.5 V | -50 | -140 | -180 | -50 | -180 | -50 | -180 | mA |
| I _{CC} | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | 1 | 250 | 250 | 250 | 250 | μA | |
| | | Outputs low | 24 | 38 | 38 | 38 | 38 | mA | |
| | | Outputs disabled | 0.5 | 250 | 250 | 250 | 250 | μA | |
| ΔI _{CC} # | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | | | 1.5 | | 1.5 | | 1.5 | mA |
| C _i | V _I = 2.5 V or 0.5 V | | | 4 | | | | | pF |
| C _o | V _O = 2.5 V or 0.5 V | | | 7 | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | $V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$ | | SN54ABT823 | | SN74ABT823 | | UNIT |
|--------------------|----------------------------------|--|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 0 | 125 | 0 | 125 | 0 | 125 | MHz |
| t_w | Pulse duration | CLR low | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | ns |
| | | CLK high | 2.9 | 2.9 | 2.9 | 2.9 | | |
| | | CLK low | 3.8 | 3.8 | 3.8 | 3.8 | | |
| t_{su} | Setup time before CLK \uparrow | CLR inactive | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | ns |
| | | Data | 2.1 | 2.1 | 2.1 | 2.1 | | |
| | | CLKEN high | 2 | 2 | 2 | 2 | | |
| | | CLKEN low | 3.3 | 3.3 | 3.3 | 3.3 | | |
| t_h | Hold time after CLK \uparrow | Data | 1.3 | 1.3 | 1.3 | 1.3 | ns | |
| | | CLKEN high | 1 | 1 | 1 | 1 | | |
| | | CLKEN low | 2 | 2 | 2 | 2 | | |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

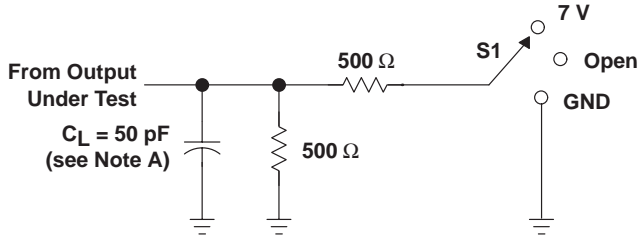
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$ | | | SN54ABT823 | | SN74ABT823 | | UNIT |
|------------------|-------------------------|-------------|--|-----|---------------|------------|-----|------------|---------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 125 | 200 | | 125 | | 125 | | MHz |
| t_{PLH} | CLK | Q | 2.1 | 4.3 | 5.9 | 2.1 | 8.1 | 2.1 | 6.8 | ns |
| t_{PHL} | | | 2.2 | 4.4 | 6.1 | 2.2 | 7 | 2.2 | 6.7 | |
| t_{PHL} | $\overline{\text{CLR}}$ | Q | 2 | 4.1 | 6.3 | 2 | 7.3 | 2 | 7.1 | ns |
| t_{PZH} | $\overline{\text{OE}}$ | Q | 1 | 3 | 4.7 \dagger | 1 | 6.3 | 1 | 6 \dagger | ns |
| t_{PZL} | | | 2.2 | 4.1 | 5.6 | 2.2 | 6.6 | 2.2 | 6.5 \dagger | |
| t_{PHZ} | $\overline{\text{OE}}$ | Q | 2.7 | 4.8 | 6.5 \dagger | 2.7 | 7.7 | 2.7 | 7.5 \dagger | ns |
| t_{PLZ} | | | 1.9 | 5 | 6.4 | 1.9 | 7.4 | 1.9 | 6.9 | |

\dagger This data sheet limit may vary among suppliers.

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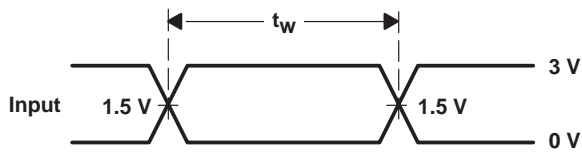
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PARAMETER MEASUREMENT INFORMATION

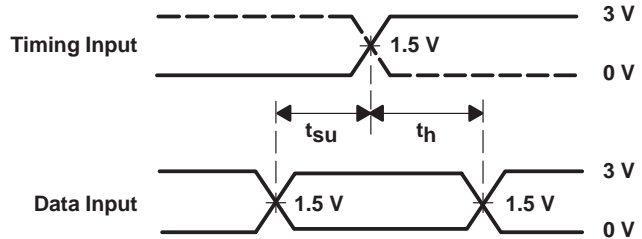


LOAD CIRCUIT

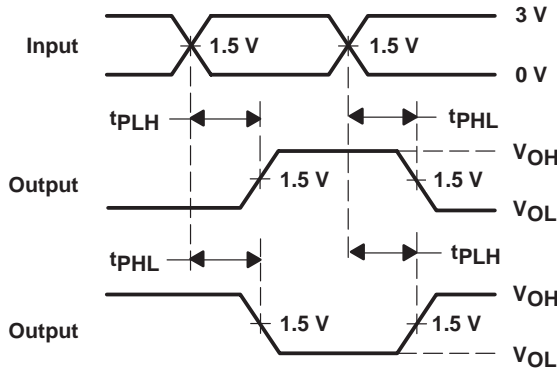
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



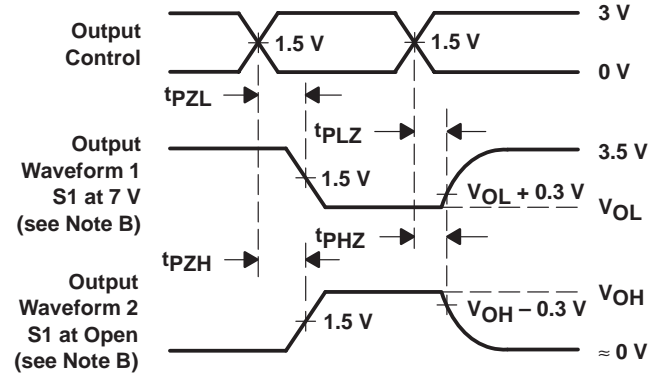
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9450801Q3A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9450801QKA | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9450801QLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74ABT823DBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI |
| SN74ABT823DBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPD | Level-1-260C-UNLIM |
| SN74ABT823DBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPD | Level-1-260C-UNLIM |
| SN74ABT823DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823NSR | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823NSRE4 | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823NSRG4 | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT823NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT823NTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SNJ54ABT823FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ABT823JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54ABT823W | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT823DBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT823DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ABT823NSR | SO | NS | 24 | 2000 | 330.0 | 24.4 | 8.2 | 15.4 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT823DBR | SSOP | DB | 24 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74ABT823DWR | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT823NSR | SO | NS | 24 | 2000 | 346.0 | 346.0 | 41.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

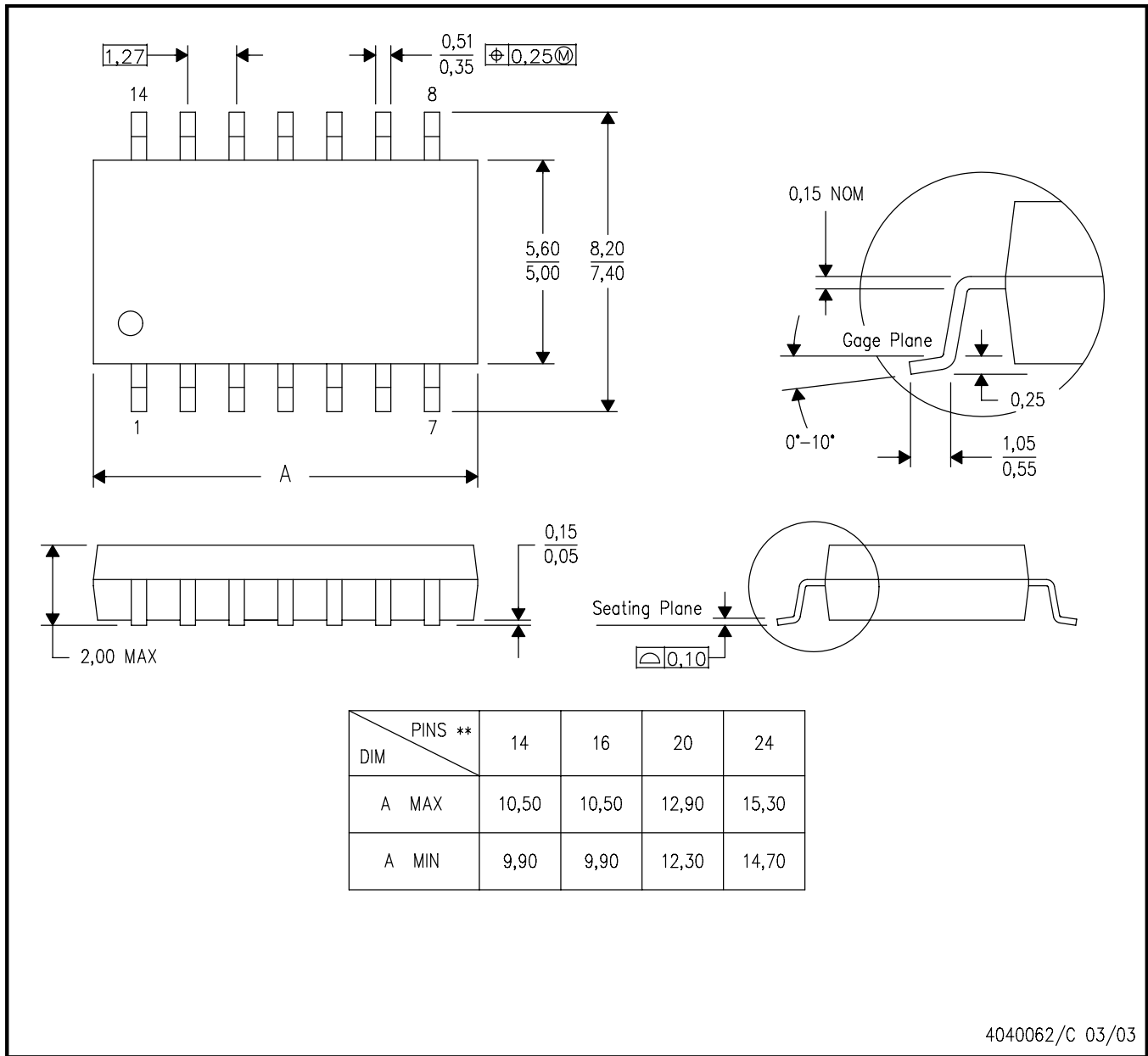
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MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

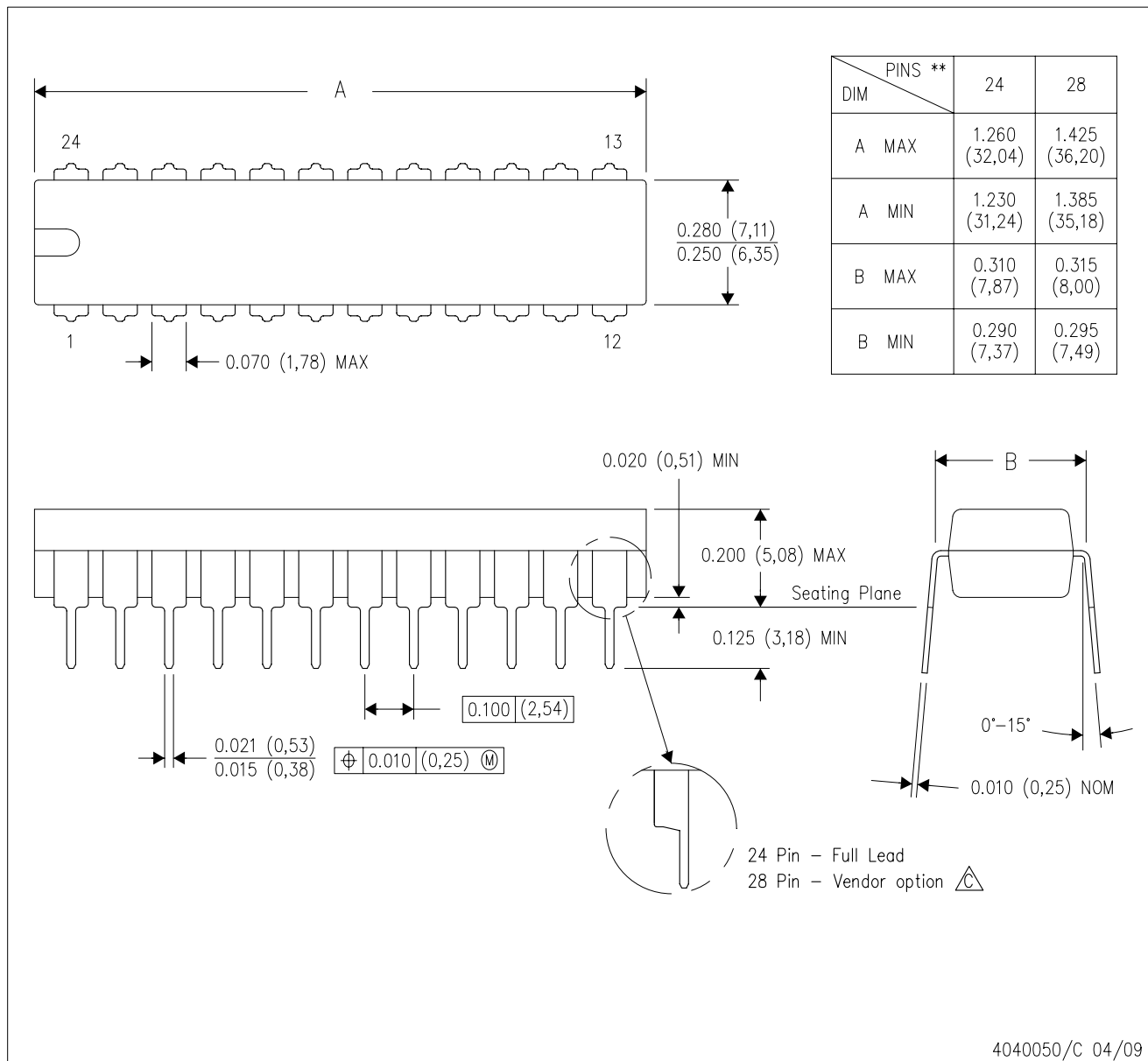
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

MECHANICAL DATA


NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



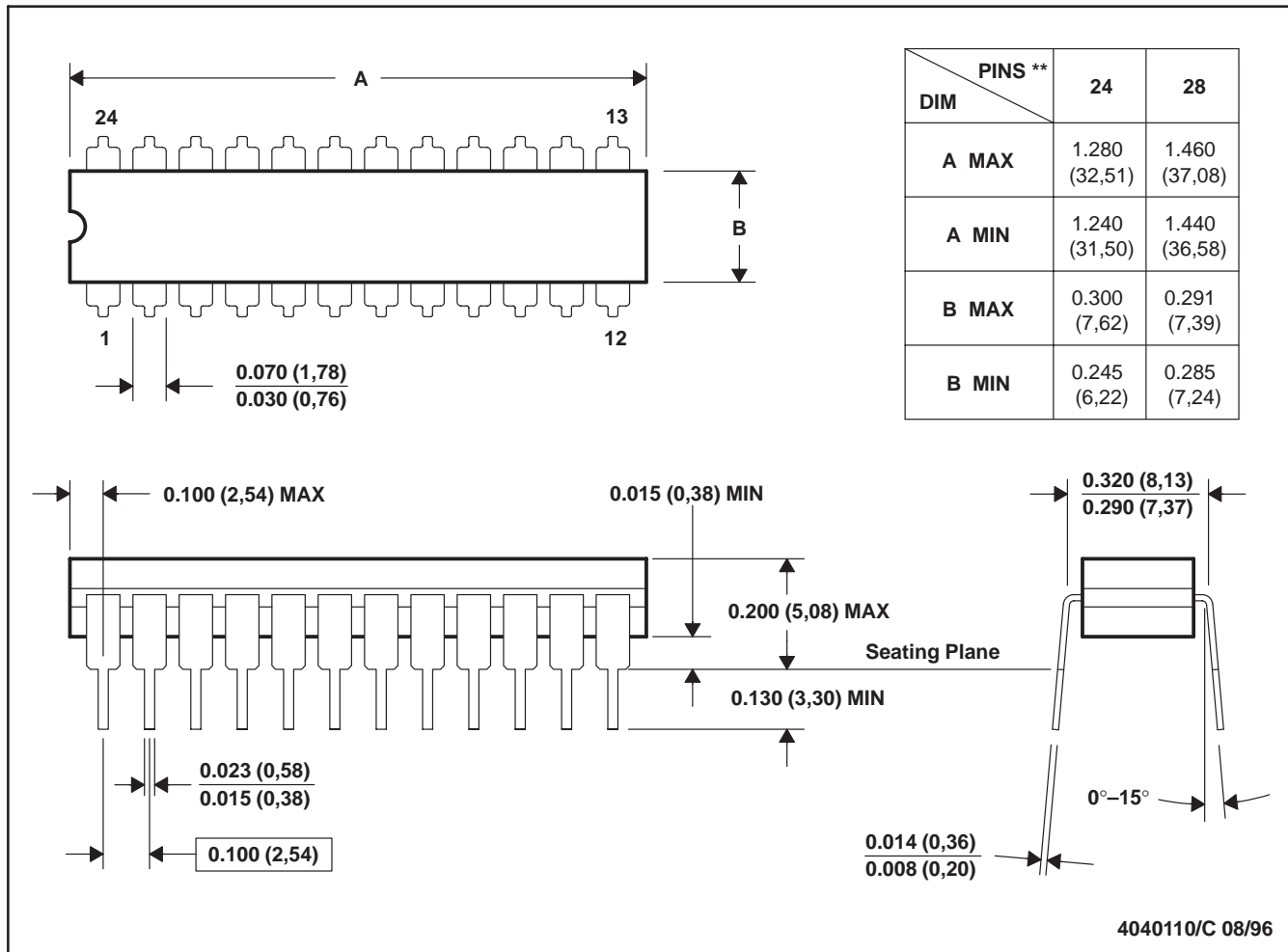
4040050/C 04/09

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



4040110/C 08/96

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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