

# SN54ABT652A, SN74ABT652A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS072F – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

## description

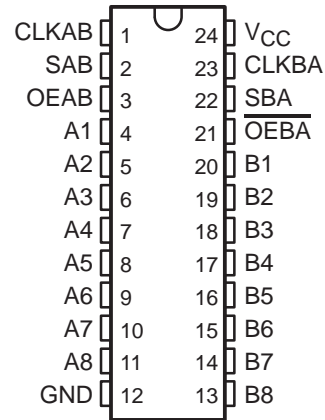
These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and  $\overline{OEBA}$ ) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select either real-time or stored data for transfer. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT652A.

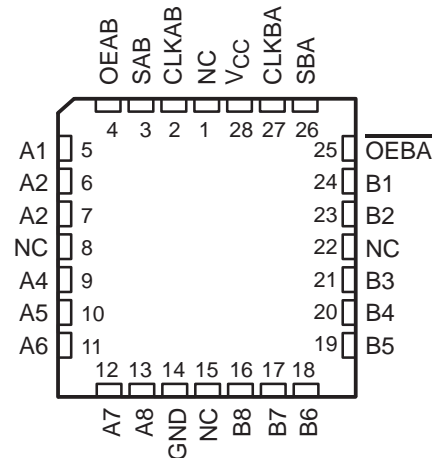
Data on the A- or B-data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control inputs. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

SN54ABT652A . . . JT OR W PACKAGE  
SN74ABT652A . . . DB, DW, NT, OR PW PACKAGE  
(TOP VIEW)



SN54ABT652A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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INSTRUMENTS

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## description (continued)

The SN54ABT652A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  
The SN74ABT652A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

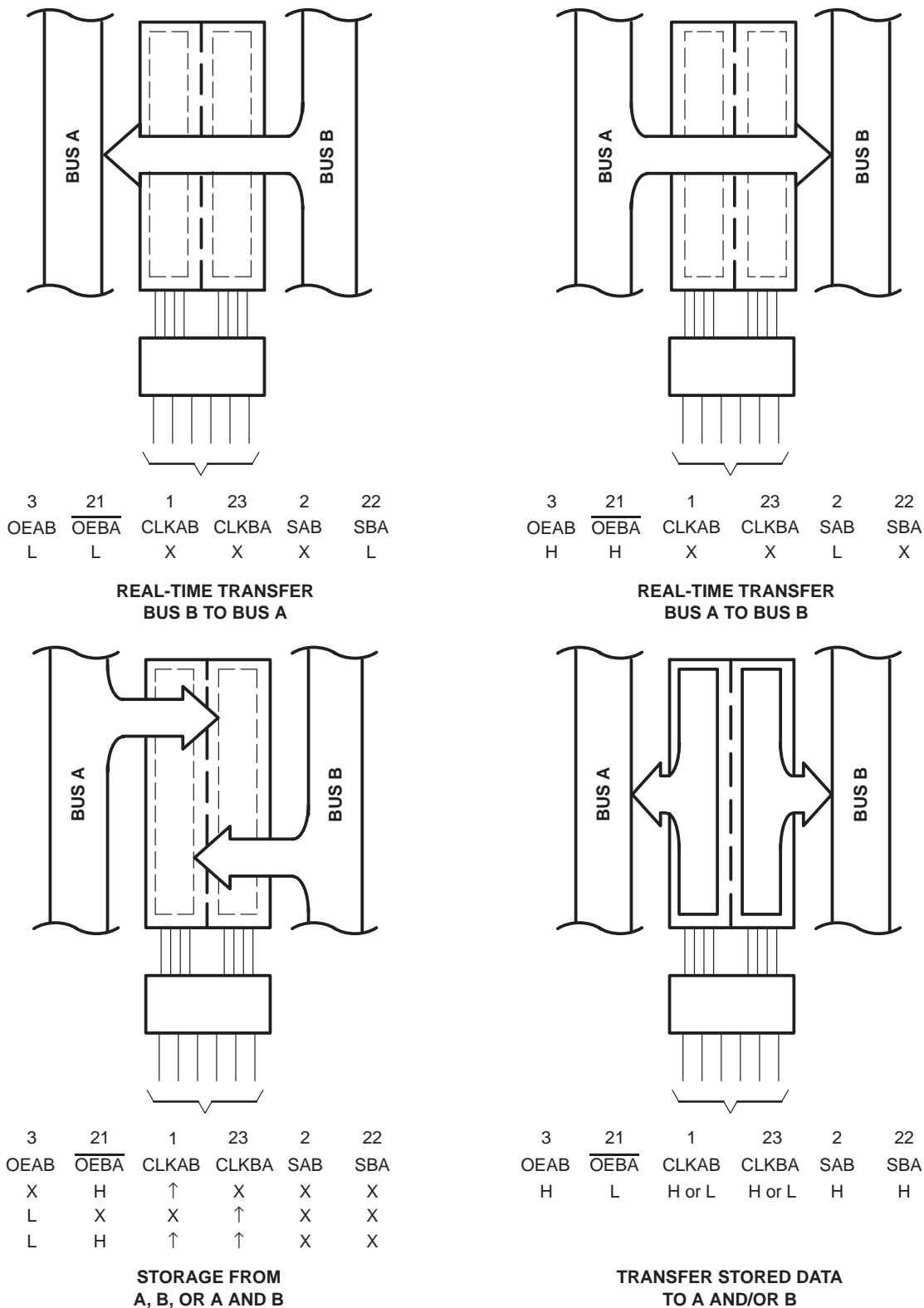
† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or  $\overline{\text{OEBA}}$ . Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

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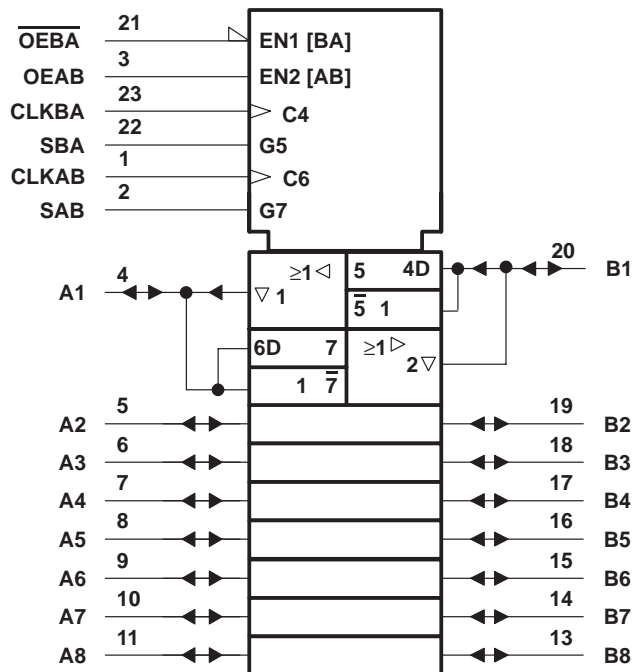
Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

**Figure 1. Bus-Management Functions**

# SN54ABT652A, SN74ABT652A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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## logic symbol†

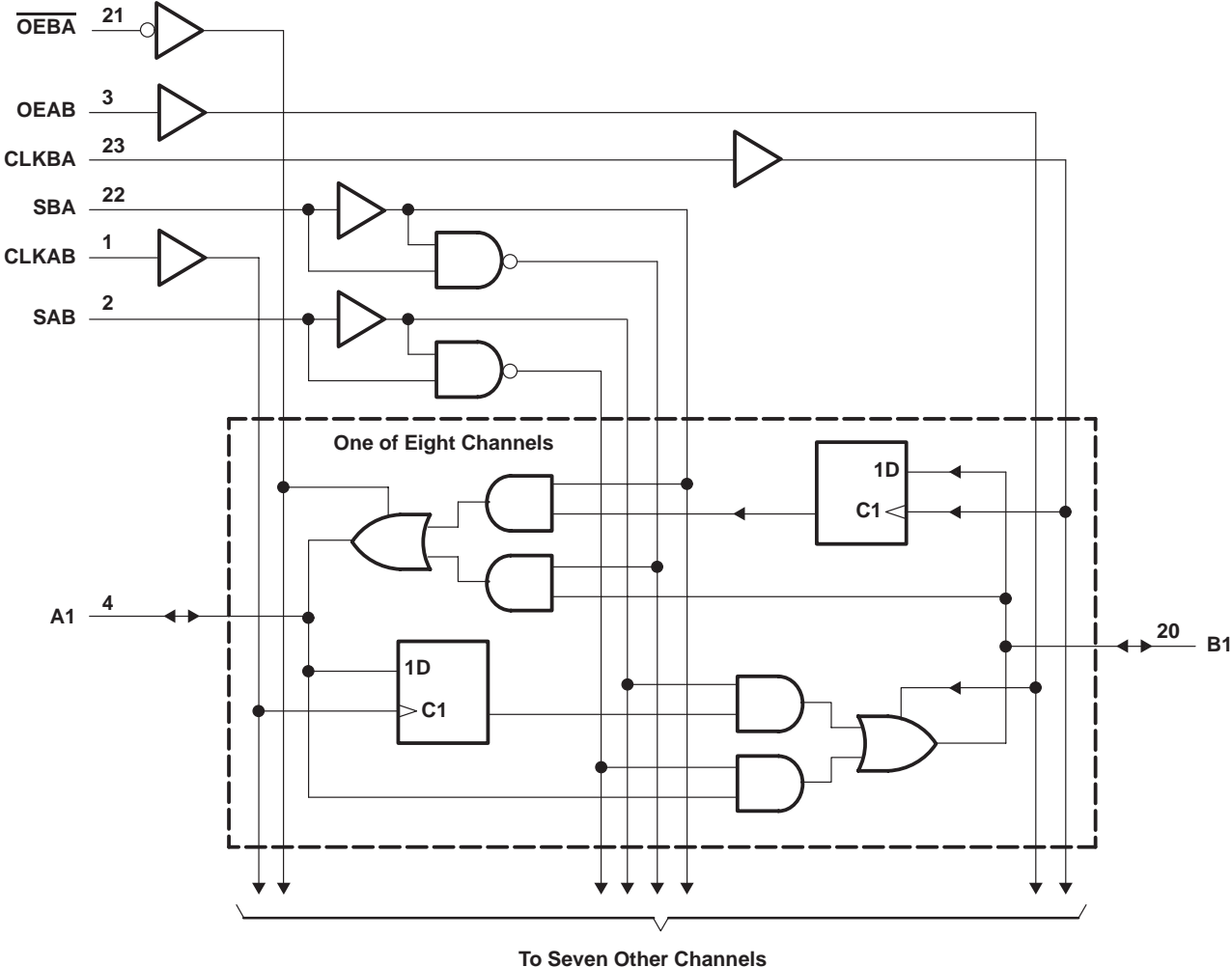


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.



# SN54ABT652A, SN74ABT652A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT652A .....	96 mA
SN74ABT652A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	104°C/W
DW package .....	81°C/W
NT package .....	67°C/W
PW package .....	120°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions (see Note 3)

		SN54ABT652A		SN74ABT652A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
	Outputs enabled					
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



# SN54ABT652A, SN74ABT652A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT652A		SN74ABT652A		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5		2.5		2.5	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		3		3		
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA			2		2			
I <sub>OH</sub> = -32 mA				2*				2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA				0.55			V	
		I <sub>OL</sub> = 64 mA				0.55*		0.55		
V <sub>hys</sub>				100					mV	
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1	±1	μA
	A or B ports					±100		±100	±100	
I <sub>OZH</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50**		10		50	μA	
I <sub>OZL</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50**		-10		-50	μA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high				50		50	μA	
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			-50	-100	-180		-50	-180	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high				250		250	250	μA
		Outputs low				30		30	30	mA
		Outputs disabled				250		250	250	μA
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					1.5		1.5	mA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V				7			pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V				12			pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* These limits apply only to the SN74ABT652A.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABT652A, SN74ABT652A**  
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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

	SN54ABT652A				UNIT
	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	
	MIN	MAX			
f <sub>clock</sub> Clock frequency	0	125	0	125	MHz
t <sub>w</sub> Pulse duration, CLK high or low	4		4		ns
t <sub>su</sub> Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		ns
t <sub>h</sub> Hold time, A or B after CLKAB↑ or CLKBA↑	1.5		1.5		ns

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

	SN74ABT652A				UNIT
	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	
	MIN	MAX			
f <sub>clock</sub> Clock frequency	0	125	0	125	MHz
t <sub>w</sub> Pulse duration, CLK high or low	4		4		ns
t <sub>su</sub> Setup time, A or B before CLKAB↑ or CLKBA↑	3		3		ns
t <sub>h</sub> Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		ns



# SN54ABT652A, SN74ABT652A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT652A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
$f_{max}$			125	200		125	MHz	
$t_{PLH}$	CLK	B or A	2.2	4	5.1	1.7	5.9	ns
$t_{PHL}$			1.7	4	5.1	1.7	5.9	
$t_{PLH}$	A or B	B or A	1.5	3	4.8	1	5	ns
$t_{PHL}$			1.5	3.3	4.6	1	5.6	
$t_{PLH}$	SAB or SBA†	B or A	1.5	4	5.5	1.5	6.8	ns
$t_{PHL}$			1.5	3.6	4.9	1.5	6.2	
$t_{PZH}$	$\overline{OEBA}$	A	2	3.6	5.4	2	6.8	ns
$t_{PZL}$			3	5.7	7.7	3	9.2	
$t_{PHZ}$	$\overline{OEBA}$	A	1.5	3.2	5.8	1	7.5	ns
$t_{PLZ}$			1.5	3	4.3	1	4.6	
$t_{PZH}$	OEAB	B	2	4.3	6.1	2	7.8	ns
$t_{PZL}$			3	5.5	7.4	3	8.9	
$t_{PHZ}$	OEAB	B	1.5	3.3	6	1	8	ns
$t_{PLZ}$			1.5	3.4	5	1.5	6.8	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT652A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
$f_{max}$			125	200		125	MHz	
$t_{PLH}$	CLK	B or A	2.2	4	5.1	2.2	5.6	ns
$t_{PHL}$			1.7	4	5.1	1.7	5.6	
$t_{PLH}$	A or B	B or A	1.5	3	4.3	1.5	4.8	ns
$t_{PHL}$			1.5	3.3	4.6	1.5	5.4	
$t_{PLH}$	SAB or SBA†	B or A	1.5	4	5.1	1.5	6.5	ns
$t_{PHL}$			1.5	3.6	4.9	1.5	5.9	
$t_{PZH}$	$\overline{OEBA}$	A	2	3.6	4.6	2	5.8	ns
$t_{PZL}$			3	5.7	6.8	3	8.5	
$t_{PHZ}$	$\overline{OEBA}$	A	1.5	3.2	4.5	1.5	5	ns
$t_{PLZ}$			1.5	3	3.8	1.5	4.1	
$t_{PZH}$	OEAB	B	2	4.3	6.1	2	6.5	ns
$t_{PZL}$			3	5.5	6.5	3	7.4	
$t_{PHZ}$	OEAB	B	1.5	3.3	4.5	1.5	5.5	ns
$t_{PLZ}$			1.5	3.4	4.4	1.5	5.1	

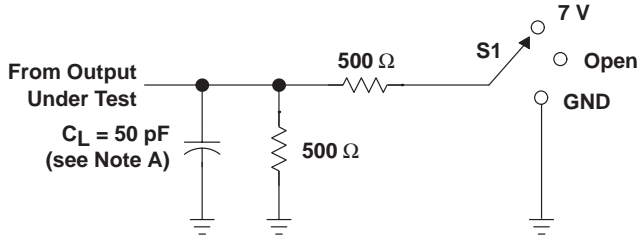
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.



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**WITH 3-STATE OUTPUTS**

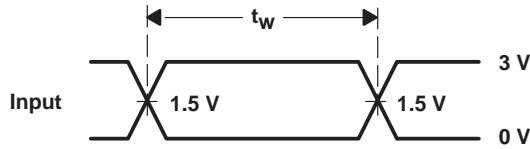
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**PARAMETER MEASUREMENT INFORMATION**

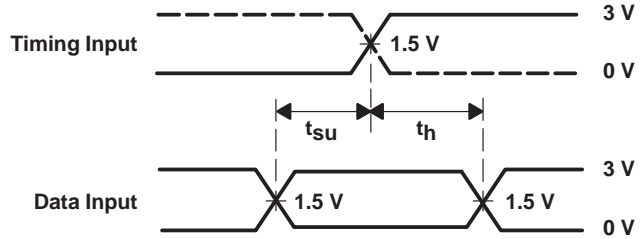


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

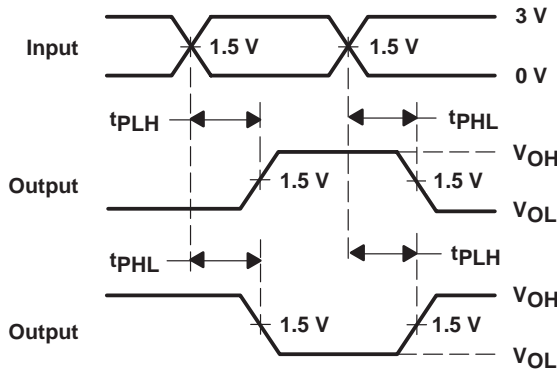
**LOAD CIRCUIT**



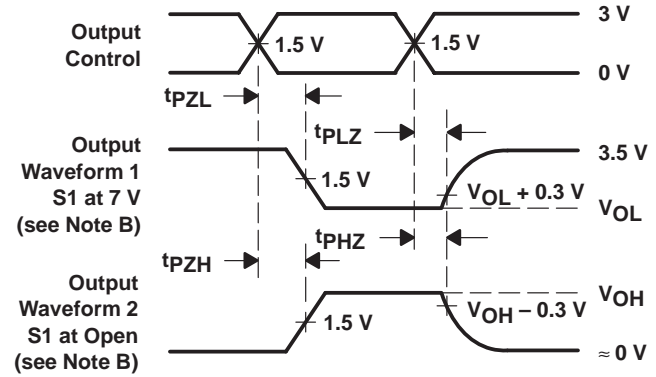
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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