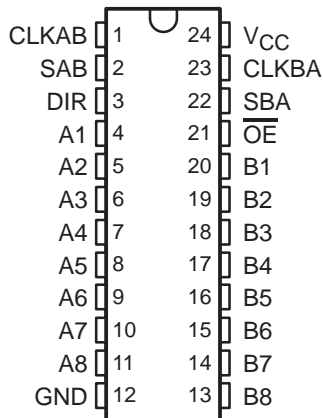


SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

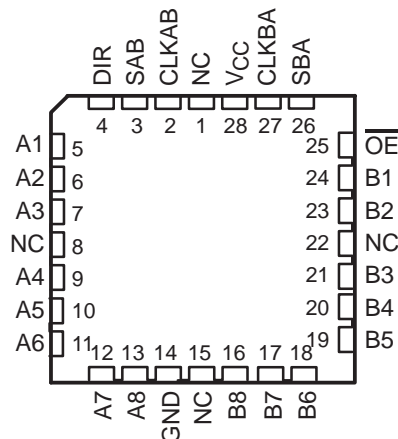
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- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54ABT646A . . . JT OR W PACKAGE
SN74ABT646A . . . DB, DGV, DW, NS, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT646A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT646A devices.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – NT	Tube	SN74ABT646ANT	SN74ABT646ANT
	SOIC – DW	Tube	SN74ABT646ADW	ABT646A
		Tape and reel	SN74ABT646ADWR	
	SOP – NS	Tape and reel	SN74ABT646ANSR	ABT646A
	SSOP – DB	Tape and reel	SN74ABT646ADBR	AB646A
	TSSOP – PW	Tube	SN74ABT646APW	AB646A
		Tape and reel	SN74ABT646APWR	
TVSOP – DGV	Tape and reel	SN74ABT646ADGVR	AB646A	
-55°C to 125°C	CDIP – JT	Tube	SNJ54ABT646AJT	SNJ54ABT646AJT
	CFP – W	Tube	SNJ54ABT646AW	SNJ54ABT646AW
	LCCC – FK	Tube	SNJ54ABT646AFK	SNJ54ABT646AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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description/ordering information(continued)

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

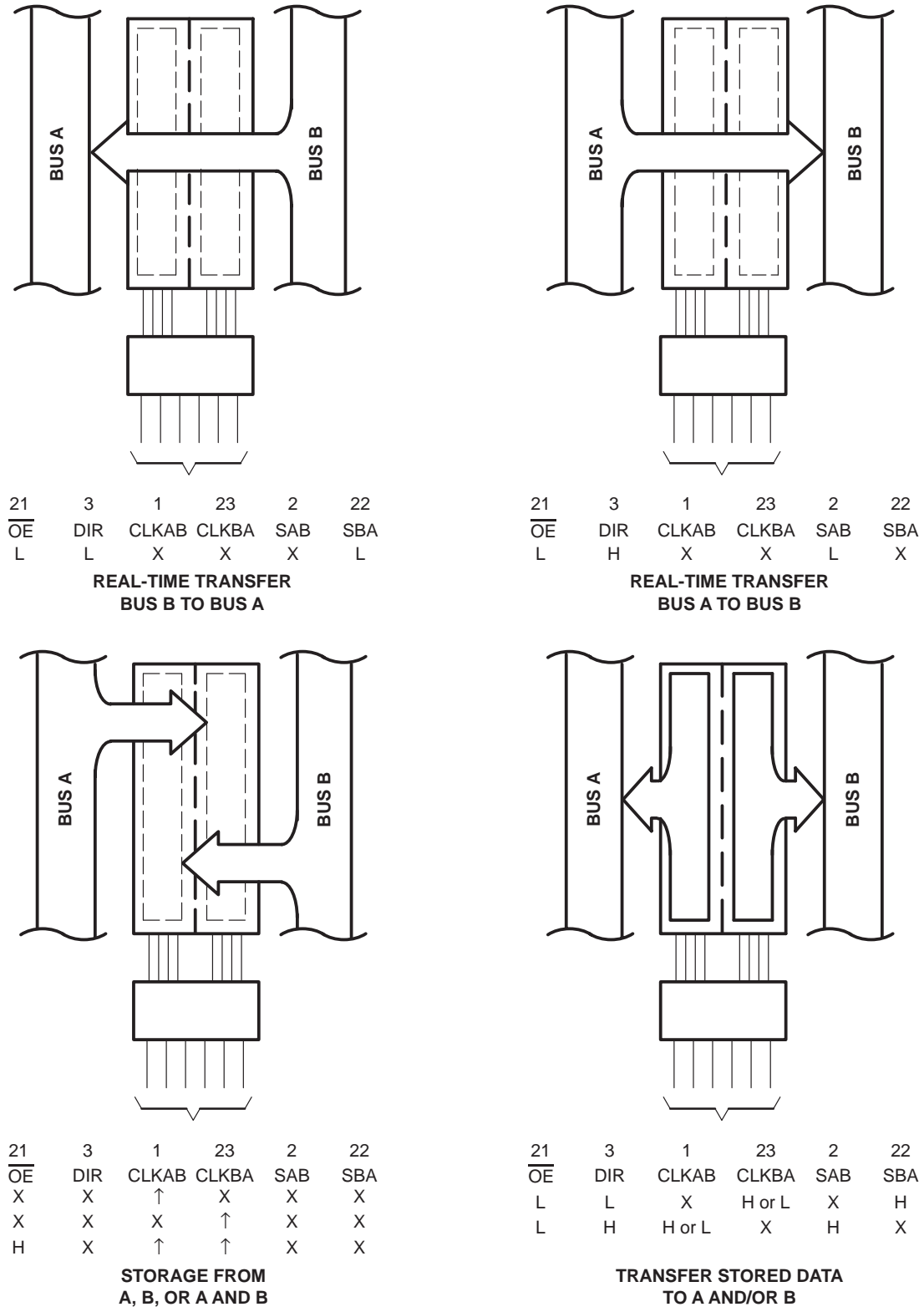
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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Pin numbers shown are for the DB, DGV, DW, JT, NS, NT, PW, and W packages.

Figure 1. Bus-Management Functions

SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

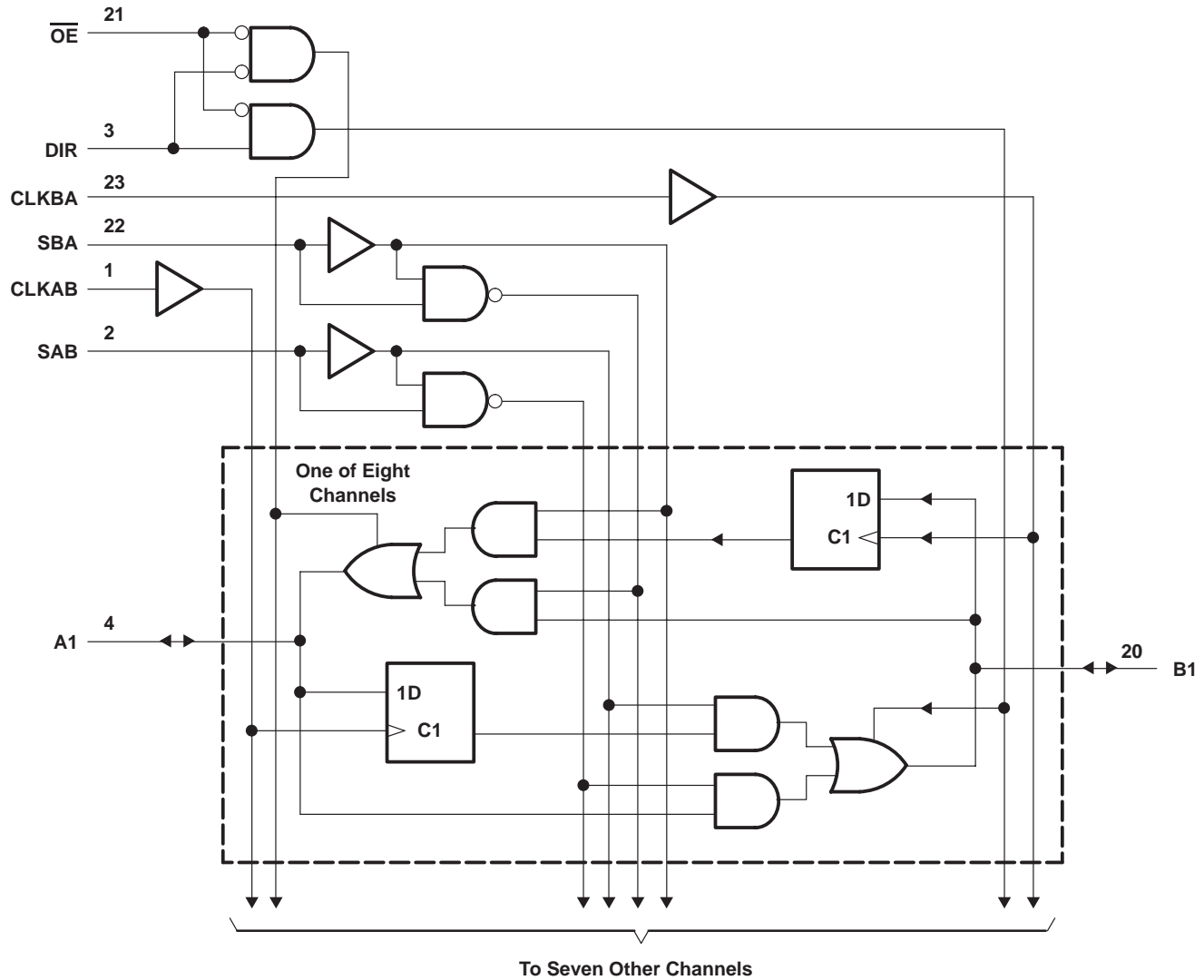
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FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data-output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, NT, PW, and W packages.



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SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT646A	96 mA
SN74ABT646A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	63°C/W
(see Note 2): DGV package	86°C/W
(see Note 2): DW package	46°C/W
(see Note 2): NS package	65°C/W
(see Note 3): NT package	67°C/W
(see Note 2): PW package	88°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-3.

recommended operating conditions (see Note 4)

	SN54ABT646A		SN74ABT646A		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		-24		-32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		5		5	ns/V
T_A Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT646A		SN74ABT646A		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5	V	
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA		2		2				
		I _{OH} = -32 mA		2*				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA				0.55		0.55	V	
		I _{OL} = 64 mA				0.55*		0.55		
V _{hys}				100					mV	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports				±100		±100		±100	
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			10§		10§		10§	μA	
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			-10§		-10§		-10§	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50	50	μA	
I _O ¶	V _{CC} = 5.5 V, V _O = 2.5 V			-50	-100	-180		-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			250		250	250	μA	
		Outputs low			30		30	30	mA	
		Outputs disabled			250		250	250	μA	
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA	
C _i	Control inputs	V _I = 2.5 V or 0.5 V			7				pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			12				pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data-sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN54ABT646A				UNIT
		V _{CC} = 5 V, T _A = 25°C		MIN	MAX	
		MIN	MAX			
f _{clock}	Clock frequency		125		125	MHz
t _w	Pulse duration, CLK high or low	4		4		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3.5		ns
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑	1.5		1.5		ns



SN54ABT646A, SN74ABT646A OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN74ABT646A				UNIT	
		V _{CC} = 5 V, T _A = 25°C			MIN		MAX
		MIN	MAX				
f _{clock}	Clock frequency	125		125	MHz		
t _w	Pulse duration, CLK high or low	4		4	ns		
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	3		3	ns		
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0	ns		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT646A					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			125			125	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	6.7	ns
t _{PHL}			1.7	4	5.1	1.2	6.7	
t _{PLH}	A or B	B or A	1.5	3	4.3	1.5	5	ns
t _{PHL}			1.5	3.3	4.6	1.5	5.6	
t _{PLH}	SAB or SBA†	B or A	1.5	4	5.7	1.5	7.8	ns
t _{PHL}			1.5	3.6	4.9	1.5	6.2	
t _{pZH}	\overline{OE}	A or B	1.5	4.3	5.3	1.5	7	ns
t _{pZL}			3	5.8	8	3	10.5	
t _{PHZ}	\overline{OE}	A or B	1.5	3.5	5.8	1	7.3	ns
t _{PLZ}			1.5	3	4	1.5	5.7	
t _{pZH}	DIR	A or B	1.5	4.5	5.7	1.5	7.3	ns
t _{pZL}			2.5	6.5	9	2.5	11	
t _{PHZ}	DIR	A or B	1.5	3.8	6.5	1	9	ns
t _{PLZ}			1.5	3.8	4.7	1.2	6.7	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ABT646A, SN74ABT646A
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

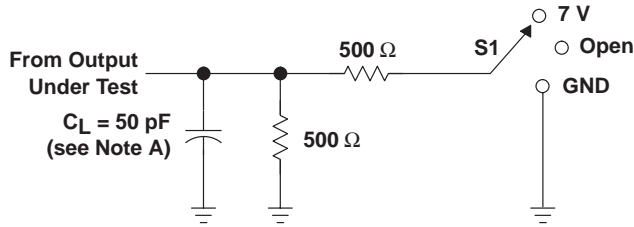
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT646A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
f_{max}			125			125	MHz	
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	3	4.3	1.5	4.8	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.4	
t_{PLH}	SAB or SBA†	B or A	1.5	4	5.1	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	5.9	
t_{PZH}	\overline{OE}	A or B	1.5	4.3	5.3	1.5	6.3	ns
t_{PZL}			3	5.8	7.4	3	8.8	
t_{PHZ}	\overline{OE}	A or B	1.5	3.5	4.5	1.5	5	ns
t_{PLZ}			1.5	3	4	1.5	4.5	
t_{PZH}	DIR	A or B	1.5	4.5	5.7	1.5	6.7	ns
t_{PZL}			2.5	6.5	9	2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	5	1.5	5.7	ns
t_{PLZ}			1.5	3.8	4.7	1.5	6	

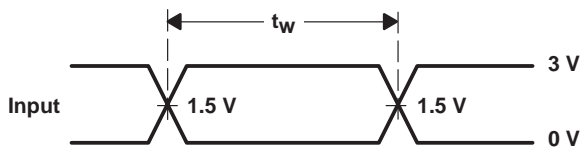
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

PARAMETER MEASUREMENT INFORMATION

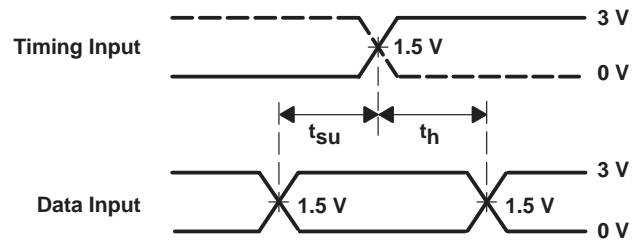


LOAD CIRCUIT

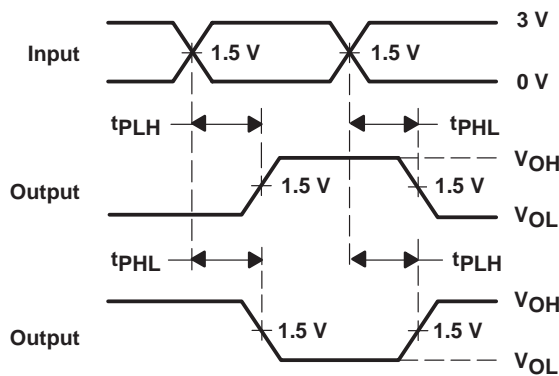
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



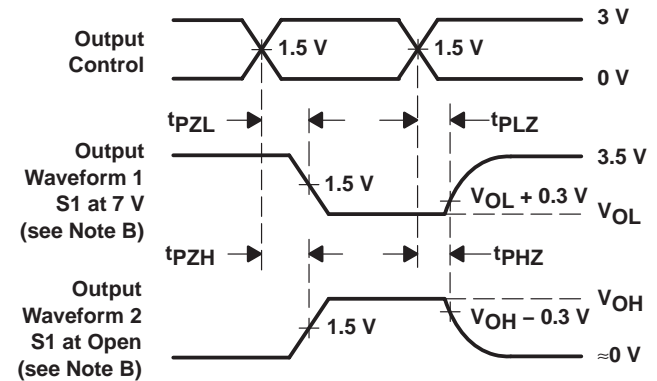
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

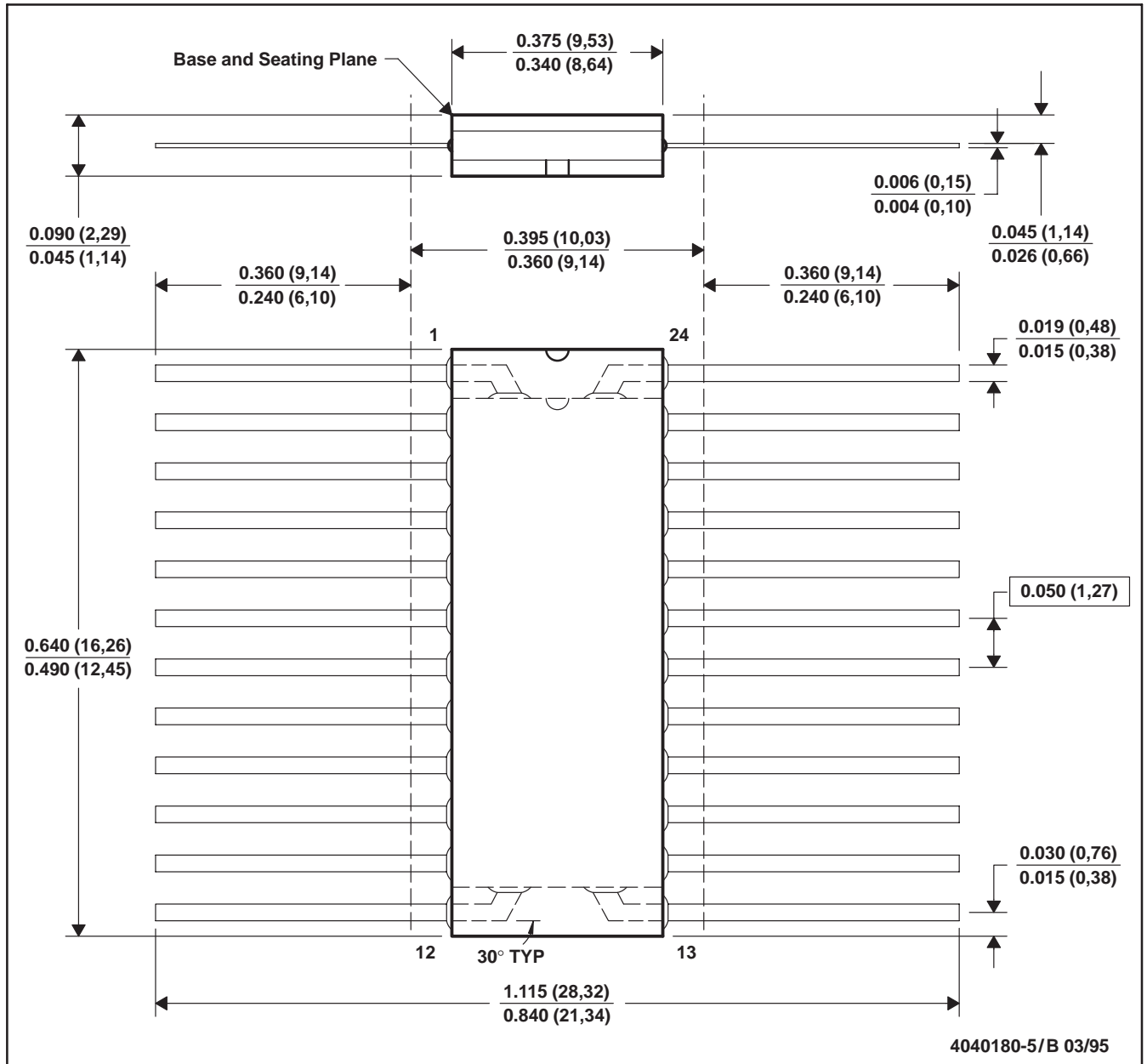
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

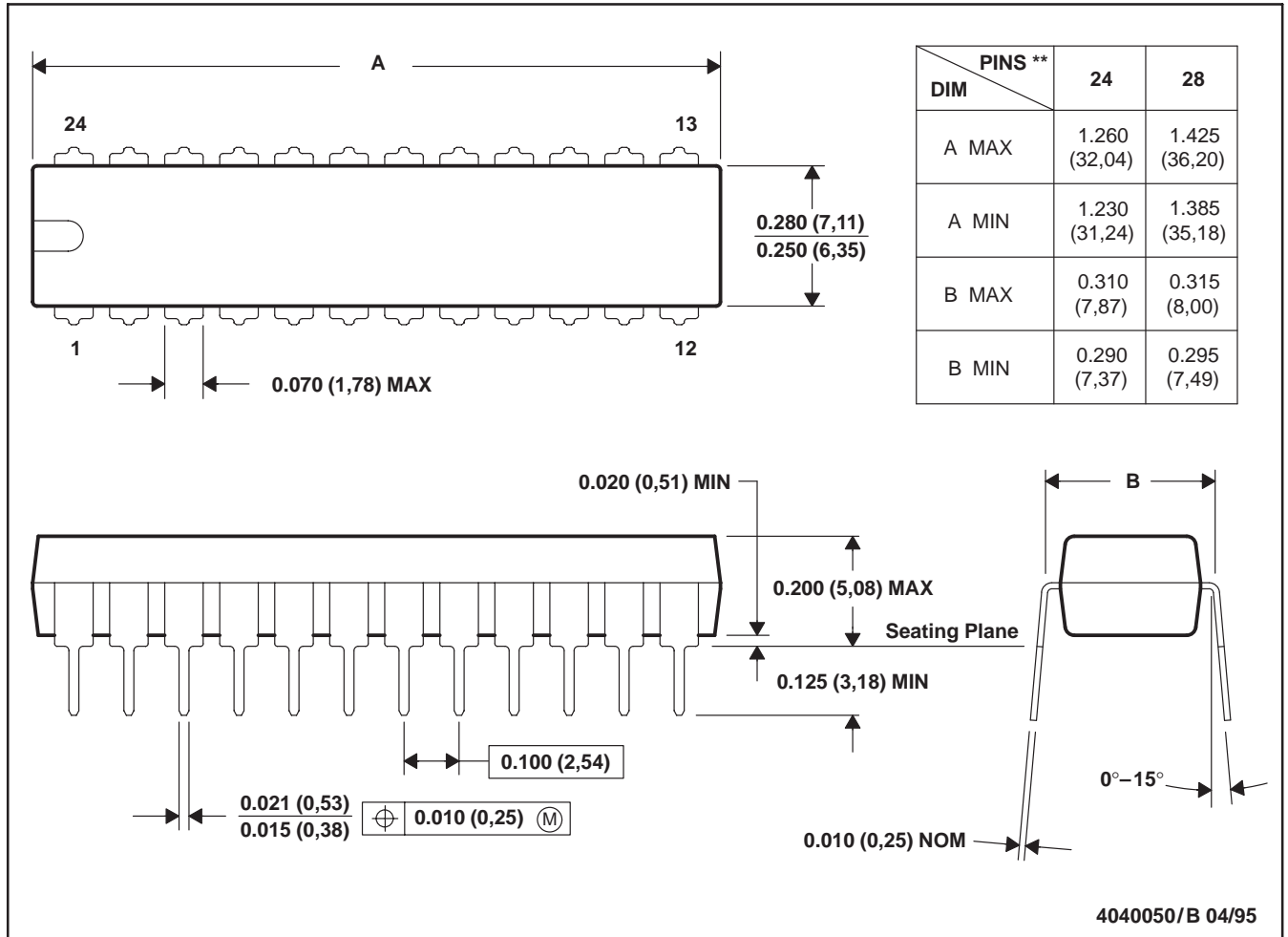


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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