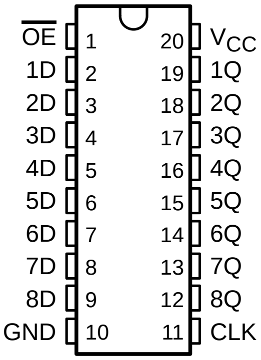
SN54ABT574, SN74ABT574A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

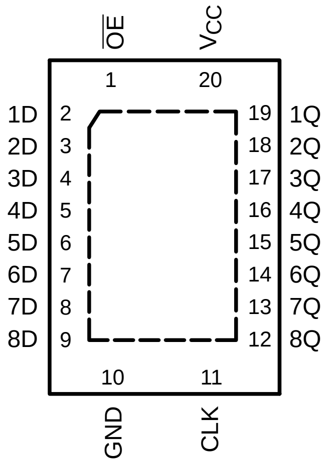
SCBS191E – JANUARY 1991 – REVISED NOVEMBER 2002

- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**

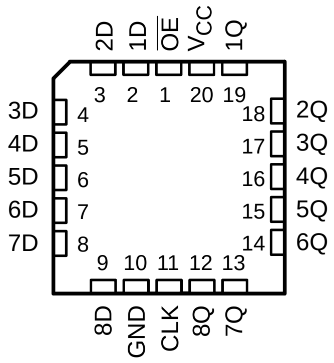
SN54ABT574 . . . J OR W PACKAGE
SN74ABT574A . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74ABT574A . . . RGY PACKAGE
(TOP VIEW)



SN54ABT574 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SN54ABT574 and SN74ABT574A are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74ABT574AN	SN74ABT574AN
	QFN – RGY	Tape and reel	SN74ABT574ARGYR	AB574A
	SOIC – DW	Tube	SN74ABT574ADW	ABT574A
		Tape and reel	SN74ABT574ADWR	
	SOP – NS	Tape and reel	SN74ABT574ANSR	ABT574A
	SSOP – DB	Tape and reel	SN74ABT574ADBR	AB574A
	TSSOP – PW	Tape and reel	SN74ABT574APWR	AB574A
	VFBGA – GQN	Tape and reel	SN74ABT574AGQNR	AB574A
–55°C to 125°C	CDIP – J	Tube	SNJ54ABT574J	SNJ54ABT574J
	CFP – W	Tube	SNJ54ABT574W	SNJ54ABT574W
	LCCC – FK	Tube	SNJ54ABT574FK	SNJ54ABT574FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description/ordering information (continued)

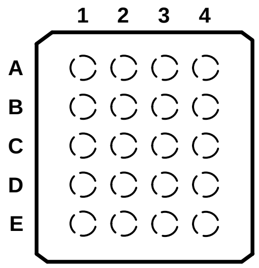
A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{\text{OE}}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

SN74ABT574A . . . GQN PACKAGE
(TOP VIEW)



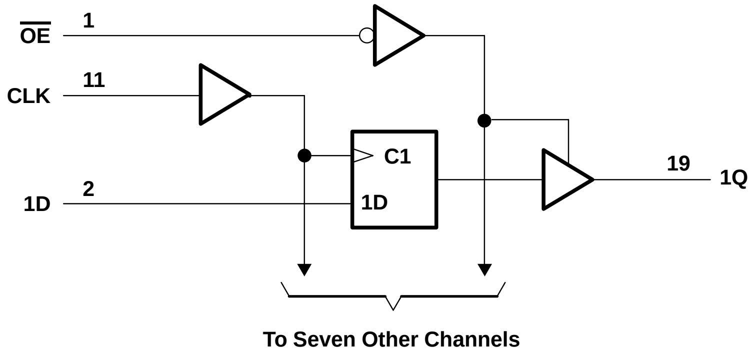
terminal assignments

	1	2	3	4
A	1D	$\overline{\text{OE}}$	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

FUNCTION TABLE
(each flip-flop)

INPUTS			**OUTPUT Q**
$\overline{\text{OE}}$	**CLK**	**D**	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I (see Note 1)		–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O		–0.5 V to 5.5 V
Current into any output in the low state, I_O:	SN54ABT574	96 mA
	SN74ABT574A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)		–18 mA
Output clamp current, I_{OK} ($V_O < 0$)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	70°C/W
(see Note 2):	DW package	58°C/W
(see Note 2):	GQN package	78°C/W
(see Note 2):	N package	69°C/W
(see Note 2):	NS package	60°C/W
(see Note 2):	PW package	83°C/W
(see Note 3):	RGY package	37°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			SN54ABT574		SN74ABT574A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT574		SN74ABT574A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2			2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
V_{hys}					100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10‡		10‡		10‡	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				–10‡		–10‡		–10‡	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±500		±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V				3.5						pF
C_o	V_O = 2.5 V or 0.5 V				6.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This data sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT574				UNIT
			V_{CC} = 5 V, T_A = 25°C				
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	High	1.5		1.5		ns
		Low	2		2		
t_h	Hold time, data after CLK↑	High or low	2		2		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT574A				UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
			MIN	MAX			
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	High	1		1		ns
		Low	1.5		1.5		
t_h	Hold time, data after CLK↑	High or low	1.8[†]		1.8[†]		ns

[†] This data-sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

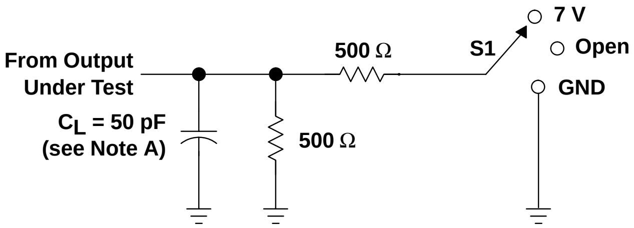
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT574					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150	200		150		MHz
t_{PLH}	CLK	Q	2.2	3.9	6.2	2.2	7	ns
t_{PHL}			3	4.8	7	3	7.4	
t_{PZH}	$\overline{OE}$	Q	1	3.3	5	1	5.8	ns
t_{PZL}			2.5	4.7	5.9	2.5	7.2	
t_{PHZ}	$\overline{OE}$	Q	2.4	4.9	6.2	2.4	7.2	ns
t_{PLZ}			2	4	5.8	2	6.9	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT574A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f_{max}			150	200		150		MHz
t_{PLH}	CLK	Q	2.2	3.9	6.2	2.2	6.8	ns
t_{PHL}			3	4.8	6.6	3	7.1	
t_{PZH}	$\overline{OE}$	Q	1	3.3	4.3	1	5.1	ns
t_{PZL}			2.1[†]	4.7	5.9	2.1[†]	6.7	
t_{PHZ}	$\overline{OE}$	Q	2.4	4.9	6.2	2.4	7	ns
t_{PLZ}			2	4	5.8	2	6.5	

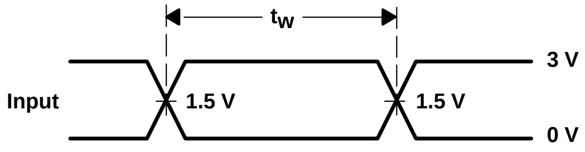
[†] This data-sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

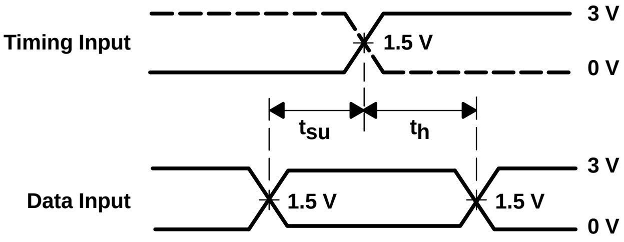


LOAD CIRCUIT

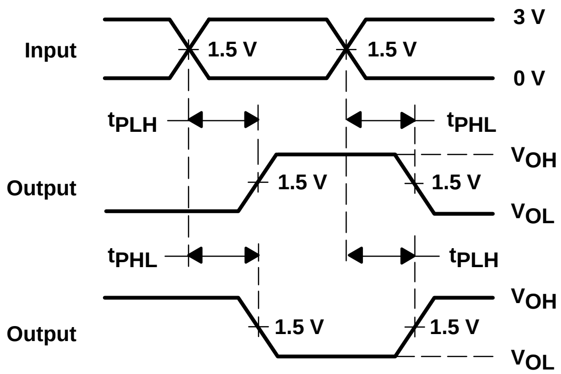
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



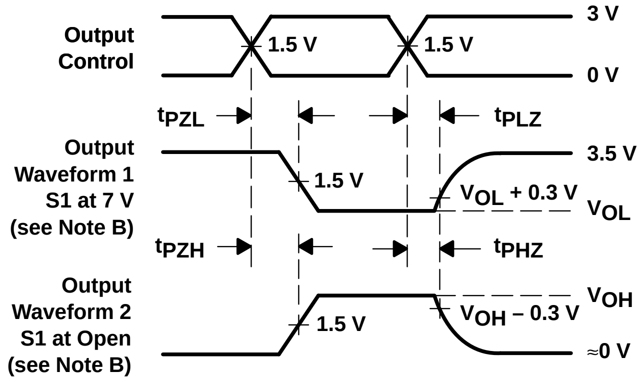
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

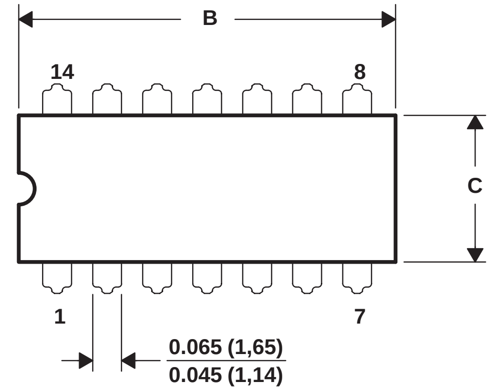
NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

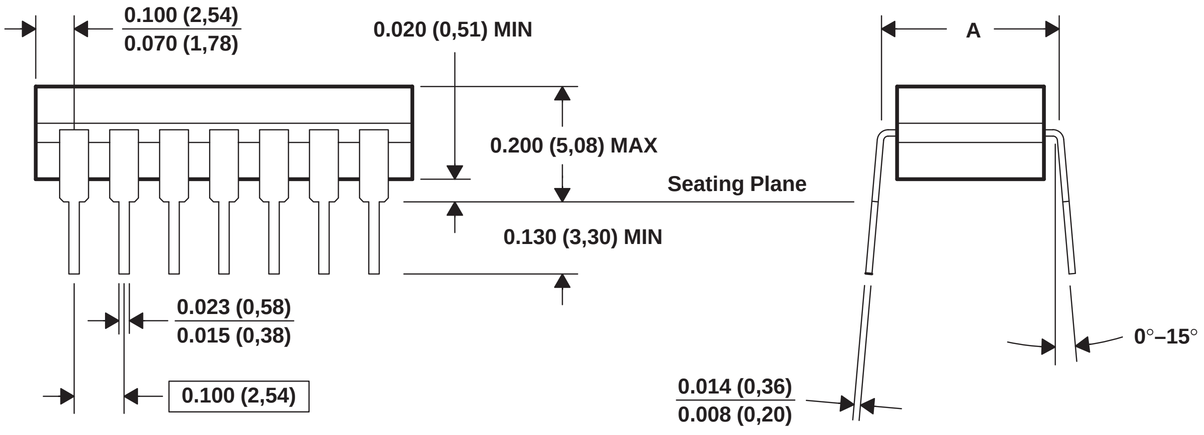
Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**) CERAMIC DUAL-IN-LINE

14 LEADS SHOWN

PINS ** / DIM	14	16	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)



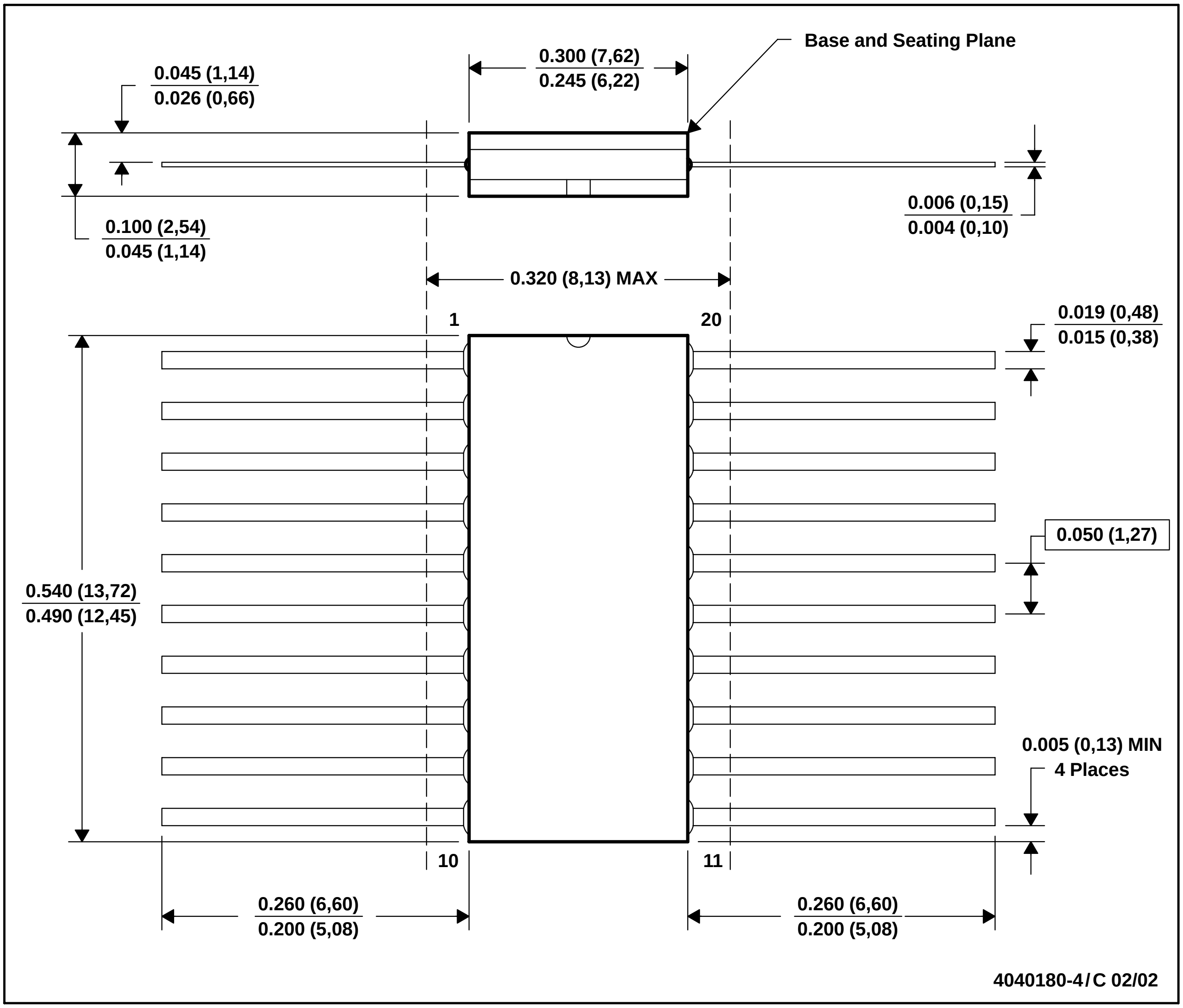


4040083/E 03/99

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

W (R-GDFP-F20)

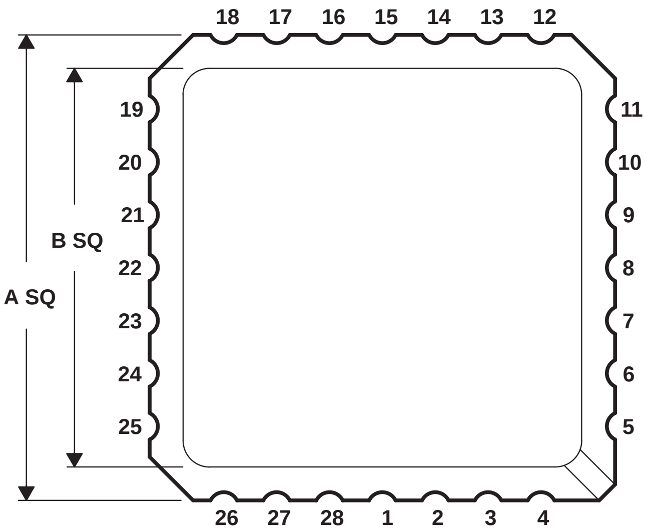
CERAMIC DUAL FLATPACK



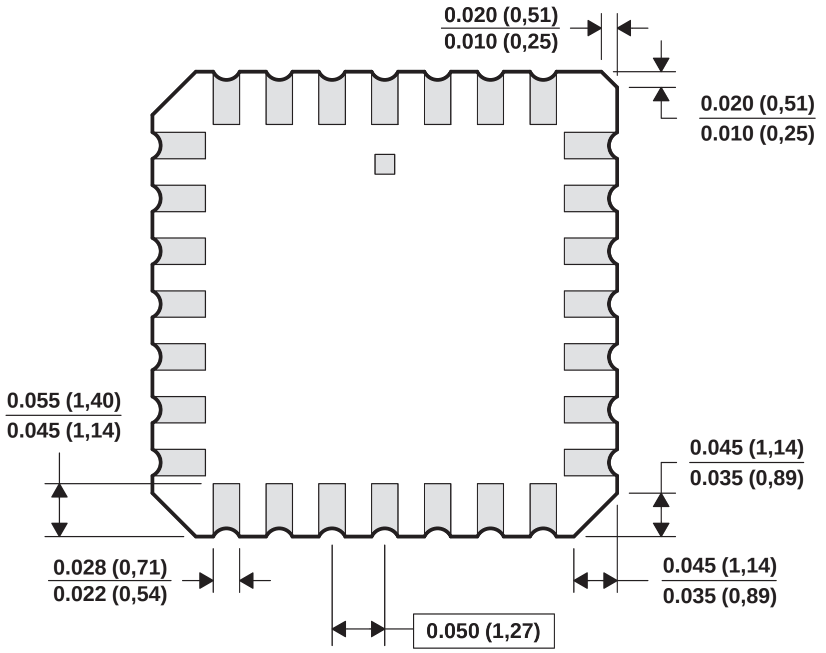
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.

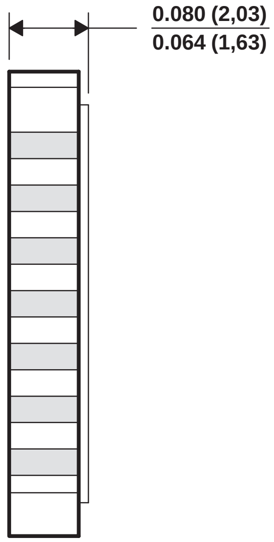
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

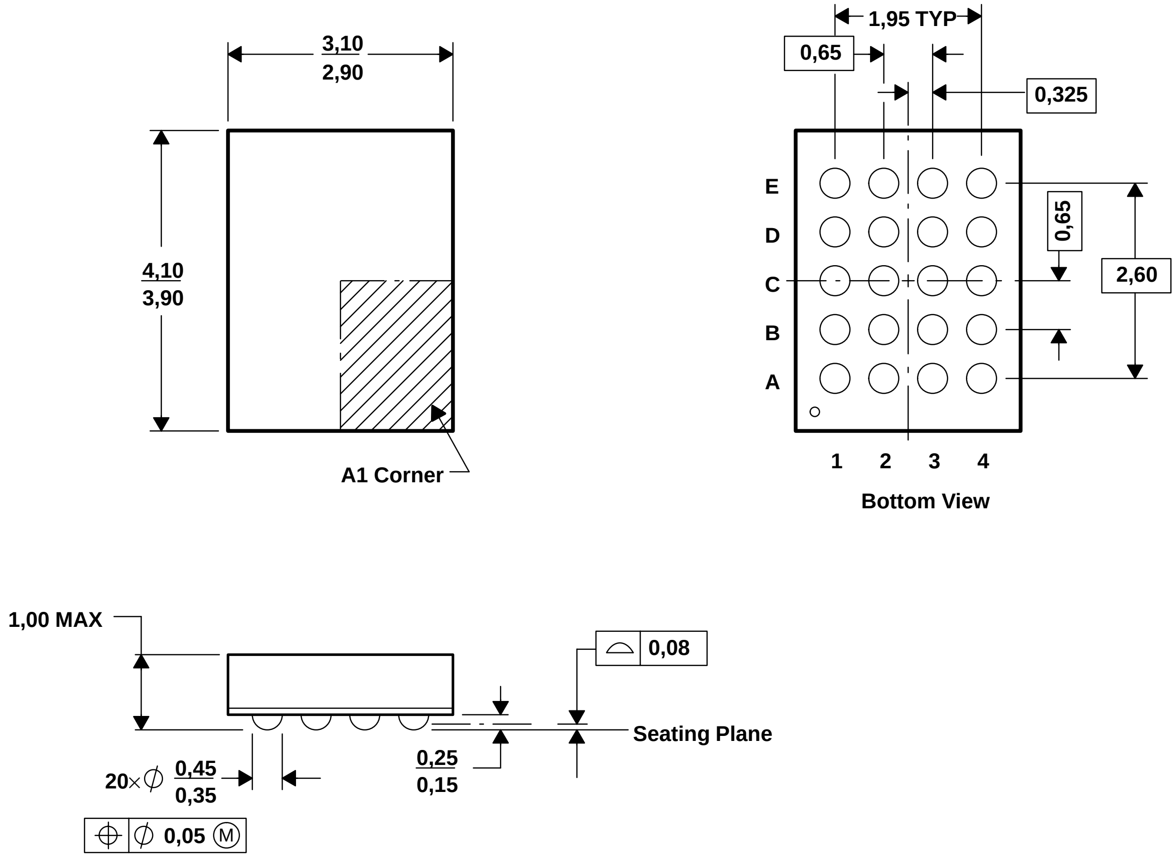




4040140 / D 10/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

GQN (R-PBGA-N20) PLASTIC BALL GRID ARRAY



4200704/D 07/2002

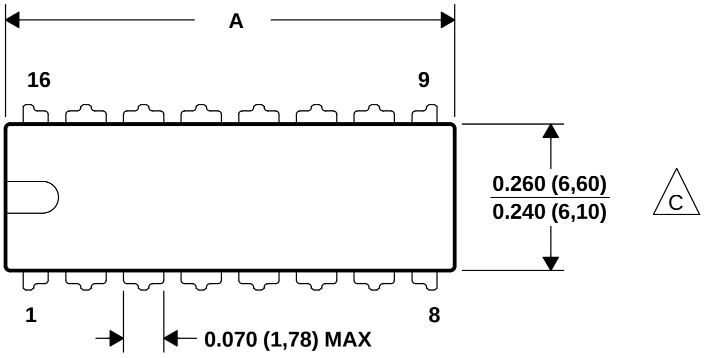
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ configuration
- D. Falls within JEDEC MO-225 variation BC.
- E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

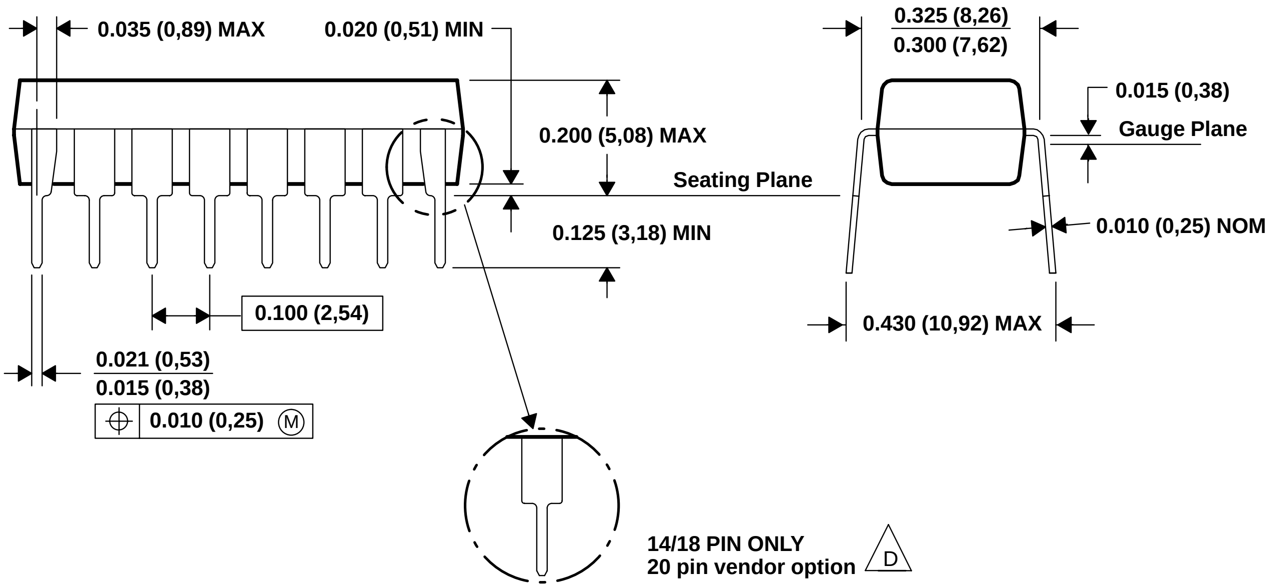
MicroStar Junior is a trademark of Texas Instruments.

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

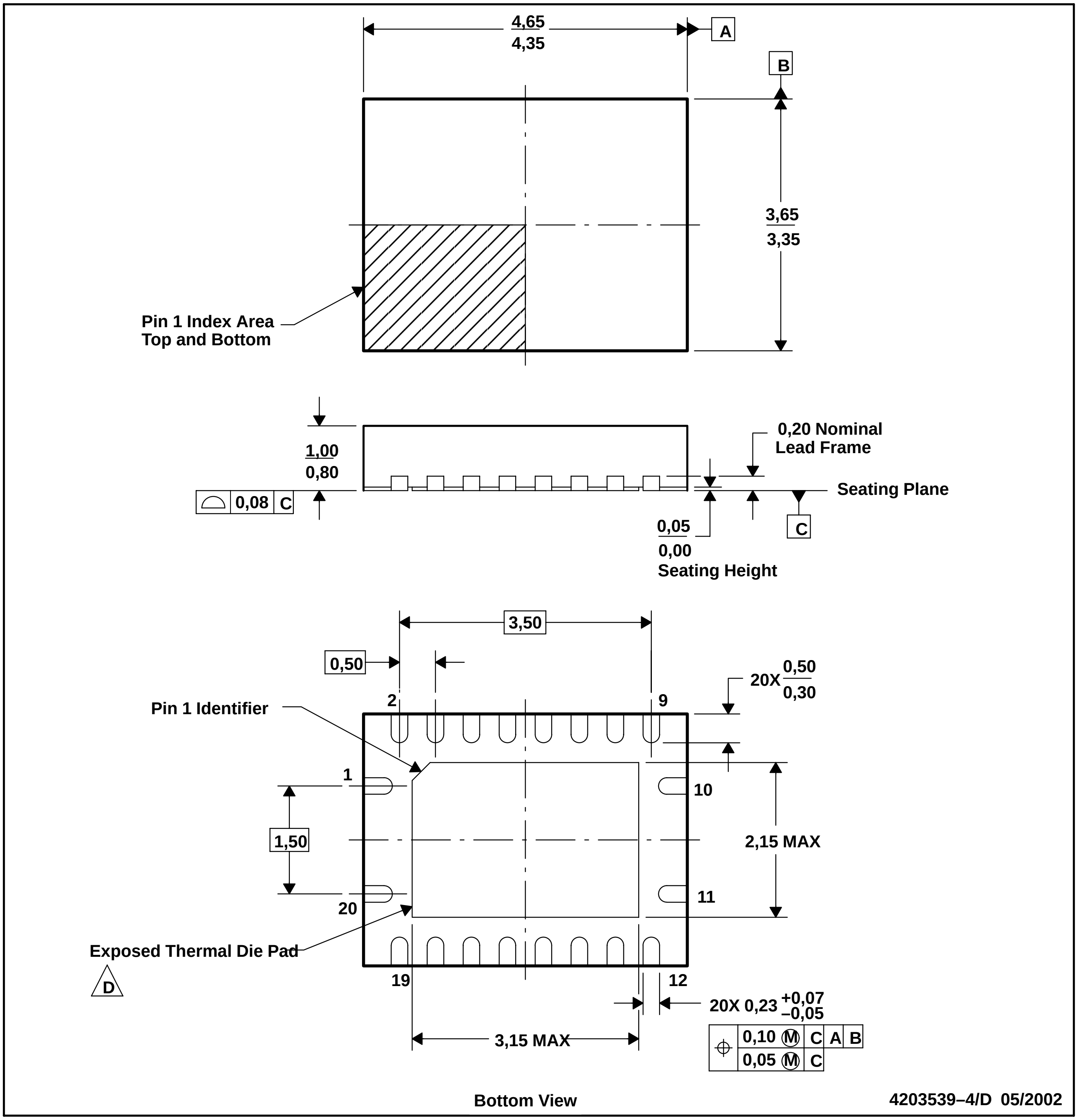




4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

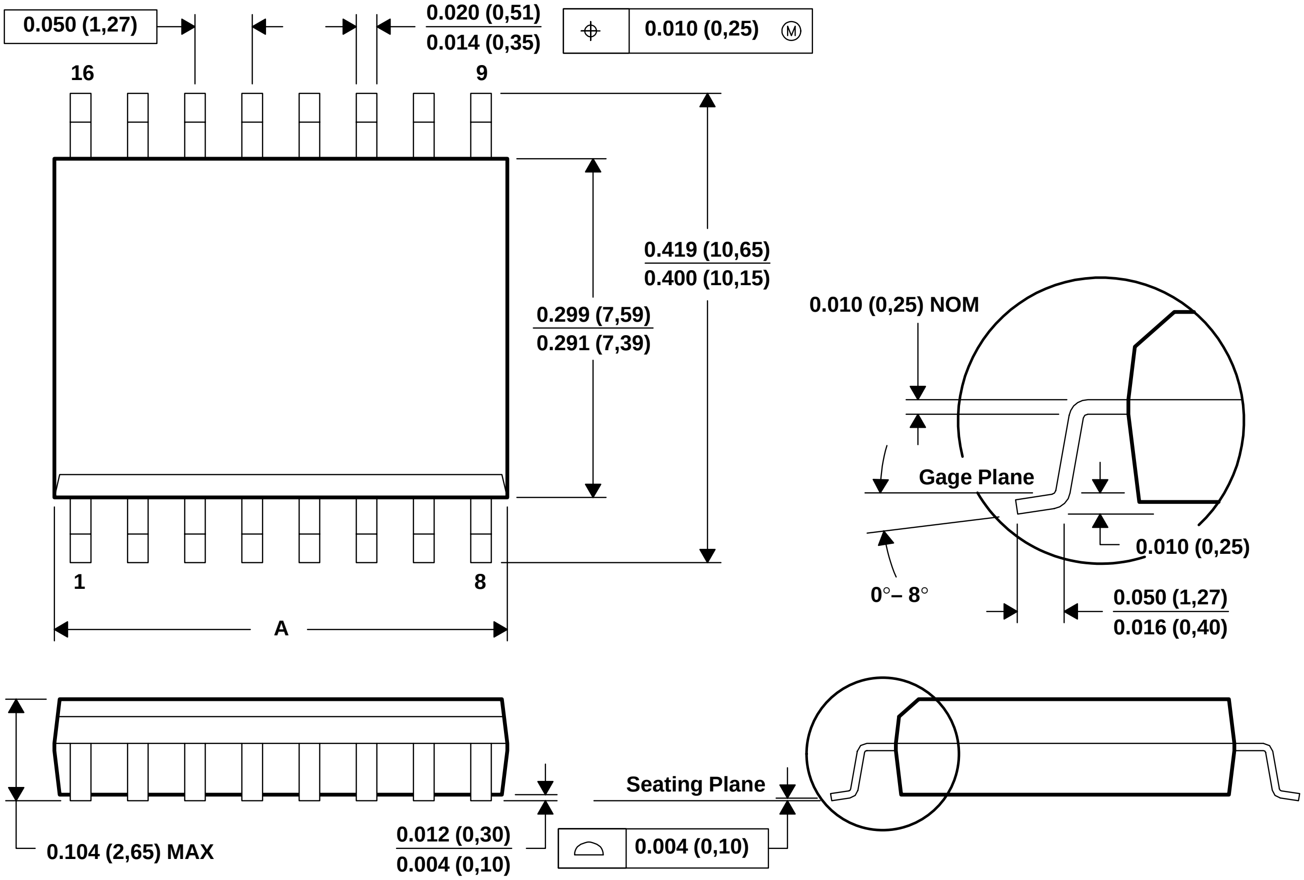
RGY (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The Package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

DW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



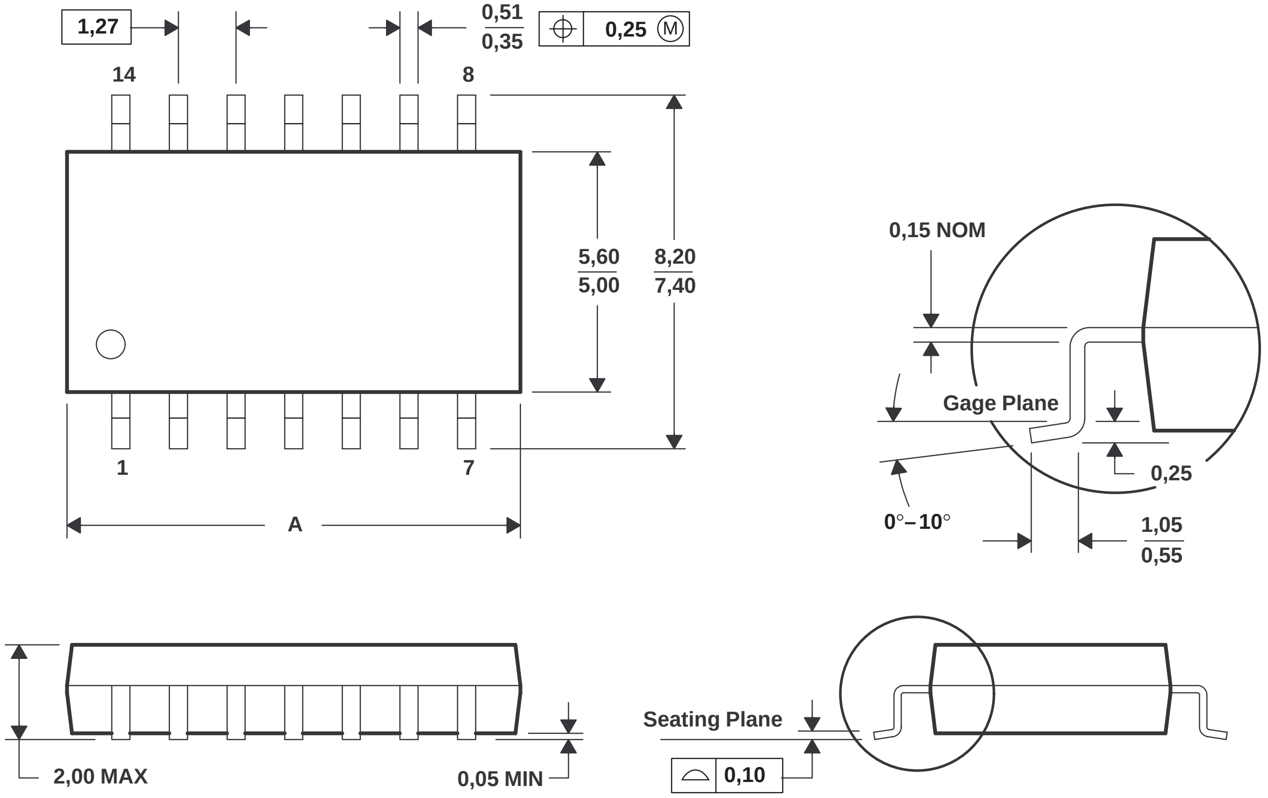
PINS ** / DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



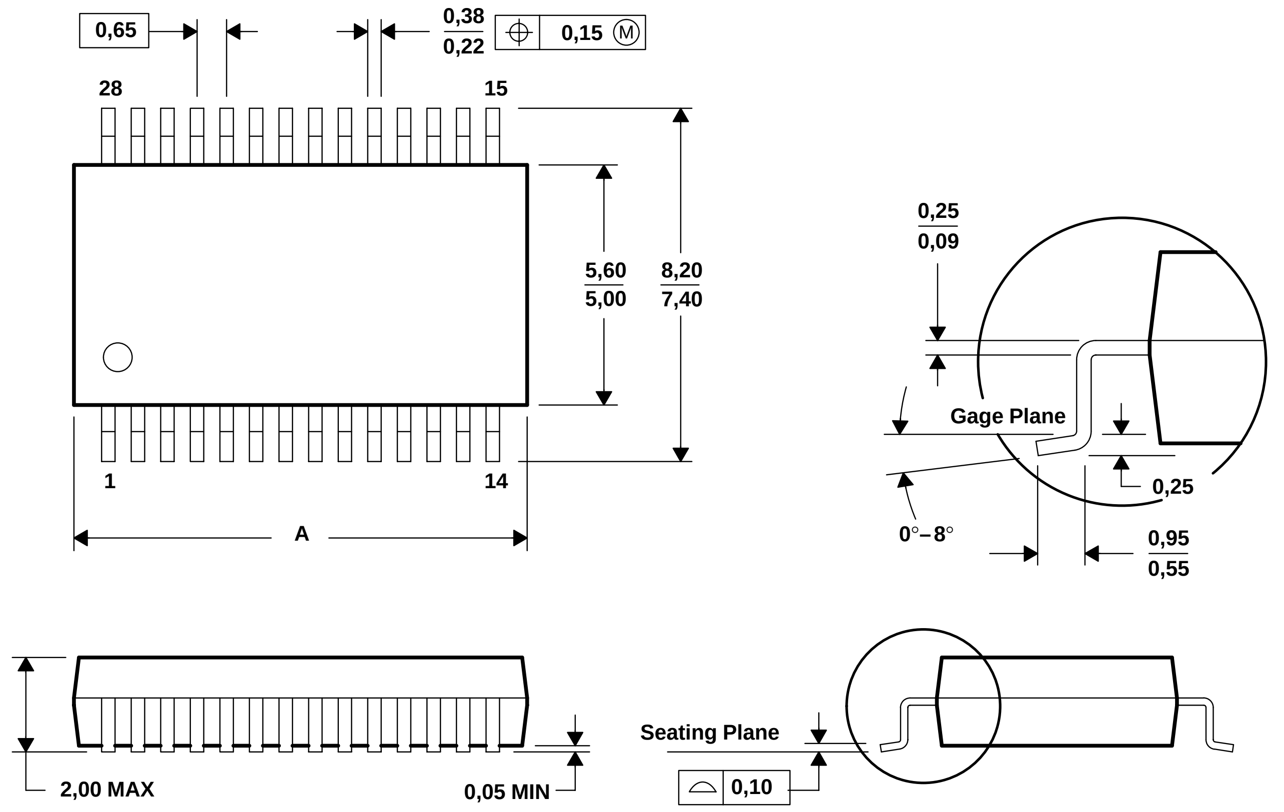
PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062 / B 02/95

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN



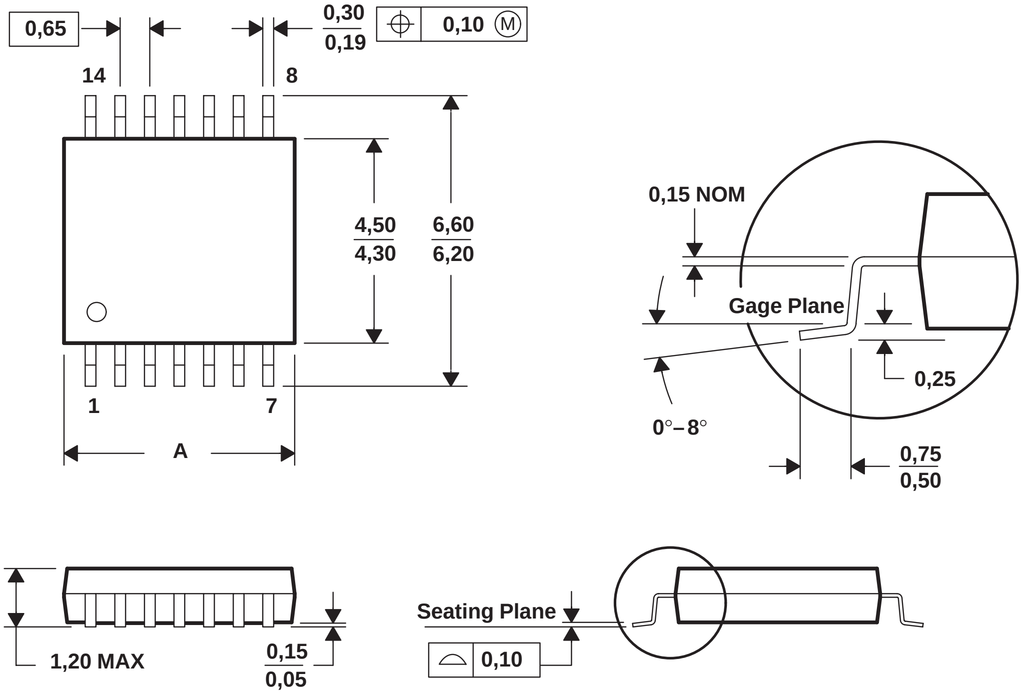
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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