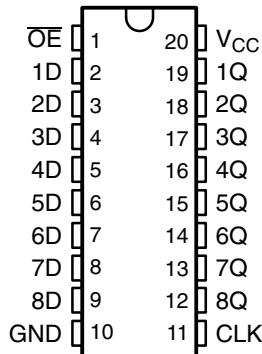


SN54ABT574, SN74ABT574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

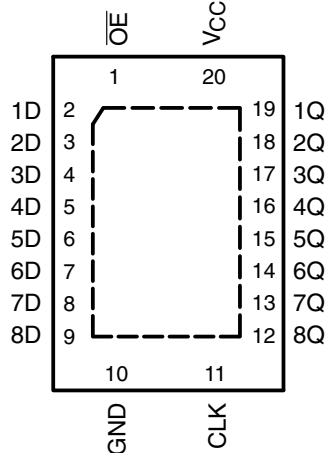
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- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

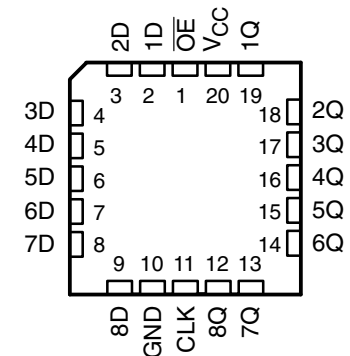
SN54ABT574 . . . J OR W PACKAGE
SN74ABT574A . . . DB, DW, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74ABT574A . . . RGY PACKAGE
(TOP VIEW)



SN54ABT574 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|-----------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube | SN74ABT574AN | SN74ABT574AN |
| | QFN – RGY | Tape and reel | SN74ABT574ARGYR | AB574A |
| | SOIC – DW | Tube | SN74ABT574ADW | ABT574A |
| | | Tape and reel | SN74ABT574ADWR | |
| | SOP – NS | Tape and reel | SN74ABT574ANSR | ABT574A |
| | SSOP – DB | Tape and reel | SN74ABT574ADBR | AB574A |
| | TSSOP – PW | Tube | SN74ABT574APW | AB574A |
| | | Tape and reel | SN74ABT574APWR | |
| VFBGA – GQN | Tape and reel | SN74ABT574AGQNR | AB574A | |
| | | SN74ABT574AZQNR | | |
| -55°C to 125°C | CDIP – J | Tube | SNJ54ABT574J | SNJ54ABT574J |
| | CFP – W | Tube | SNJ54ABT574W | SNJ54ABT574W |
| | LCCC – FK | Tube | SNJ54ABT574FK | SNJ54ABT574FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The eight flip-flops of the SN54ABT574 and SN74ABT574A are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

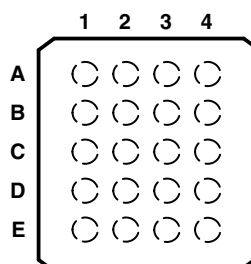
\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

SN74ABT574A . . . GQN OR ZQN PACKAGE

(TOP VIEW)



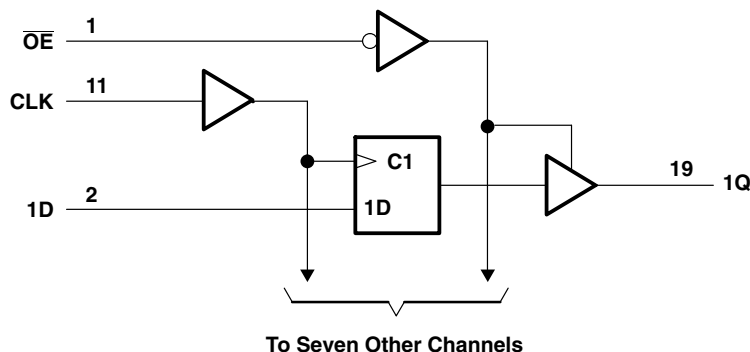
terminal assignments

| | 1 | 2 | 3 | 4 |
|---|-----|-----------------|----------|----|
| A | 1D | \overline{OE} | V_{CC} | 1Q |
| B | 3D | 3Q | 2D | 2Q |
| C | 5D | 4D | 5Q | 4Q |
| D | 7D | 7Q | 6D | 6Q |
| E | GND | 8D | CLK | 8Q |

FUNCTION TABLE (each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|------------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | \uparrow | H | H |
| L | \uparrow | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, N, NS, PW, RGY, and W packages.



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SN54ABT574, SN74ABT574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | –0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT574 | 96 mA |
| SN74ABT574A | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DB package | 70°C/W |
| (see Note 2): DW package | 58°C/W |
| (see Note 2): GQN/ZQN package | 78°C/W |
| (see Note 2): N package | 69°C/W |
| (see Note 2): NS package | 60°C/W |
| (see Note 2): PW package | 83°C/W |
| (see Note 3): RGY package | 37°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

| | | SN54ABT574 | | SN74ABT574A | | UNIT |
|---------------------|------------------------------------|-----------------|----------|-------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | –24 | | –32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 5 | 5 | ns/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ABT574, SN74ABT574A

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A = 25^\circ\text{C}$ | | | SN54ABT574 | | SN74ABT574A | | UNIT |
|-----------------------------|--|--------------------------|------|----------------|------------|----------------|-------------|----------------|---------------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$ | | | 2.5 | | 2.5 | | 2.5 | V |
| | $V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$ | | | 3 | | 3 | | 3 | |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -24\text{ mA}$ | | | 2 | | | 2 | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | | | | 0.55 | | 0.55 | V |
| | | $I_{OL} = 64\text{ mA}$ | | | | 0.55* | | 0.55 | |
| V_{hys} | | | | 100 | | | | | mV |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND | | | ± 1 | | ± 1 | | ± 1 | μA |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$ | | | 10^\ddagger | | 10^\ddagger | | 10^\ddagger | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$ | | | -10^\ddagger | | -10^\ddagger | | -10^\ddagger | μA |
| I_{off} | $V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$ | | | ± 100 | | ± 500 | | ± 100 | μA |
| I_{CEX} | $V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$ | Outputs high | | | | 50 | | 50 | μA |
| I_O^{\S} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$ | | | -50 | -100 | -180 | -50 | -180 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | 1 | 250 | | 250 | 250 | μA |
| | | Outputs low | | 24 | 30 | | 30 | 30 | mA |
| | | Outputs disabled | | 0.5 | 250 | | 250 | 250 | μA |
| $\Delta I_{CC}^{\parallel}$ | $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND | | | | | 1.5 | | 1.5 | mA |
| C_i | $V_I = 2.5\text{ V}$ or 0.5 V | | | 3.5 | | | | | pF |
| C_o | $V_O = 2.5\text{ V}$ or 0.5 V | | | 6.5 | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ This data-sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54ABT574 | | | | UNIT |
|-------------|---------------------------------|---|-----|-----|-----|------|
| | | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | MIN | MAX | |
| | | MIN | MAX | | | |
| f_{clock} | Clock frequency | | 150 | | 150 | MHz |
| t_w | Pulse duration, CLK high or low | | 3.3 | | 3.3 | ns |
| t_{su} | Setup time, data before CLK↑ | High | 1.5 | | 1.5 | ns |
| | | Low | 2 | | 2 | |
| t_h | Hold time, data after CLK↑ | High or low | 2 | | 2 | ns |



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN74ABT574A | | | | UNIT | |
|--------------------|---------------------------------|---|------|-----|-----|------|-----|
| | | V _{CC} = 5 V, T _A = 25°C | | | MIN | | MAX |
| | | MIN | MAX | | | | |
| f _{clock} | Clock frequency | 150 | | 150 | MHz | | |
| t _w | Pulse duration, CLK high or low | 3.3 | | 3.3 | ns | | |
| t _{su} | Setup time, data before CLK↑ | High | 1 | | ns | | |
| | | Low | 1.5 | | | | |
| t _h | Hold time, data after CLK↑ | High or low | 1.8† | | ns | | |

† This data-sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT574 | | | | | UNIT |
|------------------|-----------------|----------------|---|-----|-----|-----|-----|------|
| | | | V _{CC} = 5 V, T _A = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| f _{max} | | | 150 | 200 | | 150 | MHz | |
| t _{PLH} | CLK | Q | 2.2 | 3.9 | 6.2 | 2.2 | 7 | ns |
| t _{PHL} | | | 3 | 4.8 | 7 | 3 | 7.4 | |
| t _{PZH} | OE | Q | 1 | 3.3 | 5 | 1 | 5.8 | ns |
| t _{PZL} | | | 2.5 | 4.7 | 5.9 | 2.5 | 7.2 | |
| t _{PHZ} | OE | Q | 2.4 | 4.9 | 6.2 | 2.4 | 7.2 | ns |
| t _{PLZ} | | | 2 | 4 | 5.8 | 2 | 6.9 | |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

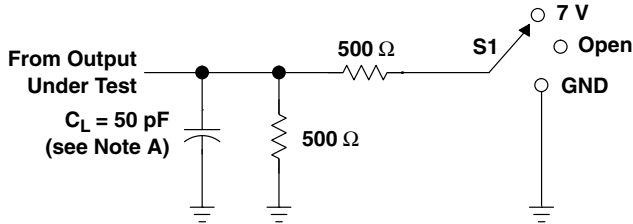
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT574A | | | | | UNIT |
|------------------|-----------------|----------------|---|-----|-----|------|-----|------|
| | | | V _{CC} = 5 V, T _A = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| f _{max} | | | 150 | 200 | | 150 | MHz | |
| t _{PLH} | CLK | Q | 2.2 | 3.9 | 6.2 | 2.2 | 6.8 | ns |
| t _{PHL} | | | 3 | 4.8 | 6.6 | 3 | 7.1 | |
| t _{PZH} | OE | Q | 1 | 3.3 | 4.3 | 1 | 5.1 | ns |
| t _{PZL} | | | 2.1† | 4.7 | 5.9 | 2.1† | 6.7 | |
| t _{PHZ} | OE | Q | 2.4 | 4.9 | 6.2 | 2.4 | 7 | ns |
| t _{PLZ} | | | 2 | 4 | 5.8 | 2 | 6.5 | |

† This data-sheet limit may vary among suppliers.

SN54ABT574, SN74ABT574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

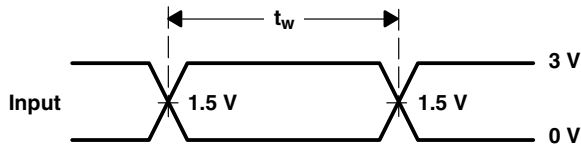
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PARAMETER MEASUREMENT INFORMATION

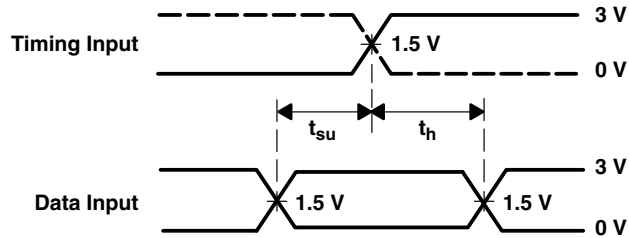


LOAD CIRCUIT

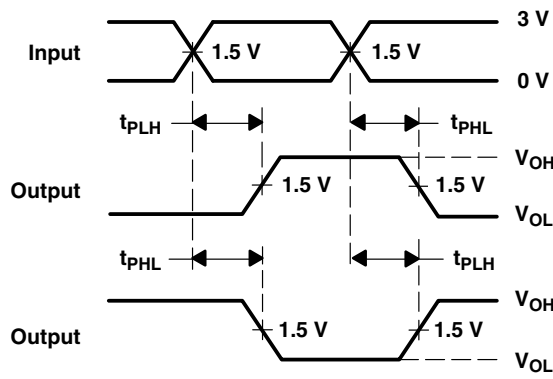
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



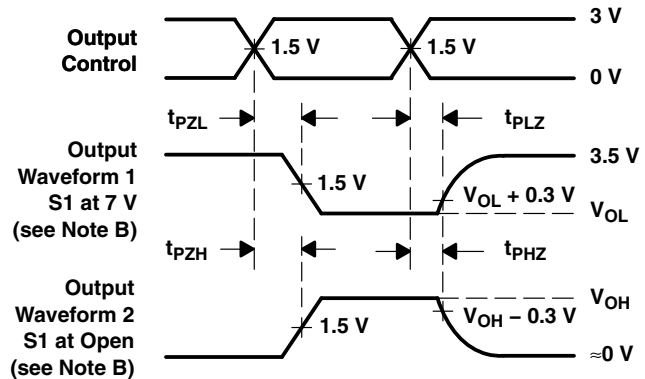
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|-------------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9322001Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9322001QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| 5962-9322001QSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |
| SN74ABT574ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74ABT574ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574AGQNR | NRND | BGA MICROST R JUNIOR | GQN | 20 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| SN74ABT574AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT574ANE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT574ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574ANSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574APWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI |
| SN74ABT574APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT574APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|----------------------------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74ABT574ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN74ABT574ARGYRG4 | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN74ABT574AZQNR | ACTIVE | BGA MI CROSTA R JUNI OR | ZQN | 20 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SNJ54ABT574FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ABT574J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54ABT574W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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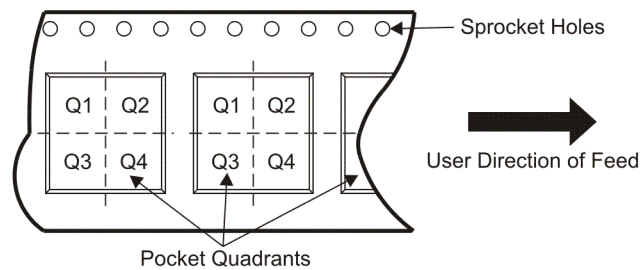
OTHER QUALIFIED VERSIONS OF SN54ABT574 :

- Catalog: [SN74ABT574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT574ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT574ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ABT574AGQNR | BGA MICROSTAR JUNIOR | GQN | 20 | 1000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| SN74ABT574ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ABT574APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74ABT574ARGYR | VQFN | RGY | 20 | 3000 | 180.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74ABT574AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT574ADBR | SSOP | DB | 20 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74ABT574ADWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT574AGQNR | BGA MICROSTAR JUNIOR | GQN | 20 | 1000 | 346.0 | 346.0 | 29.0 |
| SN74ABT574ANSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT574APWR | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74ABT574ARGYR | VQFN | RGY | 20 | 3000 | 190.5 | 212.7 | 31.8 |
| SN74ABT574AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 346.0 | 346.0 | 29.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

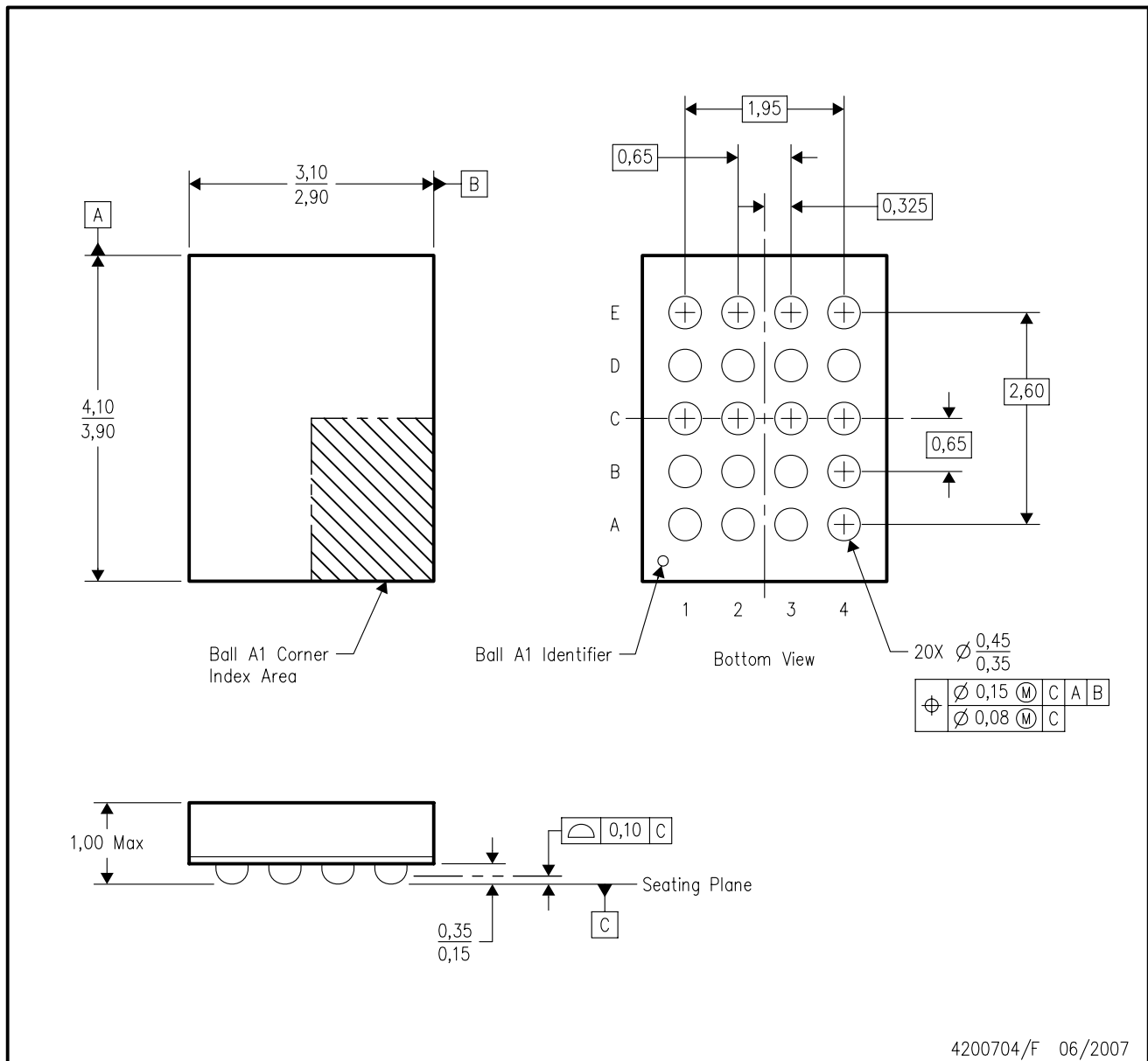


4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY

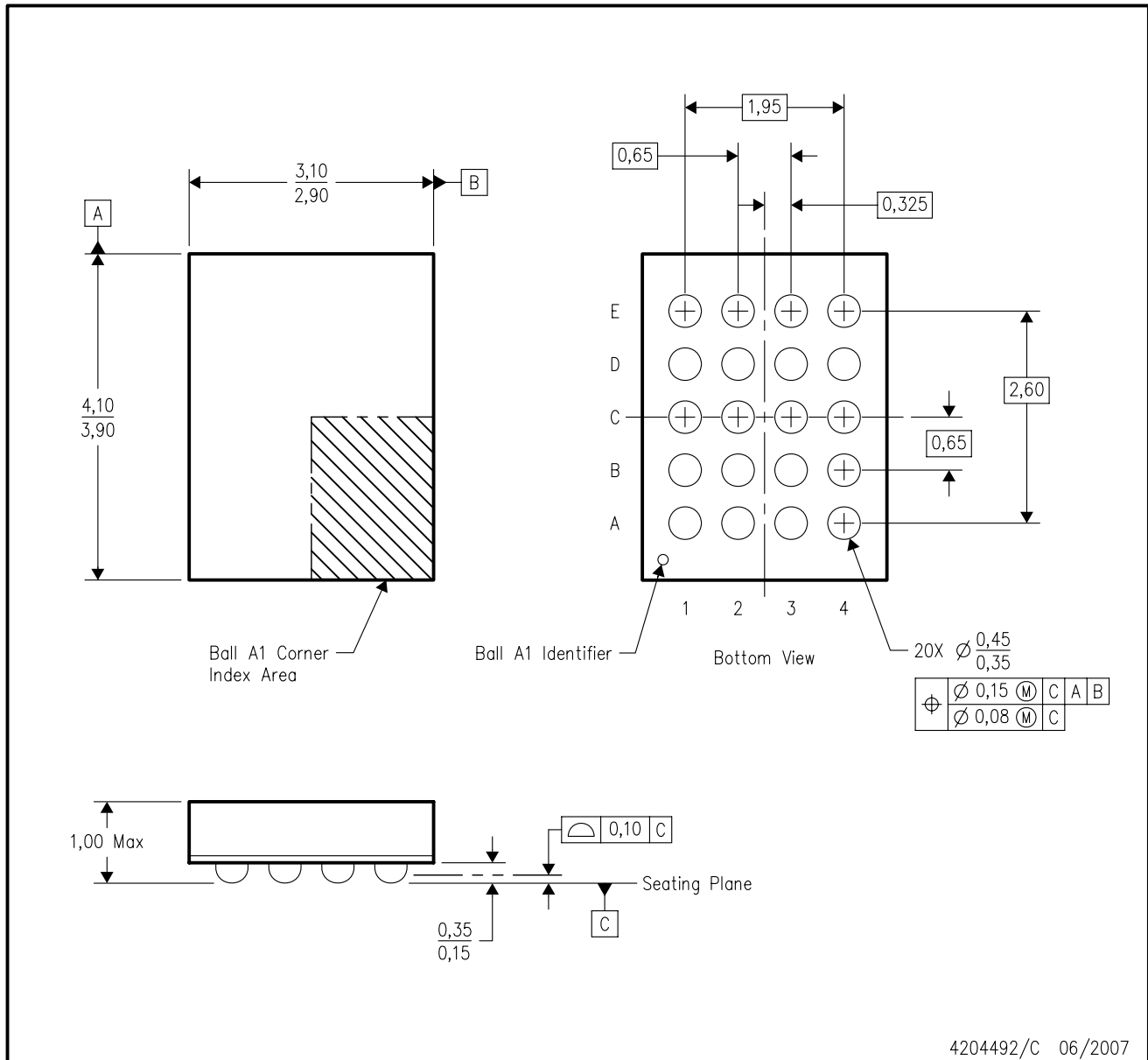


4200704/F 06/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BC-2.
 - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BC-2.
 - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

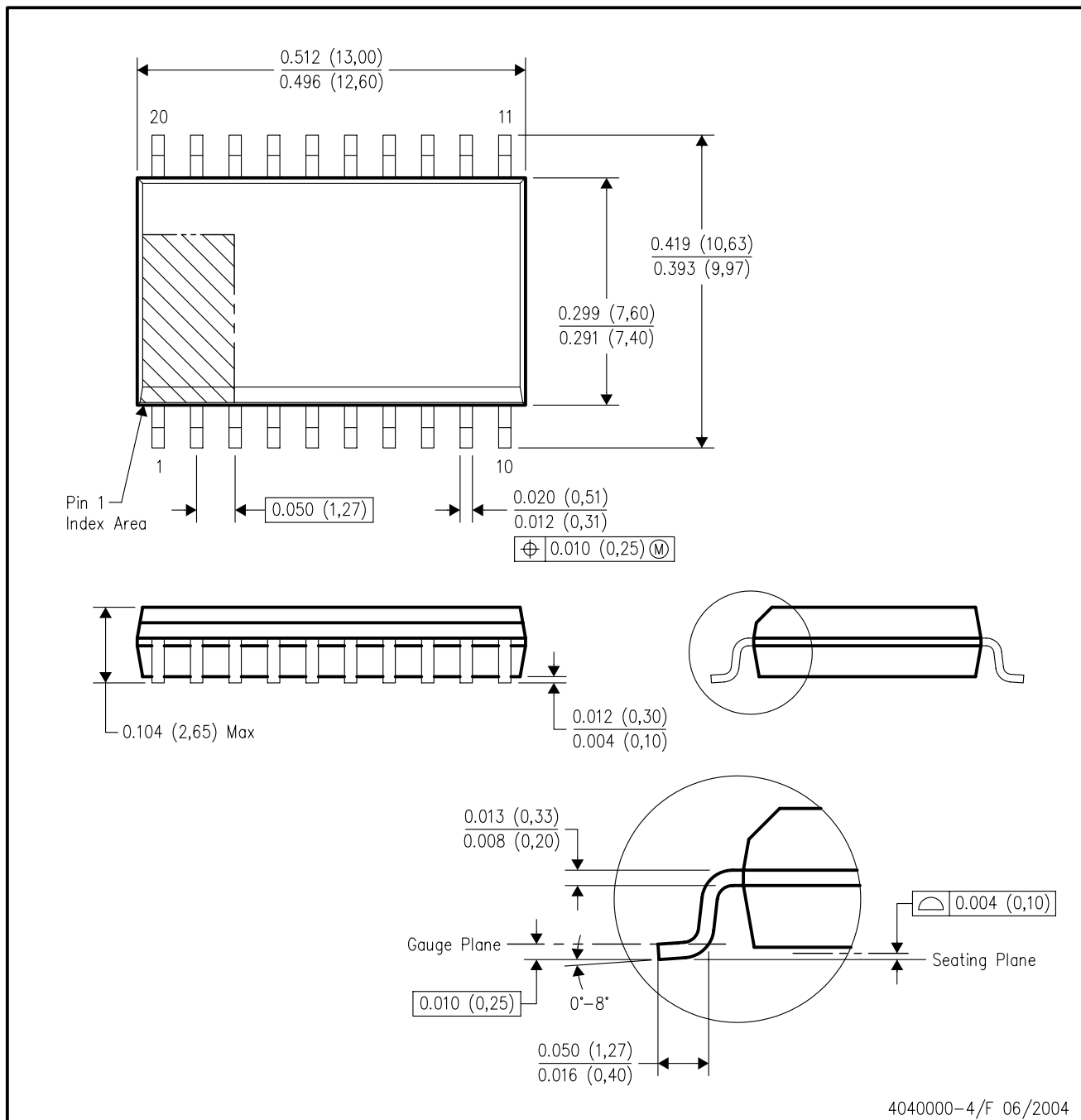
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

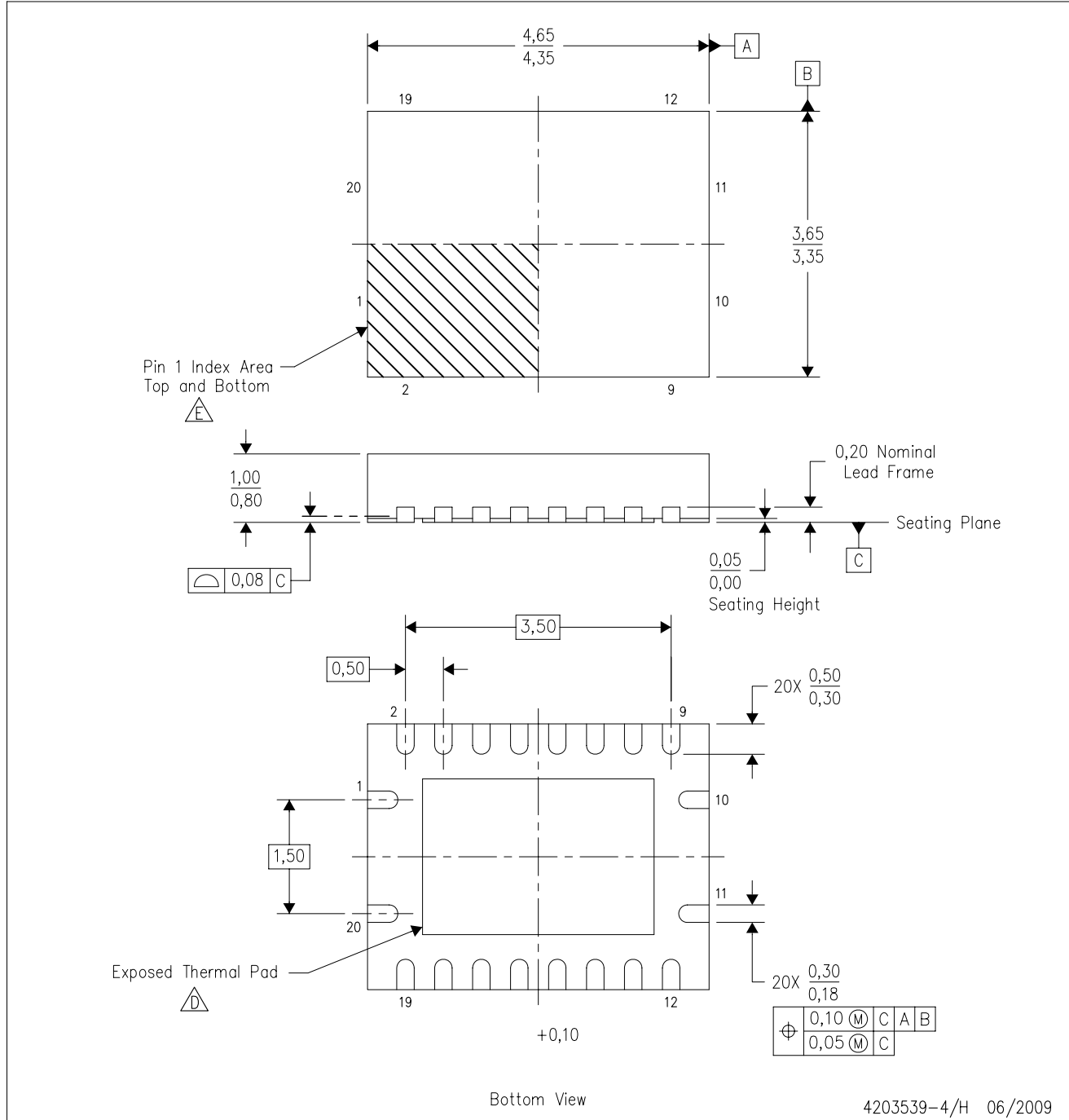
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BC.

THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

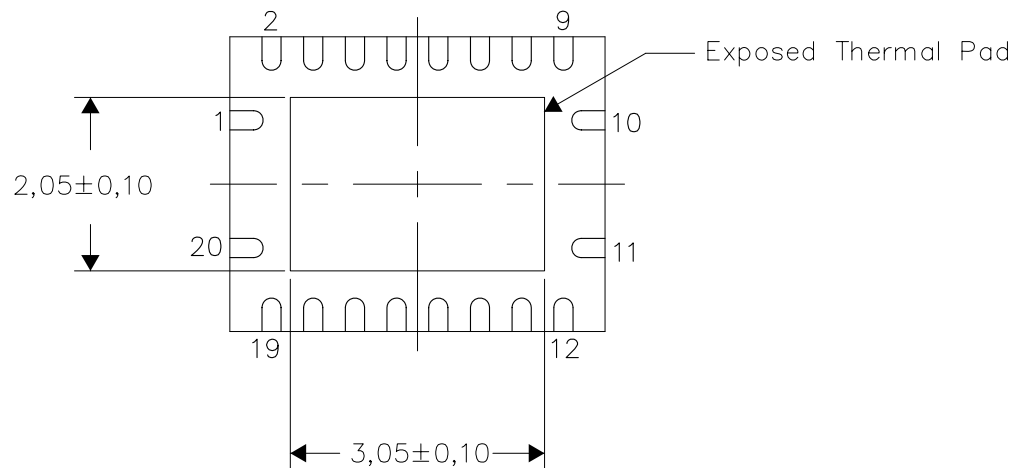
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

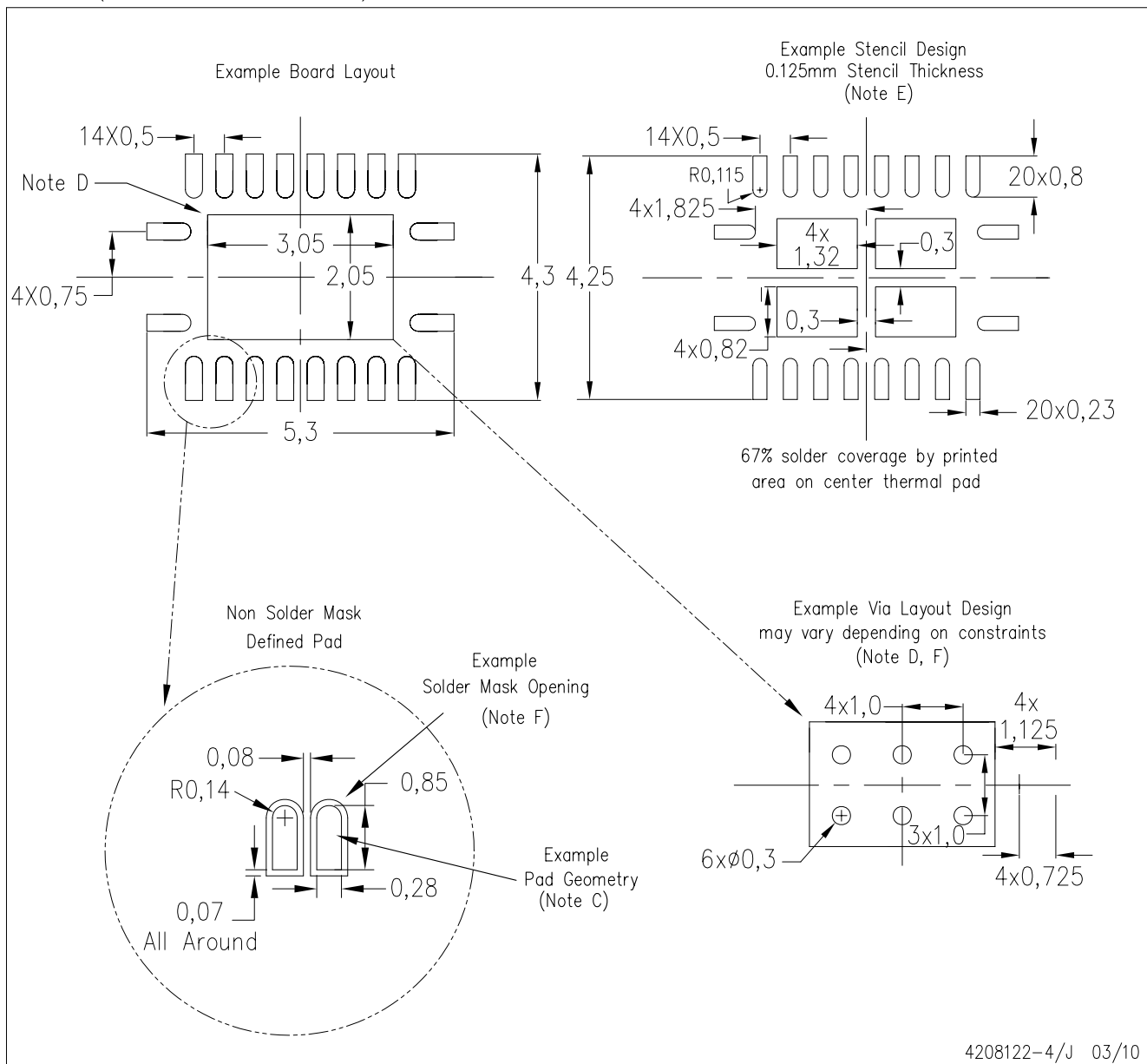
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206353-4/J 03/10

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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