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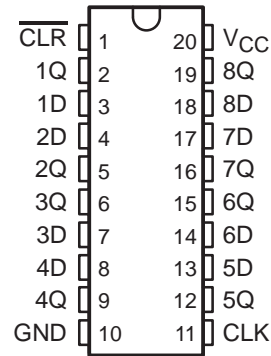
Jameco Part Number 1998749

SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

SCBS185B – FEBRUARY 1991 – REVISED JANUARY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

SN54ABT273 . . . J OR W PACKAGE
SN74ABT273 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



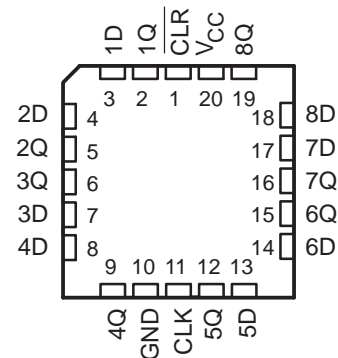
description

The 'ABT273 are 8-bit positive-edge-triggered D-type flip-flops with a direct clear (CLR) input. They are particularly suitable for implementing buffer and storage registers, shift registers, and pattern generators.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D input signal has no effect at the output.

The SN54ABT273 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT273 is characterized for operation from -40°C to 85°C .

SN54ABT273 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|--------|--------|---|--------|
| CLR | CLK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | H or L | X | Q_0 |



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EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

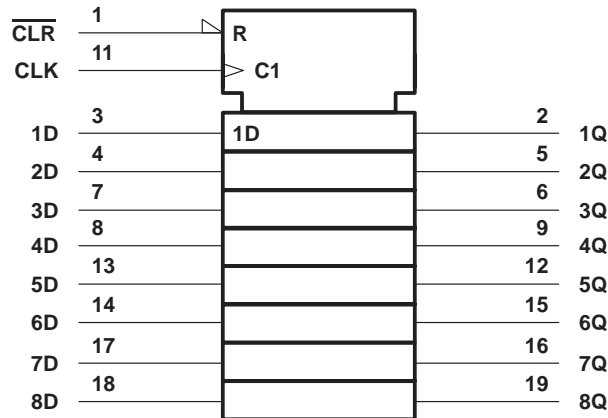
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SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

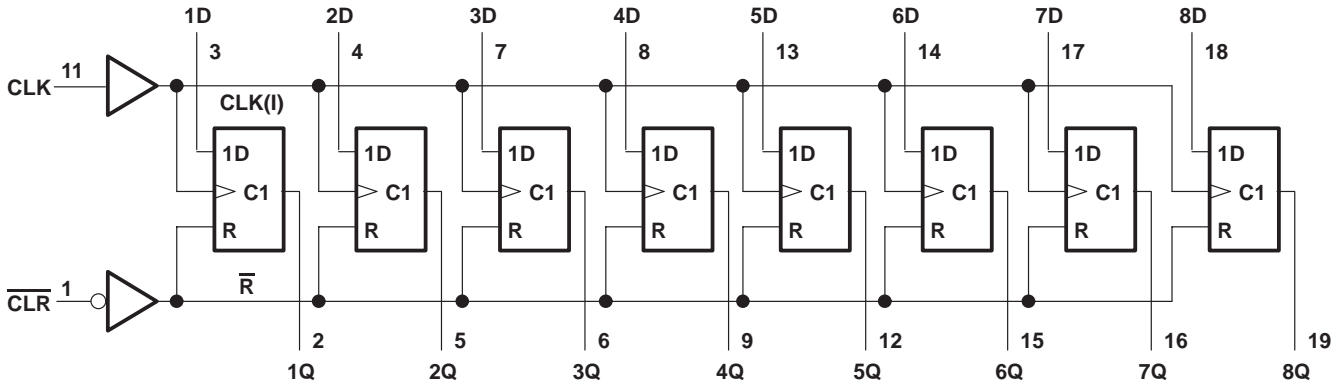
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT273 | 96 mA |
| SN74ABT273 | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DB package | 115°C/W |
| DW package | 97°C/W |
| N package | 67°C/W |
| PW package | 128°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



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SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

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recommended operating conditions (see Note 3)

| | | SN54ABT273 | | SN74ABT273 | | UNIT |
|---------------------|------------------------------------|------------|----------|------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -24 | | -32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A = 25^\circ\text{C}$ | | | SN54ABT273 | | SN74ABT273 | | UNIT | |
|---------------------------|--|--------------------------|------|-----------|------------|---------|------------|-----------|---------------|---------------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | | -1.2 | V | |
| V_{OH} | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$ | | 2.5 | | 2.5 | | 2.5 | | V | |
| | $V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$ | | 3 | | 3 | | 3 | | | |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -24\text{ mA}$ | | 2 | | 2 | | | | |
| $I_{OH} = -32\text{ mA}$ | | | 2* | | | | 2 | | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | | 0.55 | | 0.55 | | | V | |
| | | $I_{OL} = 64\text{ mA}$ | | 0.55* | | | 0.55 | | | |
| V_{hys} | | | 100 | | | | | | mV | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND | | | ± 1 | | ± 1 | | ± 1 | μA | |
| I_{off} | $V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$ | | | ± 100 | | | | ± 100 | μA | |
| I_{CEX} | $V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$ | | | 50 | | 50 | | 50 | μA | |
| I_{O}^\ddagger | $V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$ | | | -50 | -100 | -200§ | | -50 | -200§ | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | 1 | 400§ | | 400§ | | 400§ | μA |
| | | Outputs low | | 24 | 30 | | 30 | | 30 | mA |
| ΔI_{CC}^\parallel | $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND | | | | 1.5 | | 1.5 | | 1.5 | mA |
| C_i | $V_I = 2.5\text{ V}$ or 0.5 V | | | 7 | | | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This data sheet limit may vary among suppliers.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT273, SN74ABT273 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | V _{CC} = 5 V, T _A = 25°C | | SN54ABT273 | | SN74ABT273 | | UNIT |
|--------------------|------------------------|---|------|------------|------|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 0 | 150 | 0 | 150 | 0 | 150 | MHz |
| t _w | Pulse duration | CLK high or low | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | ns |
| | | $\overline{\text{CLR}}$ low | 3.3 | 3.3 | 3.3 | 3.3 | | |
| t _{su} | Setup time before CLK↑ | Data high | 2 | 2 | 2 | 2 | ns | |
| | | Data low | 2.5 | 2.5 | 2.5 | 2.5 | | |
| | | $\overline{\text{CLR}}$ high | 2 | 2 | 2 | 2 | | |
| t _h | Hold time after CLK↑ | Data high or low | 1.2† | 1.4† | 1.2† | 1.2† | ns | |

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 5 V, T _A = 25°C | | SN54ABT273 | | UNIT |
|------------------|-------------------------|----------------|---|------|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f _{max} | | | 150 | | 150 | | MHz |
| t _{PLH} | CLK | Q | 2.5 | 6 | 2.5 | 7 | ns |
| t _{PHL} | | | 3.3 | 6.8 | 3.3 | 7.5 | |
| t _{PHL} | $\overline{\text{CLR}}$ | Q | 2.5 | 7.5† | 2.5 | 8.2 | ns |

† This data sheet limit may vary among suppliers.

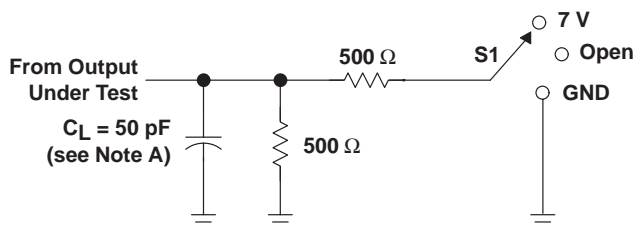
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 5 V, T _A = 25°C | | SN74ABT273 | | UNIT |
|------------------|-------------------------|----------------|---|------|------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| f _{max} | | | 150 | | 150 | | MHz |
| t _{PLH} | CLK | Q | 2.5 | 6 | 2.5 | 6.5 | ns |
| t _{PHL} | | | 3.3 | 6.8 | 3.3 | 7.3 | |
| t _{PHL} | $\overline{\text{CLR}}$ | Q | 2.5 | 6.7† | 2.5 | 7.4† | ns |

† This data sheet limit may vary among suppliers.

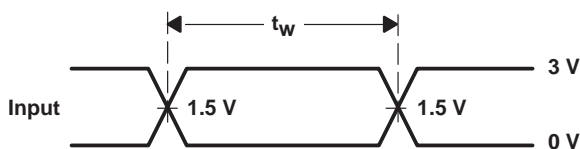


PARAMETER MEASUREMENT INFORMATION

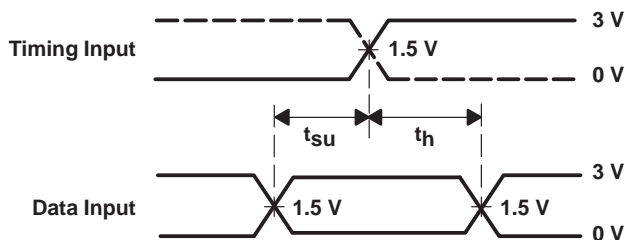


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |

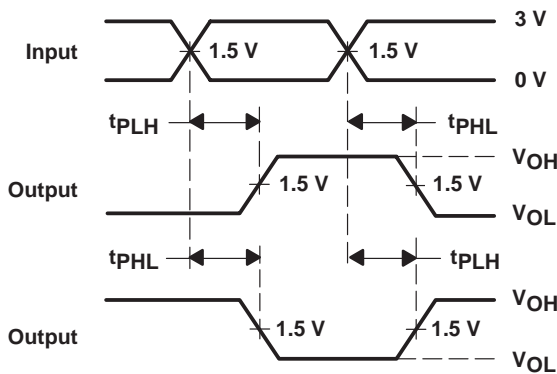
LOAD CIRCUIT



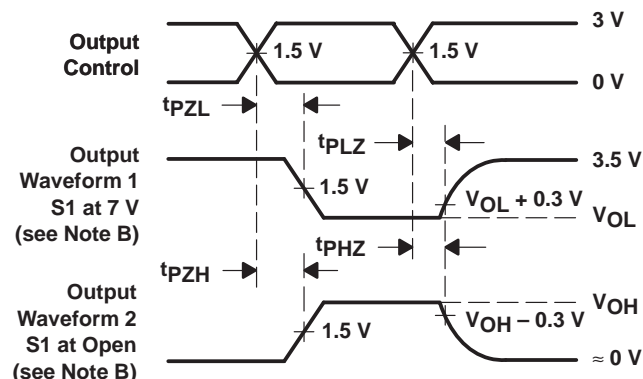
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9321701Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9321701QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-9321701QSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |
| SN74ABT273DBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI |
| SN74ABT273DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT273NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74ABT273NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273PWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273PWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI |
| SN74ABT273PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT273PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54ABT273FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54ABT273J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54ABT273W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

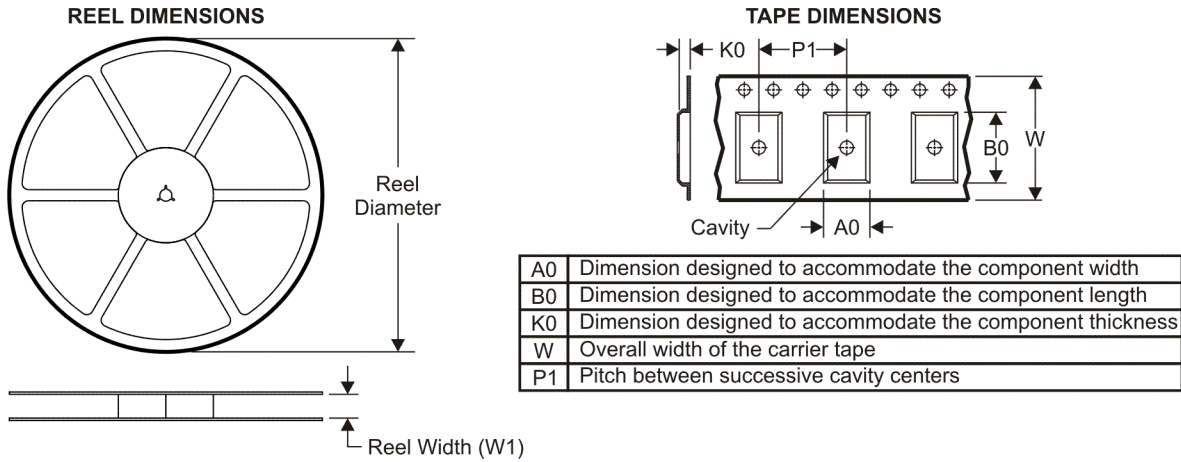
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT273DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT273DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ABT273NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ABT273PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT273DBR | SSOP | DB | 20 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74ABT273DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT273NSR | SO | NS | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74ABT273PWR | TSSOP | PW | 20 | 2000 | 346.0 | 346.0 | 33.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

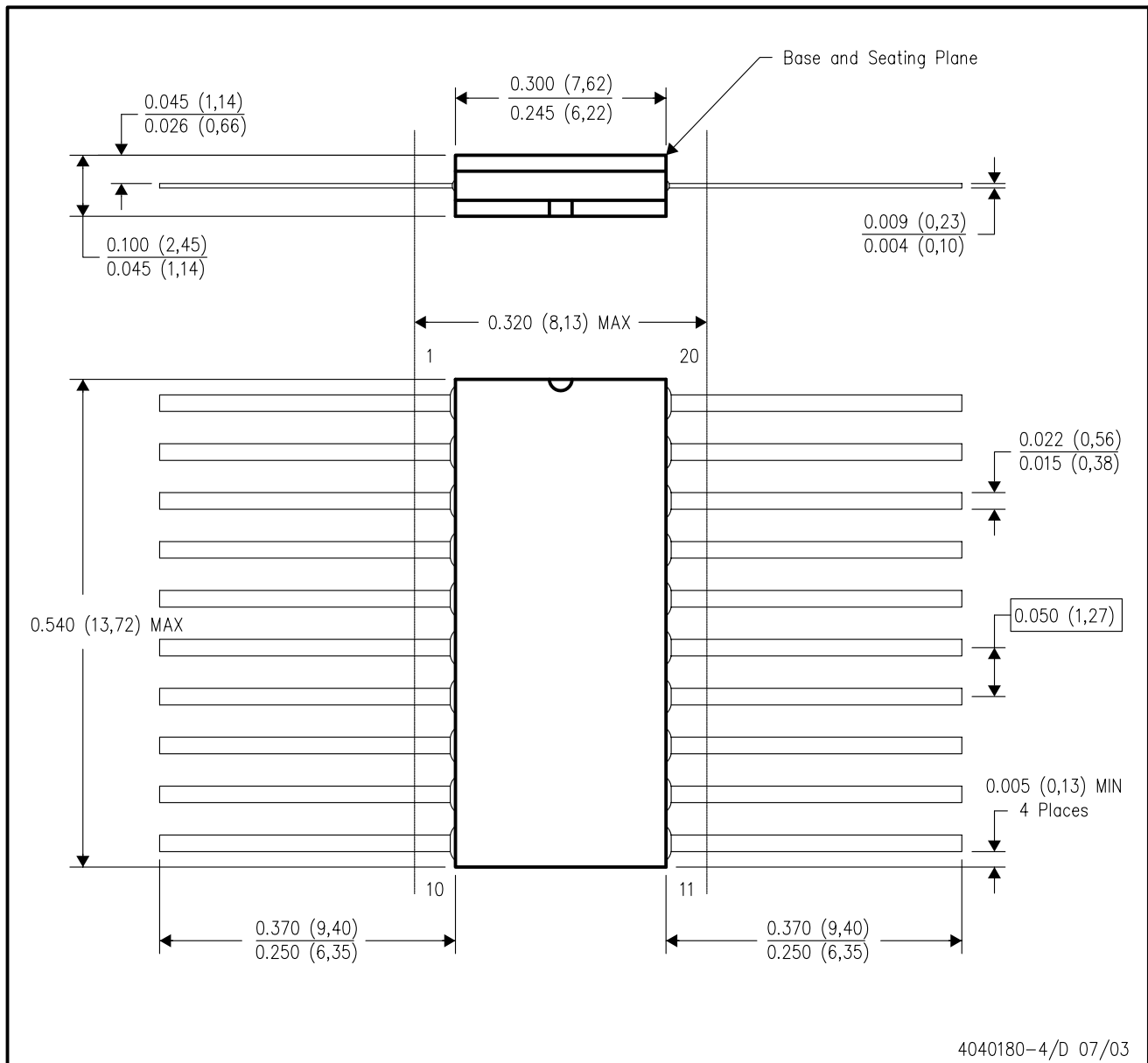
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

W (R-GDFP-F20)

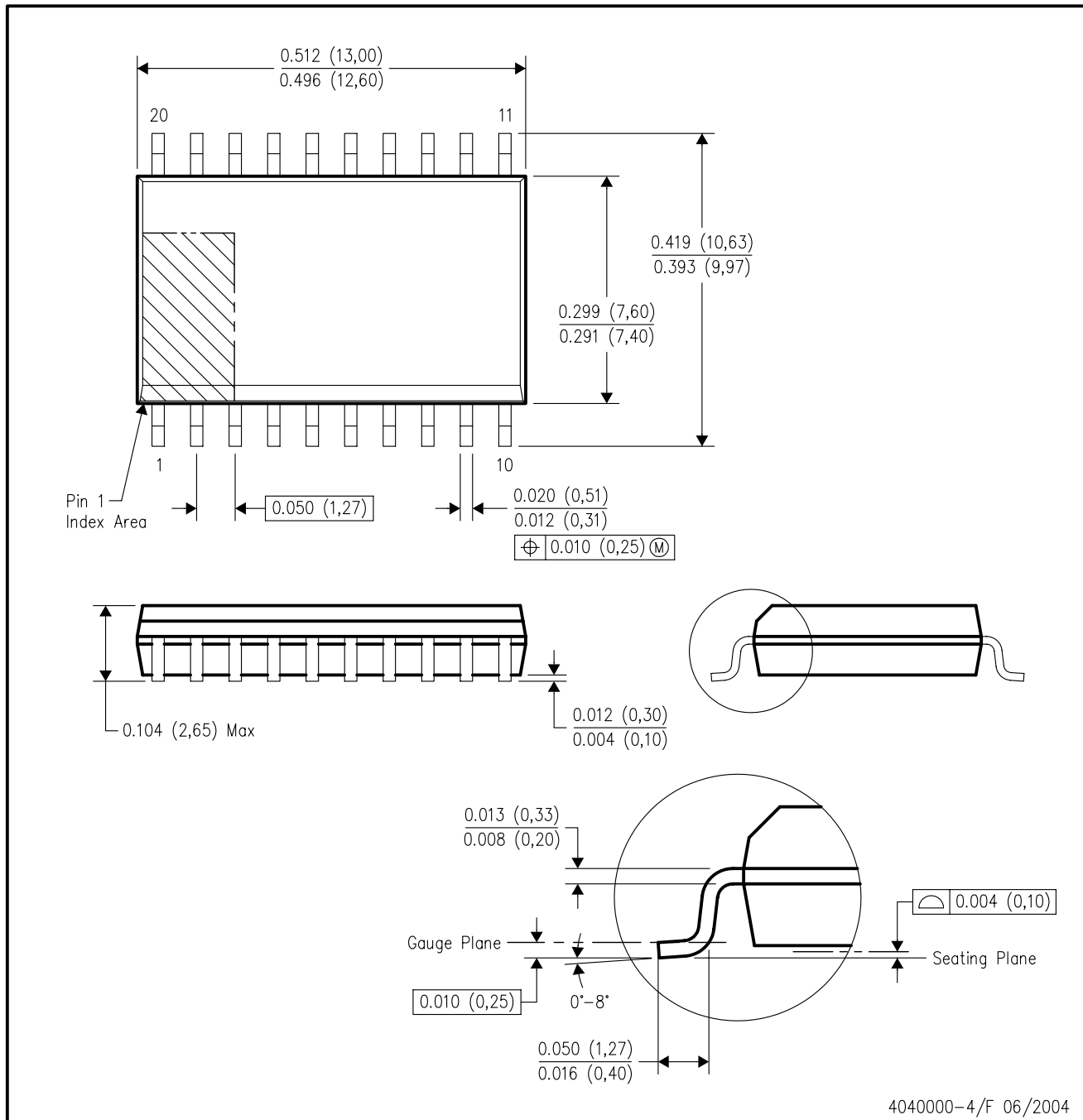
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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