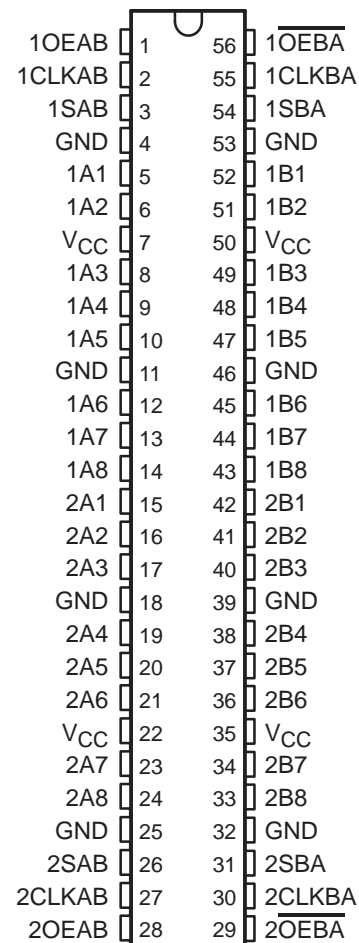


# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS215B – FEBRUARY 1991 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16652 . . . WD PACKAGE  
SN74ABT16652 . . . DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16652 are 16-bit bus transceivers that consist of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and  $\overline{\text{OEBA}}$ ) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16652.

Data on the A- or B-data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control inputs. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{\text{OEBA}}$ . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## description (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

The SN54ABT16652 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT16652 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or  $\overline{OEBA}$ . Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

SN54ABT16652, SN74ABT16652  
 16-BIT BUS TRANSCEIVERS AND REGISTERS  
 WITH 3-STATE OUTPUTS

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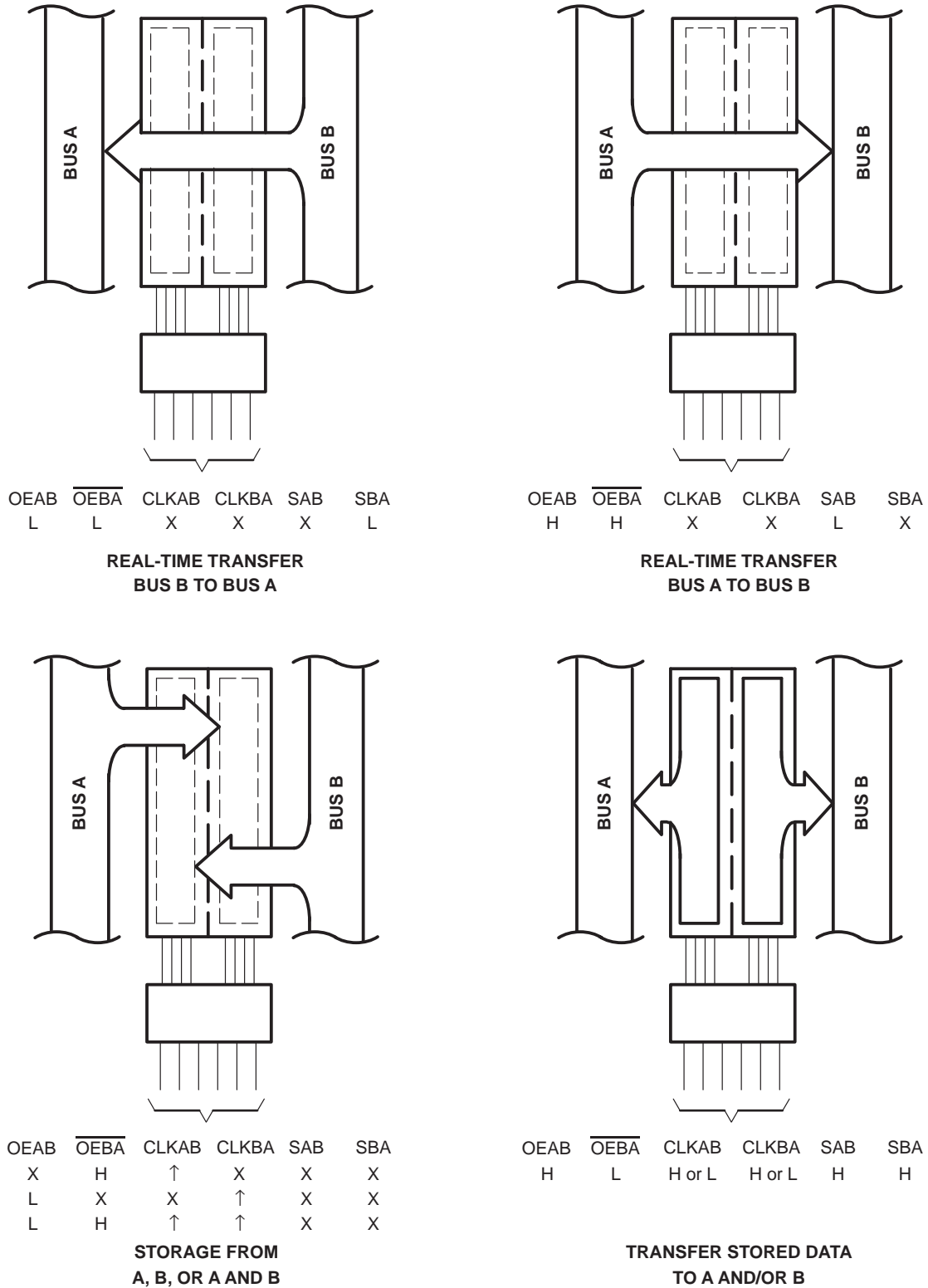
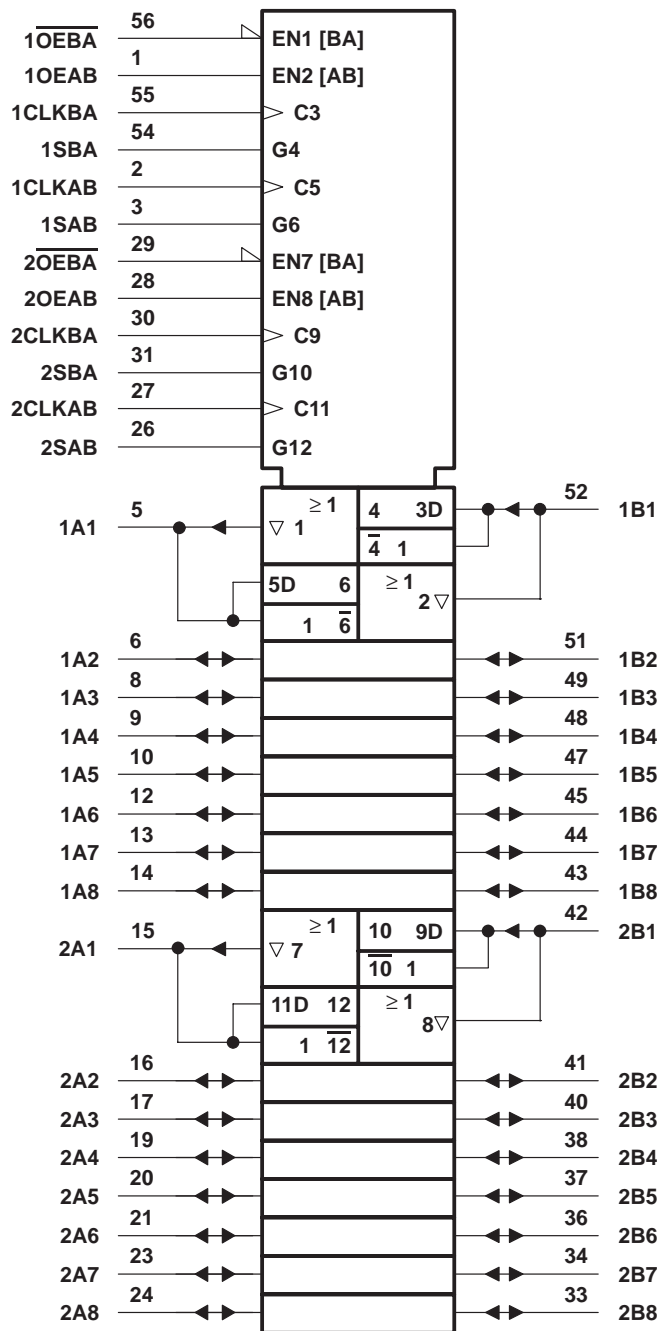


Figure 1. Bus-Management Functions

# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## logic symbol†



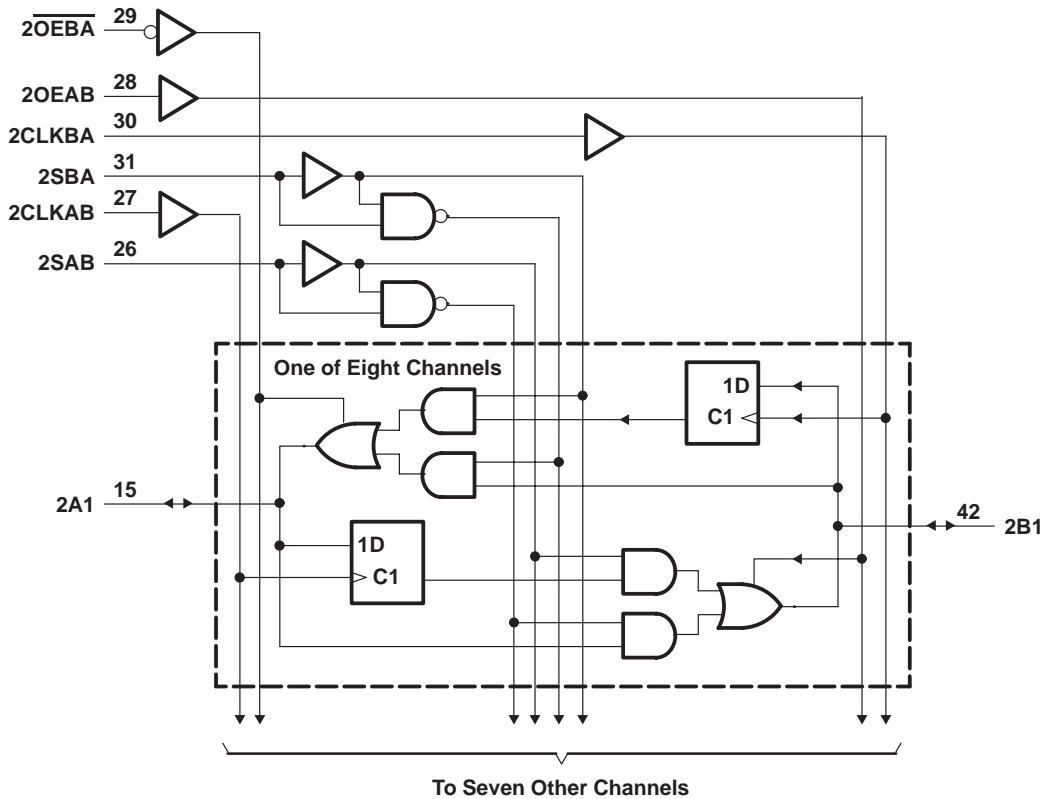
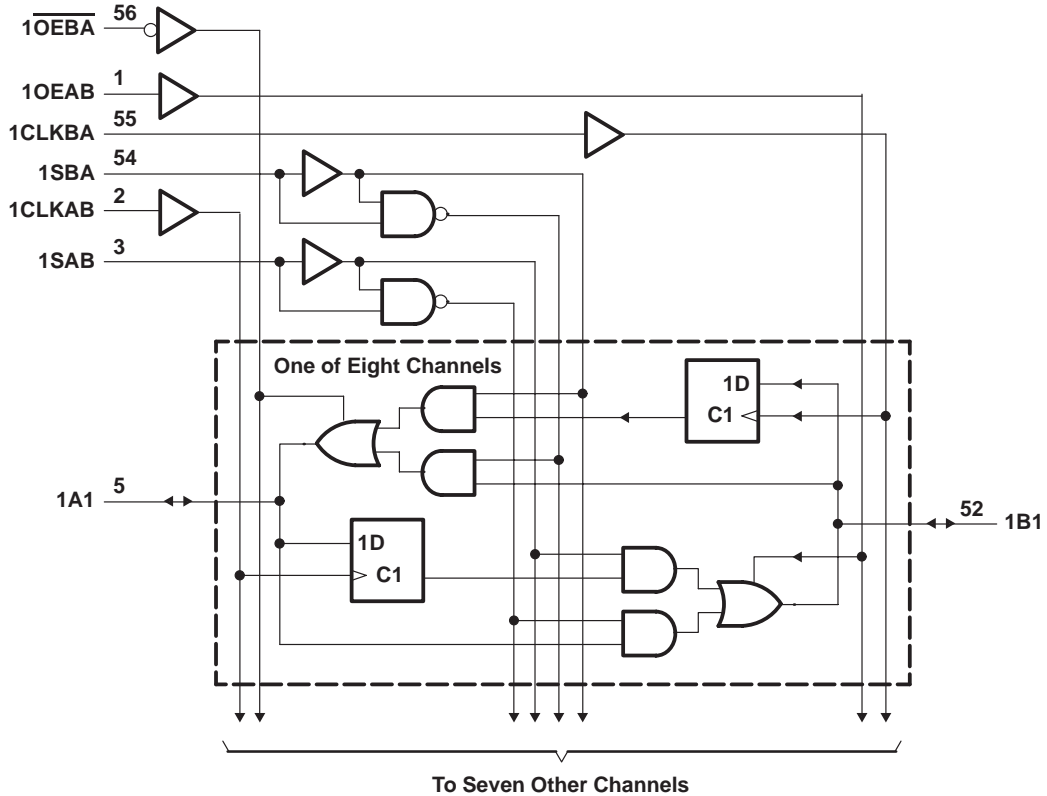
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16652 .....	96 mA
SN74ABT16652 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16652		SN74ABT16652		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage	0.8		0.8		V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	-24		-32		mA
$I_{OL}$	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16652		SN74ABT16652		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5		2.5		2.5	V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		3		3		
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -32 mA			2 2*		2		2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 64 mA					0.55		0.55	V	
						0.55*		0.55		
V <sub>hys</sub>				100					mV	
I <sub>I</sub>	Control inputs A or B ports	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND					±1		±1	µA
							±20		±20	
I <sub>OZH</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			10		10		10	µA	
I <sub>OZL</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-10		-10		-10	µA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	µA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V Outputs high			50		50		50	µA	
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V			-50 -100 -180		-50 -180		-50 -180	mA	
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high			2		2	mA	
			Outputs low			32		32		
			Outputs disabled			2		2		
ΔI <sub>CC</sub> ¶	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled			50		50	µA	
			Outputs disabled			50		50		
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			50		50	50		
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			4				pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			8				pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABT16652, SN74ABT16652**  
**16-BIT BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

	SN54ABT16652				UNIT
	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	
	MIN	MAX			
f <sub>clock</sub> Clock frequency	0	125	0	125	MHz
t <sub>w</sub> Pulse duration, CLK high or low	4.3		4.3		ns
t <sub>su</sub> Setup time, A or B before CLKAB↑ or CLKBA↑	3.5		4		ns
t <sub>h</sub> Hold time, A or B after CLKAB↑ or CLKBA↑	0.5		0.5		ns

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

	SN74ABT16652				UNIT
	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	
	MIN	MAX			
f <sub>clock</sub> Clock frequency	0	125	0	125	MHz
t <sub>w</sub> Pulse duration, CLK high or low	4.3		4.3		ns
t <sub>su</sub> Setup time, A or B before CLKAB↑ or CLKBA↑	3		3		ns
t <sub>h</sub> Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		ns



# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16652					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
$f_{max}$			125			125	MHz	
$t_{PLH}$	CLK	B or A	1.5	3.1	4	1	5	ns
$t_{PHL}$			1.5	3.2	4.1	1	5	
$t_{PLH}$	A or B	B or A	1	2.3	3.2	0.6	4	ns
$t_{PHL}$			1	3	4.1	0.6	4.9	
$t_{PLH}$	SAB or SBA†	B or A	1	2.9	4.3	0.6	5.3	ns
$t_{PHL}$			1	3.1	4.6	0.6	5.3	
$t_{PZH}$	$\overline{OEBA}$	A	1	2.8	4.1	0.6	5.2	ns
$t_{PZL}$			1.5	3.1	4.4	1	5.4	
$t_{PHZ}$	$\overline{OEBA}$	A	1.5	3.4	4.7	0.8	5.3	ns
$t_{PLZ}$			1.5	2.7	4	1	5.3	
$t_{PZH}$	OEAB	B	1	2.6	3.6	0.8	4.7	ns
$t_{PZL}$			1.5	2.8	4.5	1	5	
$t_{PHZ}$	OEAB	B	2	4.2	5.9	1	6.4	ns
$t_{PLZ}$			1.5	3.4	4.9	1	5.9	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16652					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
$f_{max}$			125			125	MHz	
$t_{PLH}$	CLK	B or A	1.5	3.1	4	1.5	4.9	ns
$t_{PHL}$			1.5	3.2	4.1	1.5	4.7	
$t_{PLH}$	A or B	B or A	1	2.3	3.2	1	3.9	ns
$t_{PHL}$			1	3	4.1	1	4.6	
$t_{PLH}$	SAB or SBA†	B or A	1	2.9	4.3	1	5	ns
$t_{PHL}$			1	3.1	4.3	1	5	
$t_{PZH}$	$\overline{OEBA}$	A	1	2.8	4.1	1	5	ns
$t_{PZL}$			1.5	3.1	4.4	1.5	5.3	
$t_{PHZ}$	$\overline{OEBA}$	A	1.5	3.4	4.4	1.5	4.9	ns
$t_{PLZ}$			1.5	2.7	3.6	1.5	4	
$t_{PZH}$	OEAB	B	1	2.6	3.6	1	4.2	ns
$t_{PZL}$			1.5	2.8	3.9	1.5	4.6	
$t_{PHZ}$	OEAB	B	2	4.2	5.5	2	5.9	ns
$t_{PLZ}$			1.5	3.4	4.5	1.5	5.2	

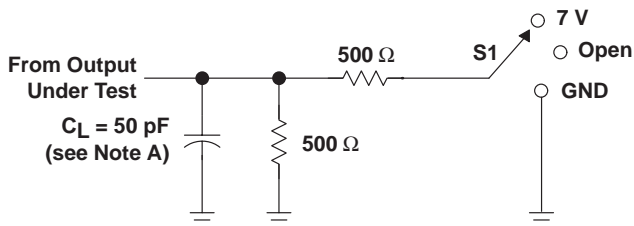
† These parameters are measured with the internal output state of the storage register opposite that of the bus input.



# SN54ABT16652, SN74ABT16652 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

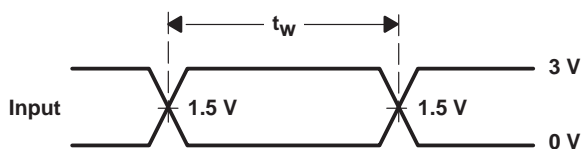
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## PARAMETER MEASUREMENT INFORMATION

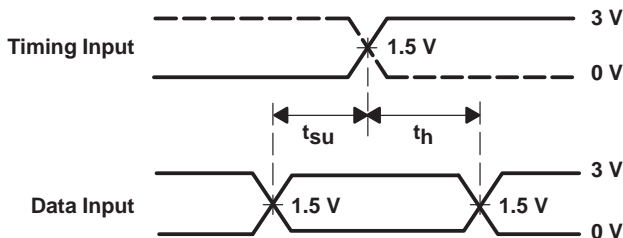


LOAD CIRCUIT

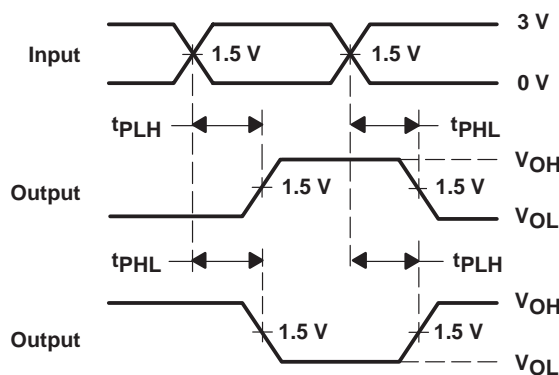
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



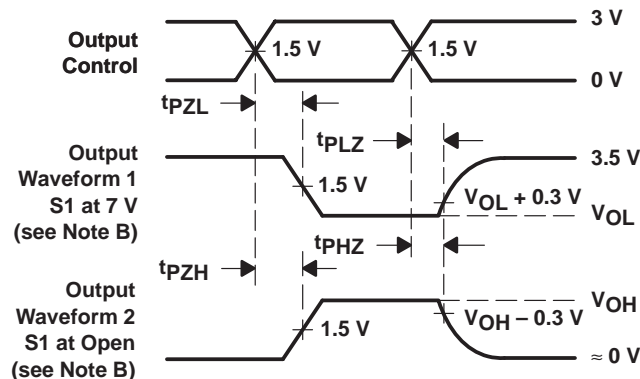
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9584101QXA	LIFEBUY	CFP	WD	56	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9584101QX A SNJ54ABT16652W D	
SN74ABT16652DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16652	<b>Samples</b>
SN74ABT16652DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16652	<b>Samples</b>
SNJ54ABT16652WD	LIFEBUY	CFP	WD	56	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9584101QX A SNJ54ABT16652W D	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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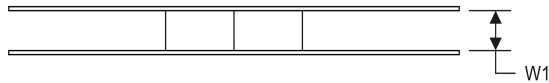
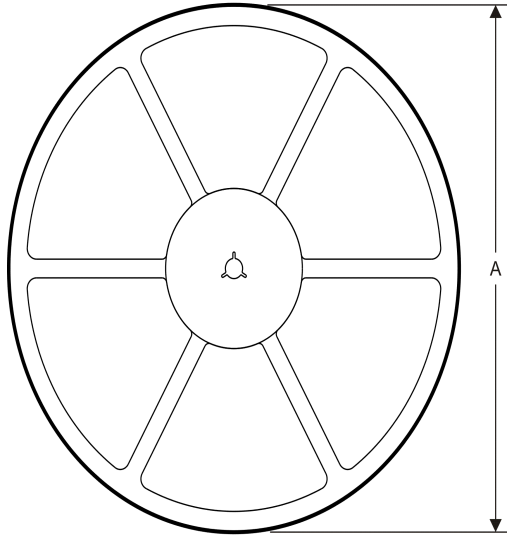
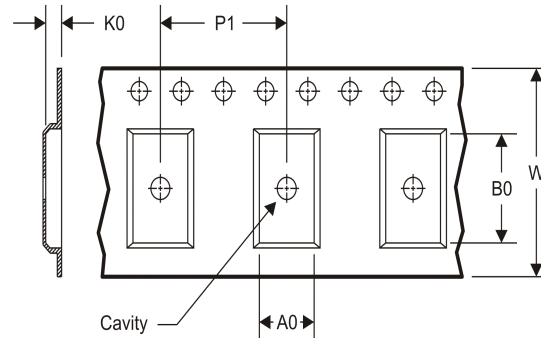
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ABT16652, SN74ABT16652 :**

- Catalog: [SN74ABT16652](#)
- Military: [SN54ABT16652](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16652DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16652DLR	SSOP	DL	56	1000	367.0	367.0	55.0

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



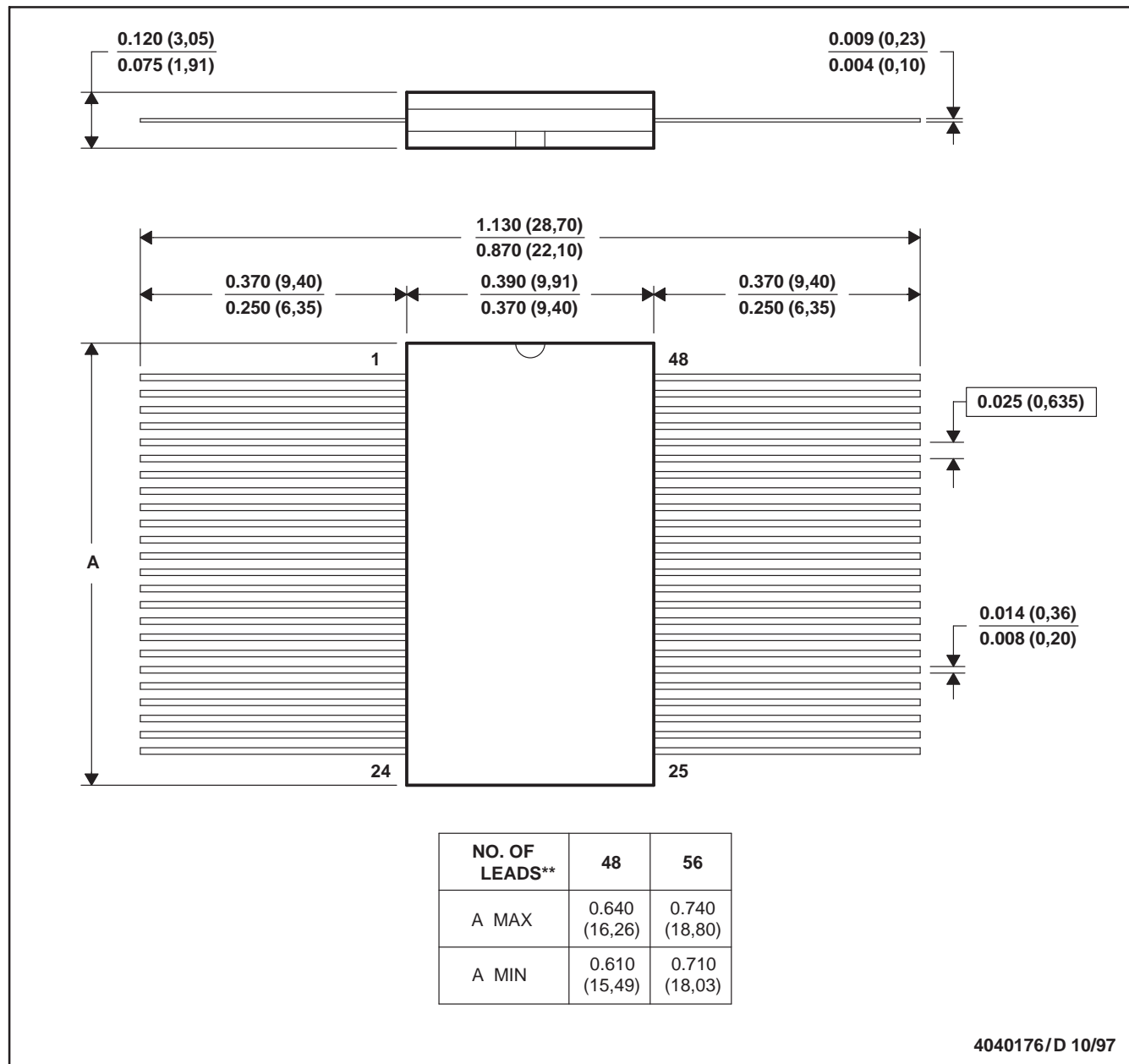
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

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