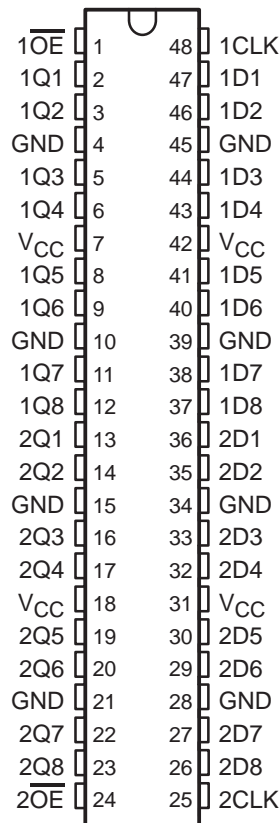


# SN54ABT16374A, SN74ABT16374A 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS205C – MARCH 1993 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16374A . . . WD PACKAGE  
SN74ABT16374A . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16374A are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16374A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16374A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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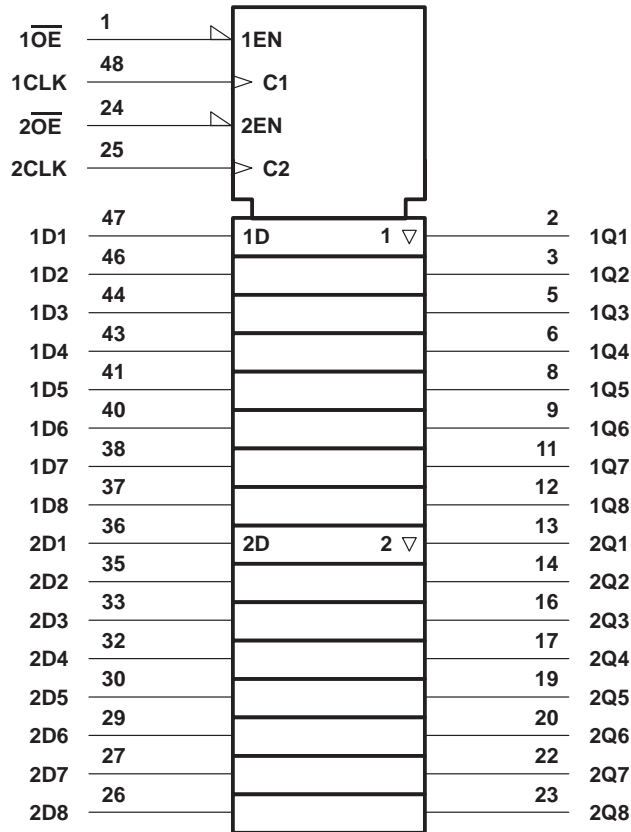
# SN54ABT16374A, SN74ABT16374A 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each flip-flop)

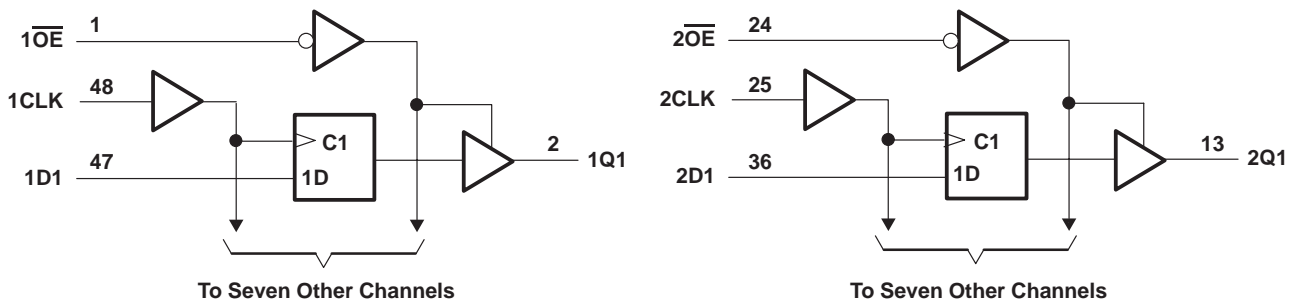
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54ABT16374A, SN74ABT16374A 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16374A .....	96 mA
SN74ABT16374A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	89°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16374A		SN74ABT16374A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



# SN54ABT16374A, SN74ABT16374A

## 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16374A		SN74ABT16374A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -24 mA	2			2				
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA			0.55		0.55			V
				0.55*			0.55		
V <sub>hys</sub>			100						mV
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
I <sub>OZPU</sub> ‡	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZPD</sub> ‡	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	μA
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>	Outputs high, V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	μA
I <sub>O</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I <sub>CC</sub>	Outputs high			2		2		2	mA
	Outputs low			72		72		72	
	Outputs disabled	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			2		2		
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = 2.5 V or 0.5 V			3.5					pF
C <sub>o</sub>	V <sub>O</sub> = 2.5 V or 0.5 V			9.5					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C#		SN54ABT16374A		SN74ABT16374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	150	0	150	0	150	MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑	1.1		1.3		1.1		ns
t <sub>h</sub>	Hold time, data after CLK↑	1.3		1.5		1.3		ns

# These values apply only to the SN74ABT16374A.



**SN54ABT16374A, SN74ABT16374A**  
**16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16374A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$f_{max}$			150			150	MHz	
$t_{PLH}$	CLK	Q	1.8	4.3	5.7	1.5	6.9	ns
$t_{PHL}$			2.7	4.7	6.1	2.2	6.9	
$t_{PZH}$	$\overline{OE}$	Q	1.2	3.4	4.8	0.8	6.1	ns
$t_{PZL}$			1.6	3.5	4.9	1.2	5.5	
$t_{PHZ}$	$\overline{OE}$	Q	2.2	5.5	8.6	1.8	9.6	ns
$t_{PLZ}$			2.2	4.3	6.2	1.8	7.2	

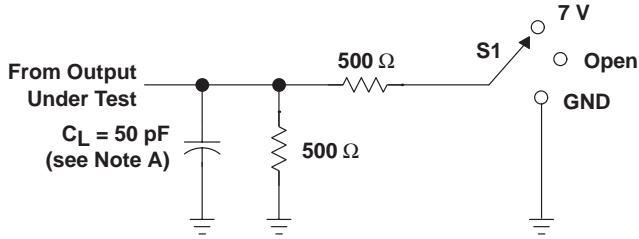
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16374A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$f_{max}$			150			150	MHz	
$t_{PLH}$	CLK	Q	1.8	4.3	5.4	1.8	6.2	ns
$t_{PHL}$			2.7	4.7	5.6	2.7	5.9	
$t_{PZH}$	$\overline{OE}$	Q	1.2	3.4	4.8	1.2	5.6	ns
$t_{PZL}$			1.6	3.5	4.7	1.6	5.3	
$t_{PHZ}$	$\overline{OE}$	Q	2.2	5.5	7.1	2.2	8.2	ns
$t_{PLZ}$			2.2	4.3	5.8	2.2	6.6	

# SN54ABT16374A, SN74ABT16374A 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

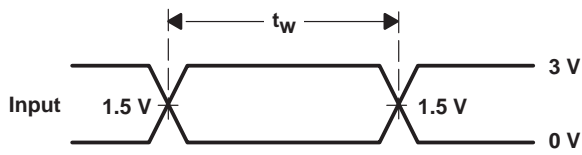
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## PARAMETER MEASUREMENT INFORMATION

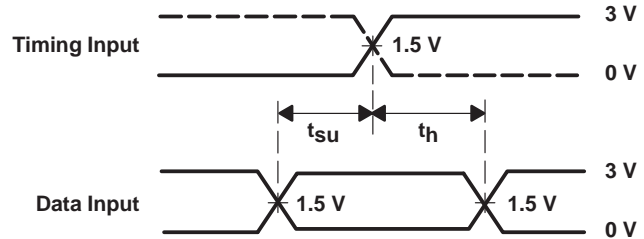


LOAD CIRCUIT

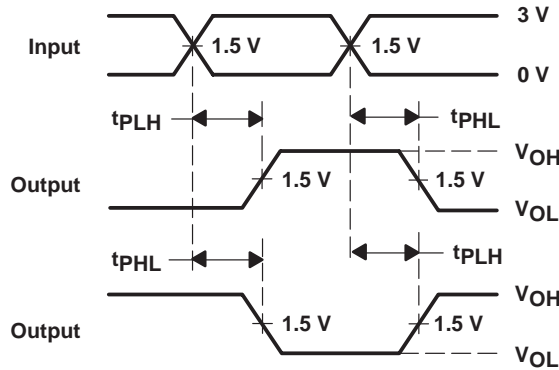
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



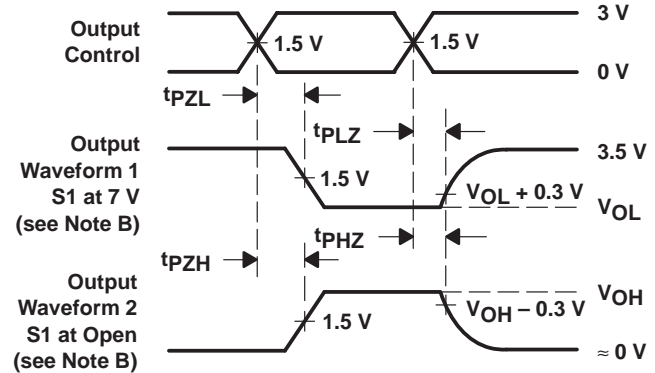
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9320101MXA	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type
74ABT16374ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16374ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16374ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16374ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16374ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16374ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT16374AWD	ACTIVE	CFP	WD	48	1	TBD	A42 SNPB	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

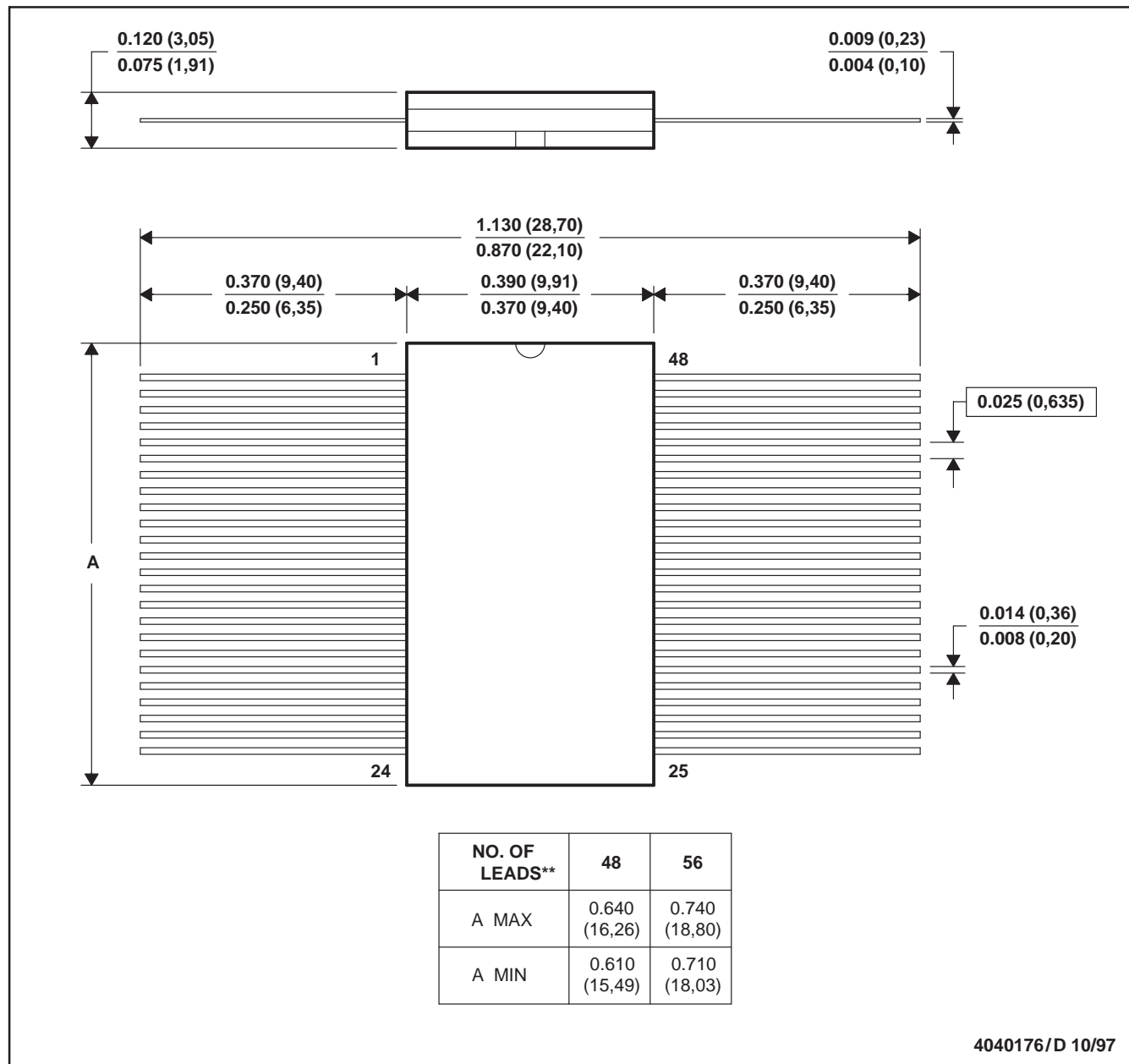
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WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

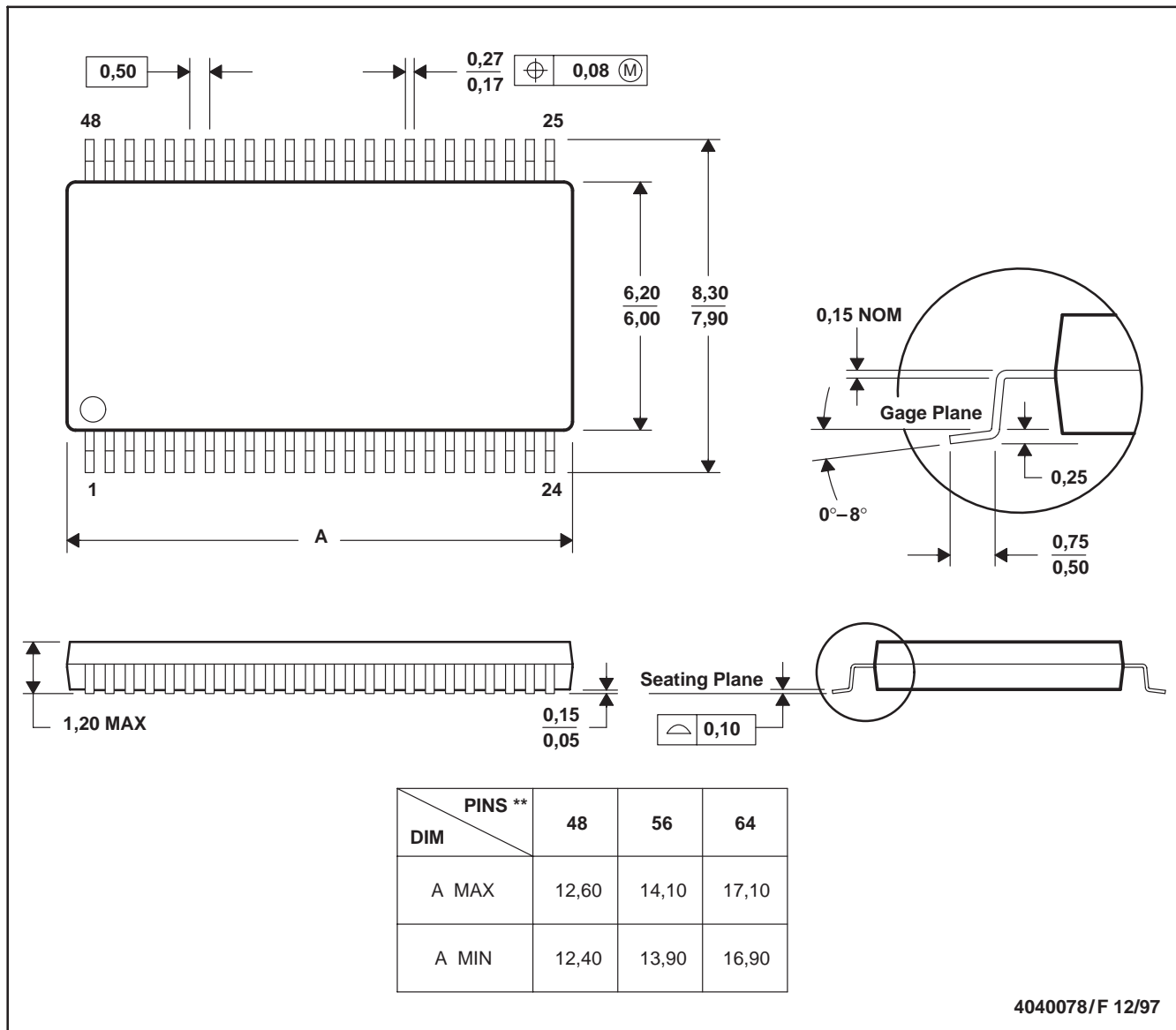


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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