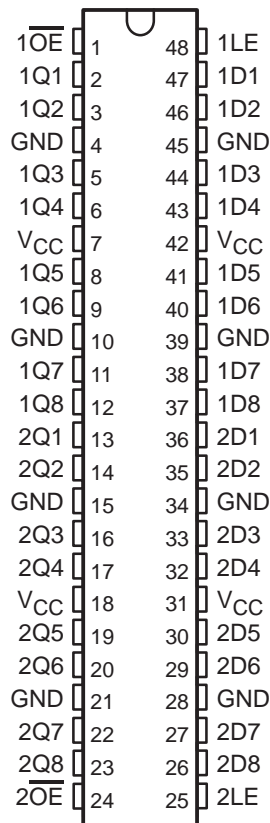


SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16373A . . . WD PACKAGE
SN74ABT16373A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16373A are 16-bit transparent D-type latches with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16373A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16373A is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54ABT16373A, SN74ABT16373A

16-BIT TRANSPARENT D-TYPE LATCHES

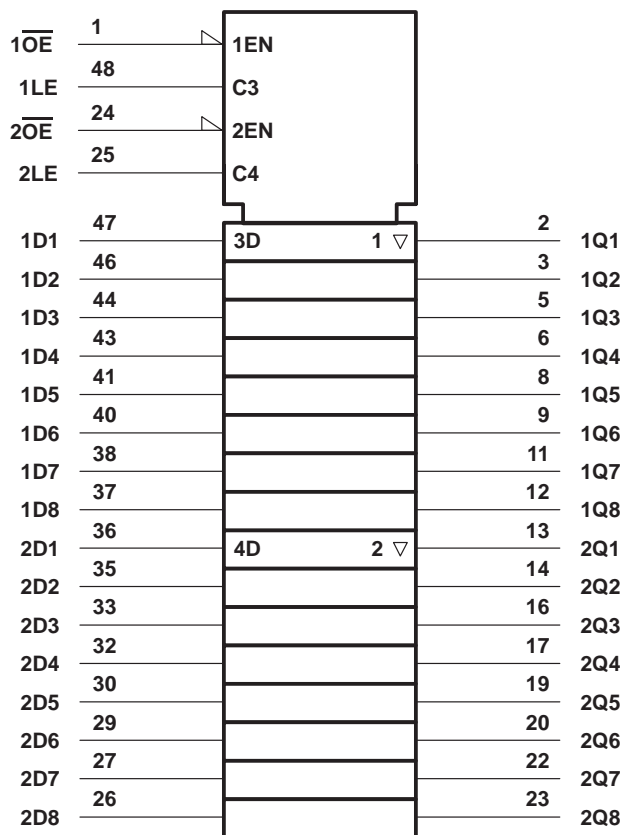
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each 8-bit section)

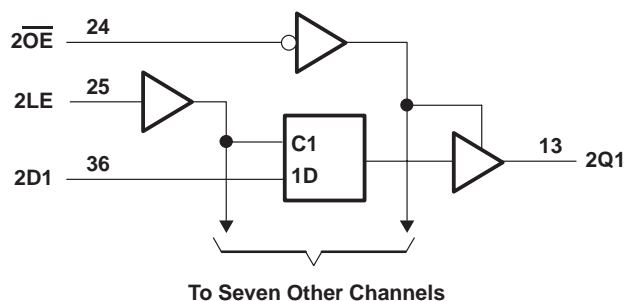
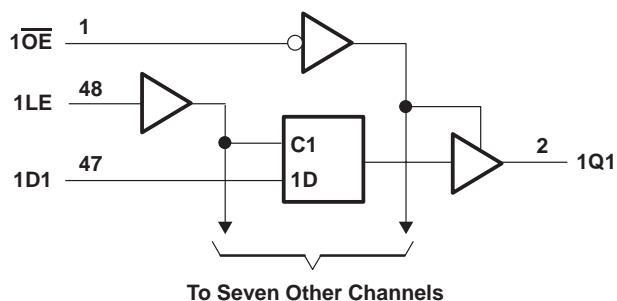
INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16373A	96 mA
SN74ABT16373A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
						Outputs enabled
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SN54ABT16373A, SN74ABT16373A
16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT16373A		SN74ABT16373A		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5	V		
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3			
	V _{CC} = 4.5 V	I _{OH} = -24 mA			2		2				
I _{OH} = -32 mA				2*				2			
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA				0.55		0.55	V		
		I _{OL} = 64 mA				0.55*		0.55			
V _{hys}				100					mV		
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND					±1		±1	µA		
I _{OZPU} ‡	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$					±50		±50	µA		
I _{OZPD} ‡	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$					±50		±50	µA		
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V					10		10	µA		
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V					-10		-10	µA		
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V					±100		±100	µA		
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V				50		50	µA		
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V				-50	-100	-180	-50	-180	mA
I _{CC}	Outputs high	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND				2		2	2	mA	
	Outputs low					85		85	85		
	Outputs disabled					2		2	2		
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				1.5		1.5	1.5	mA	
C _i		V _I = 2.5 V or 0.5 V				3.5				pF	
C _o		V _O = 2.5 V or 0.5 V				9.5				pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C#		SN54ABT16373A		SN74ABT16373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1.5		2.4		1.5		ns
t _h	Hold time, data after LE↓	1		2.2		1		ns

These values apply only to the SN74ABT16373A.



SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16373A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.4	3.7	5.3	1.4	6.5	ns
t_{PHL}			2	4	5.4	2	6.5	
t_{PLH}	LE	Q	1.7	4.1	5.7	1.7	7	ns
t_{PHL}			2.3	4.3	5.6	2.3	6.3	
t_{PZH}	\overline{OE}	Q	1.1	3.4	5	1.1	6.4	ns
t_{PZL}			1.5	3.5	4.9	1.5	5.8	
t_{PHZ}	\overline{OE}	Q	2.4	5.1	7.1	2.4	8.3	ns
t_{PLZ}			1.6	4.4	6.3	1.6	8	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16373A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.4	3.7	5.3	1.4	6.3	ns
t_{PHL}			2	4	5.4	2	6.2	
t_{PLH}	LE	Q	1.7	4.1	5.7	1.7	6.7	ns
t_{PHL}			2.3	4.3	5.6	2.3	6.1	
t_{PZH}	\overline{OE}	Q	1.1	3.4	5	1.1	6.1	ns
t_{PZL}			1.5	3.5	4.9	1.5	5.6	
t_{PHZ}	\overline{OE}	Q	2.4	5.1	7.1	2.4	8.1	ns
t_{PLZ}			1.6	4.4	5.8	1.6	6.5	

SN54ABT16373A, SN74ABT16373A 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

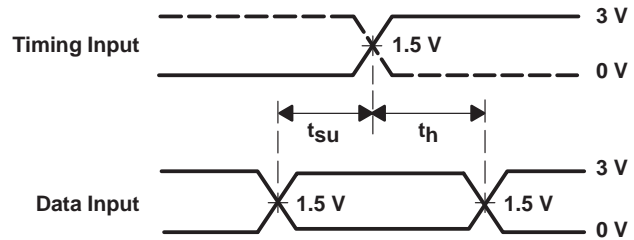


LOAD CIRCUIT

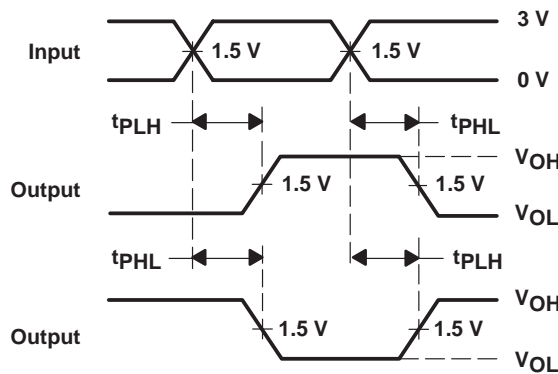
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



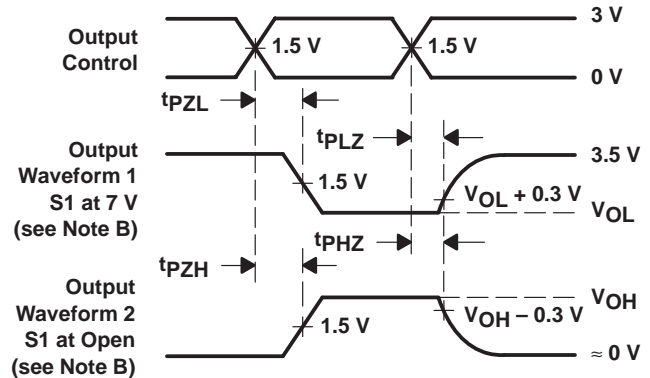
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9320001QXA	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC
74ABT16373ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ABT16373ADGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ABT16373ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16373ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16373ADLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT16373AWD	ACTIVE	CFP	WD	48	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

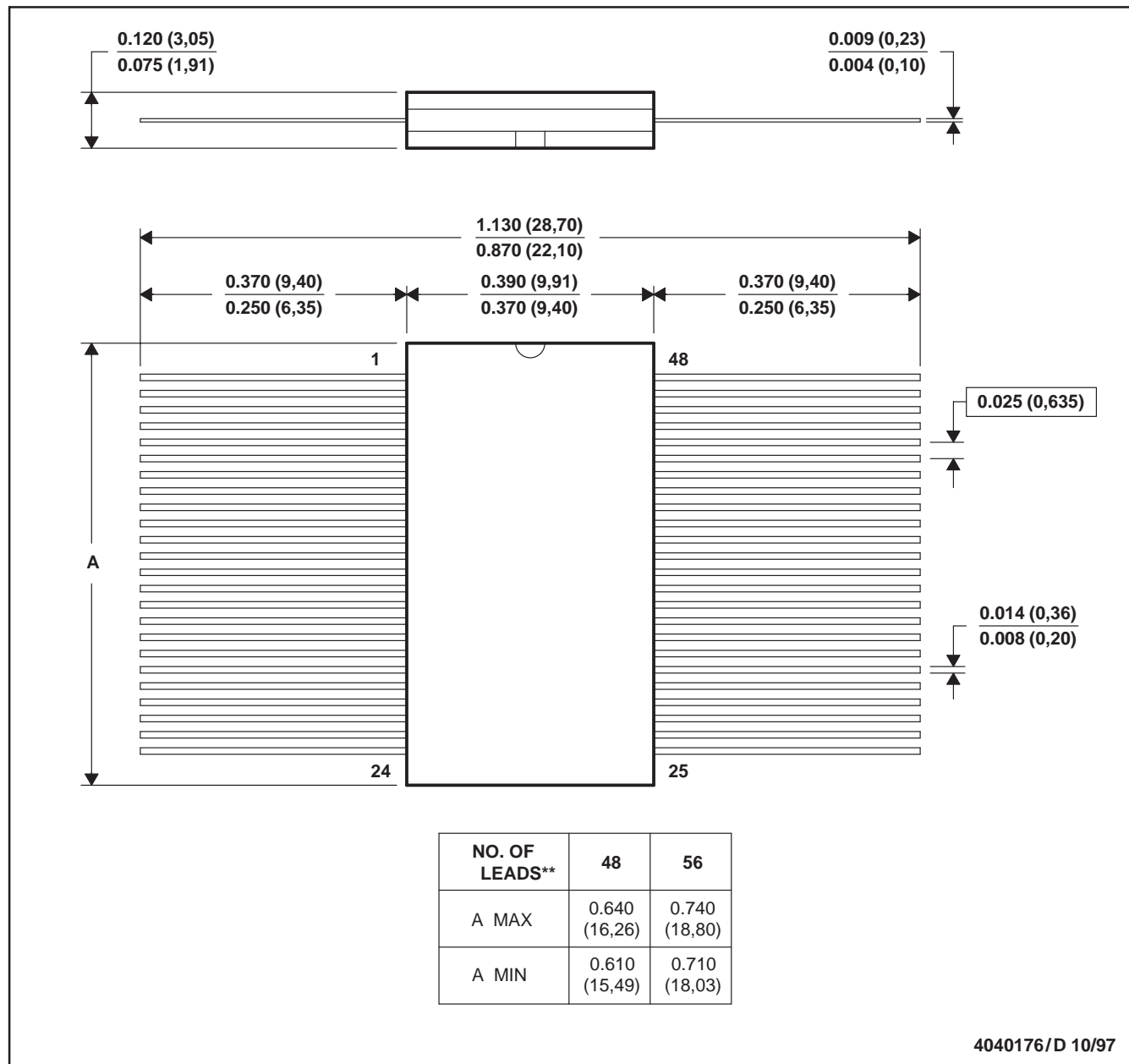
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WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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