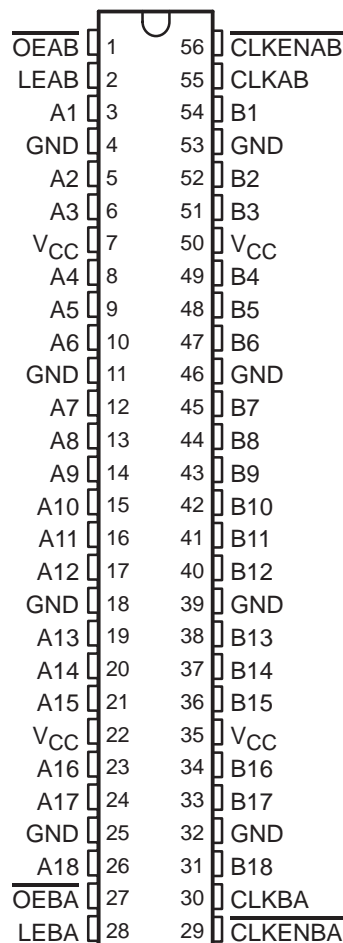


SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS247G – AUGUST 1992 – REVISED JULY 1998

- **Members of the Texas Instruments Widebus™ Family**
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT162601 . . . WD PACKAGE
SN74ABT162601 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If \overline{LEAB} is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output-enable \overline{OEAB} is active-low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA, and $\overline{CLKENBA}$.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ABT162601, SN74ABT162601
18-BIT UNIVERSAL BUS TRANSCEIVERS
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description (continued)

The SN54ABT162601 is characterized for operation over the full military temperature range of -55°C to 125°C .
 The SN74ABT162601 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

| INPUTS | | | | | OUTPUT |
|---------|------|------|-------|---|------------------|
| CLKENAB | OEAB | LEAB | CLKAB | A | B |
| X | H | X | X | X | Z |
| X | L | H | X | L | L |
| X | L | H | X | H | H |
| H | L | L | X | X | B_0^{\ddagger} |
| H | L | L | X | X | B_0^{\ddagger} |
| L | L | L | ↑ | L | L |
| L | L | L | ↑ | H | H |
| L | L | L | L | X | B_0^{\ddagger} |
| L | L | L | H | X | B_0^{\S} |

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established

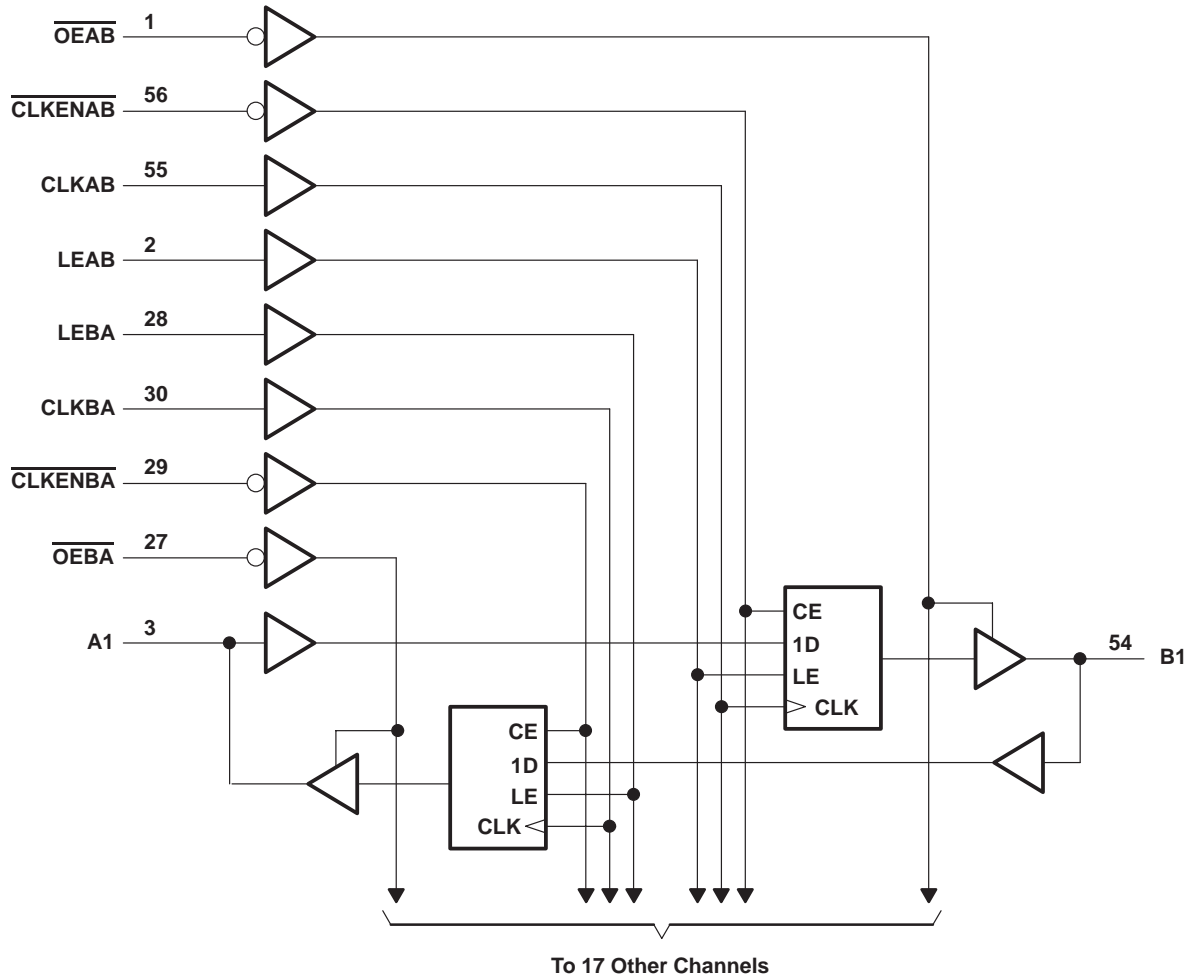
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low



SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (except I/O ports) (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT162601 (A port) | 96 mA |
| SN74ABT162601 (A port) | 128 mA |
| B port | 30 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DGG package | 81°C/W |
| DL package | 74°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.



SN54ABT162601, SN74ABT162601
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recommended operating conditions (see Note 3)

| | | SN54ABT162601 | | SN74ABT162601 | | UNIT | |
|--------------------------|------------------------------------|---------------|----------|-----------------|----------|------|--------------|
| | | MIN | MAX | MIN | MAX | | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V | |
| V_{IH} | High-level input voltage | 2 | | 2 | | V | |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V | |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V | |
| I_{OH} | High-level output current | A port | -24 | | -32 | mA | |
| | | B port | | -12 | | | -12 |
| I_{OL} | Low-level output current | A port | | 48 | | mA | |
| | | B port | | | 12 | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | Outputs enabled | 10 | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | | μ s/V |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | | $^{\circ}$ C |

NOTE 3: All unused inputs of the devices must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ABT162601, SN74ABT162601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T _A = 25°C | | | SN54ABT162601 | | SN74ABT162601 | | UNIT |
|--|---|--|--|-------|------|---------------|------|---------------|------|------|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V _{IK} | | V _{CC} = 4.5 V, I _I = -18 mA | -1.2 | | | -1.2 | | -1.2 | | V |
| V _{OH} | A port | V _{CC} = 4.5 V, I _{OH} = -3 mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | V _{CC} = 5 V, I _{OH} = -3 mA | 3 | | | 3 | | 3 | | |
| | | V _{CC} = 4.5 V, I _{OH} = -24 mA | 2 | | | 2 | | | | |
| | | V _{CC} = 4.5 V, I _{OH} = -32 mA | 2* | | | | | 2 | | |
| | B port | V _{CC} = 4.5 V, I _{OH} = -1 mA | 3.35 | | | 3.3 | | 3.35 | | |
| | | V _{CC} = 5 V, I _{OH} = -1 mA | 3.85 | | | 3.8 | | 3.85 | | |
| V _{CC} = 4.5 V, I _{OH} = -3 mA | | 3.1 | | | 3 | | 3.1 | | | |
| | V _{CC} = 4.5 V, I _{OH} = -12 mA | 2.6 | | | | | 2.6 | | | |
| V _{OL} | A port | V _{CC} = 4.5 V, I _{OL} = 48 mA | 0.55 | | | 0.55 | | | | V |
| | | | V _{CC} = 4.5 V, I _{OL} = 64 mA | 0.55* | | | | | 0.55 | |
| | B port | V _{CC} = 4.5 V, I _{OL} = 12 mA | 0.8 | | | 0.8 | | 0.8 | | |
| V _{hys} | | | 100 | | | | | | | mV |
| I _I | Control inputs | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | ±1 | | | ±1 | | ±1 | | μA |
| | A or B ports | V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND | ±20 | | | ±20 | | ±20 | | |
| I _{OZPU} | | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | ±50 | | | ±50** | | ±50 | | μA |
| I _{OZPD} | | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$ | ±50 | | | ±50** | | ±50 | | μA |
| I _{OZH} ‡ | | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V | 10 | | | 10 | | 10 | | μA |
| I _{OZL} ‡ | | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V | -10 | | | -10 | | -10 | | μA |
| I _{off} | | V _{CC} = 0, V _I or V _O ≤ 4.5 V | ±100* | | | | | ±100 | | μA |
| I _{CEX} | | V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high | 50 | | | 50 | | 50 | | μA |
| I _O § | A port | V _{CC} = 5.5 V, V _O = 2.5 V | -50 | -100 | -180 | -50 | -180 | -50 | -180 | mA |
| | B port | | -25 | -55 | -100 | -25 | -100 | -25 | -100 | |
| I _{CC} | A or B ports | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND, Outputs high | 3 | | | 3 | | 3 | | mA |
| | | | 36 | | | 36 | | 36 | | |
| | | | 3 | | | 3 | | 3 | | |
| ΔI _{CC} ¶ | | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | 50 | | | 50 | | 50 | | μA |
| C _i | Control inputs | V _I = 2.5 V or 0.5 V | 3 | | | | | | | pF |
| C _{io} | A or B ports | V _O = 2.5 V or 0.5 V | 9 | | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT162601, SN74ABT162601
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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(see Figure 1)

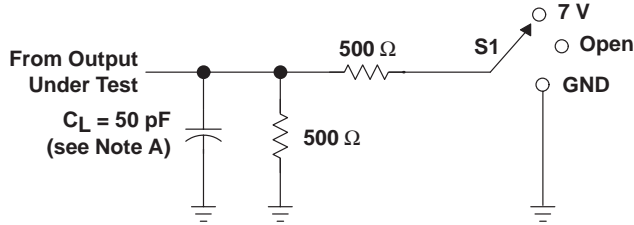
| | | SN54ABT162601 | | SN74ABT162601 | | UNIT |
|-------------|-----------------|--|----------|---------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 0 | 150 | 0 | 150 | MHz |
| t_w | Pulse duration | LEAB or LEBA high | | 2.5 | | ns |
| | | CLKAB or CLKBA high or low | | 3.3 | | |
| t_{su} | Setup time | A before CLKAB \uparrow or B before CLKBA \uparrow | | 4.8 | | ns |
| | | A before LEAB \downarrow or B before LEBA \downarrow | CLK high | 2.5 | | |
| | | | CLK low | 1.2 | | |
| | | CLKEN before CLK \uparrow | | 2.7 | | |
| t_h | Hold time | A after CLKAB \uparrow or B after CLKBA \uparrow | | 0.5 | | ns |
| | | A after LEAB \downarrow or B after LEBA \downarrow | | 2 | | |
| | | CLKEN after CLK \uparrow | | 0.5 | | |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ$ C | | | SN54ABT162601 | | SN74ABT162601 | | UNIT |
|-----------|-------------------|-------------|---------------------------------------|-----|-----|---------------|-----|---------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 150 | | | 150 | | 150 | | MHz |
| t_{PLH} | A | B | 1.5 | 2.8 | 4 | 1.5 | 5.1 | 1.5 | 4.8 | ns |
| t_{PHL} | | | 2 | 3.7 | 5.2 | 2 | 6.1 | 2 | 5.7 | |
| t_{PLH} | B | A | 1 | 2.5 | 3.6 | 1 | 4.5 | 1 | 4 | ns |
| t_{PHL} | | | 2 | 3.3 | 4.5 | 2 | 5.1 | 2 | 4.9 | |
| t_{PLH} | LEBA | A | 2 | 3.3 | 4.5 | 2 | 5.6 | 2 | 5 | ns |
| t_{PHL} | | | 2 | 3.6 | 4.7 | 2 | 5.4 | 2 | 5 | |
| t_{PLH} | LEAB | B | 2 | 3.4 | 4.8 | 2 | 6.1 | 2 | 5.6 | ns |
| t_{PHL} | | | 2 | 3.8 | 5.2 | 2 | 6.4 | 2 | 5.9 | |
| t_{PLH} | CLKBA | A | 1.5 | 3.1 | 4.7 | 1.5 | 5.4 | 1.5 | 5.3 | ns |
| t_{PHL} | | | 1.5 | 3.1 | 4.3 | 1.5 | 5.2 | 1.5 | 5 | |
| t_{PLH} | CLKAB | B | 1.5 | 3.3 | 4.7 | 1.5 | 6 | 1.5 | 5.5 | ns |
| t_{PHL} | | | 1.5 | 3.5 | 4.8 | 1.5 | 5.8 | 1.5 | 5.3 | |
| t_{PZH} | \overline{OEBA} | A | 2 | 3.5 | 4.6 | 2 | 5.5 | 2 | 5.1 | ns |
| t_{PZL} | | | 2 | 3.7 | 4.7 | 2 | 5.8 | 2 | 5.4 | |
| t_{PZH} | \overline{OEAB} | B | 2 | 3.8 | 5.3 | 1.5 | 6.6 | 2 | 6.1 | ns |
| t_{PZL} | | | 2 | 3.6 | 5.1 | 2 | 6.2 | 2 | 5.7 | |
| t_{PHZ} | \overline{OEBA} | A | 2 | 3.6 | 5.4 | 1.4 | 6.6 | 2 | 6.2 | ns |
| t_{PLZ} | | | 1.5 | 3.2 | 4.7 | 1.5 | 5.8 | 1.5 | 5.4 | |
| t_{PHZ} | \overline{OEAB} | B | 2 | 3.4 | 4.8 | 1.4 | 5.6 | 2 | 5.4 | ns |
| t_{PLZ} | | | 1.5 | 3.2 | 4.5 | 1.5 | 5.7 | 1.5 | 5.2 | |

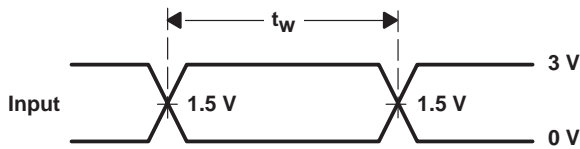


PARAMETER MEASUREMENT INFORMATION

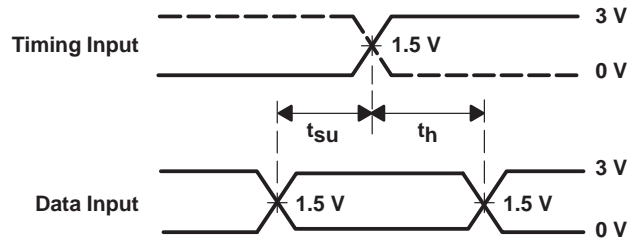


LOAD CIRCUIT

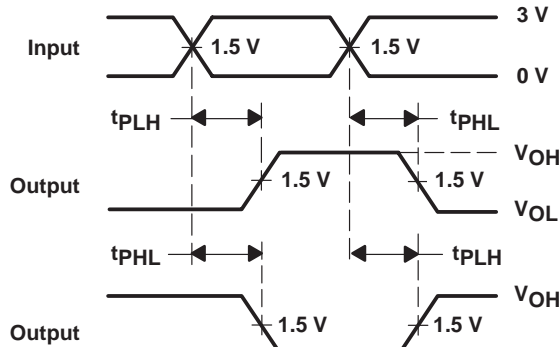
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



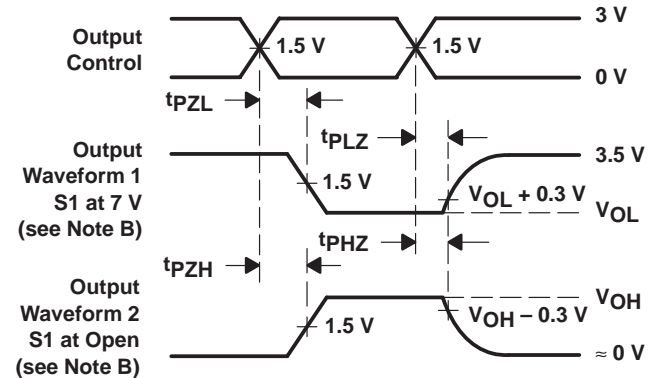
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|-------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-9859301QXA | ACTIVE | CFP | WD | 56 | 1 | TBD | Call TI | Call TI | |
| 74ABT162601DGGRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74ABT162601DGGRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| 74ABT162601DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT162601DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT162601DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT162601DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74ABT162601DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54ABT162601WD | ACTIVE | CFP | WD | 56 | 1 | TBD | A42 | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ABT162601, SN74ABT162601 :

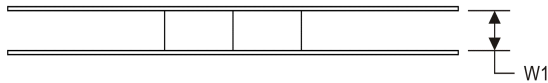
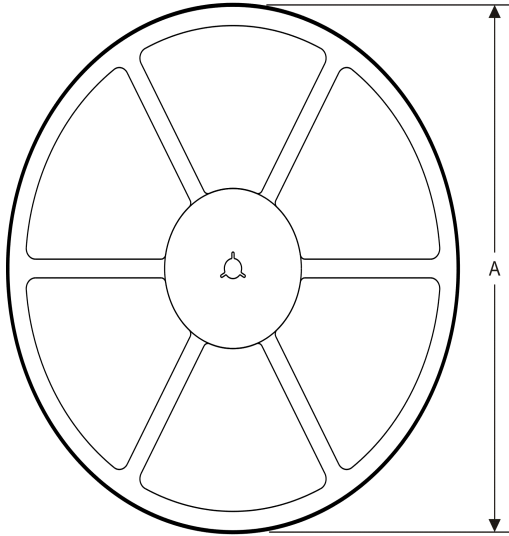
- Catalog: [SN74ABT162601](#)
- Military: [SN54ABT162601](#)

NOTE: Qualified Version Definitions:

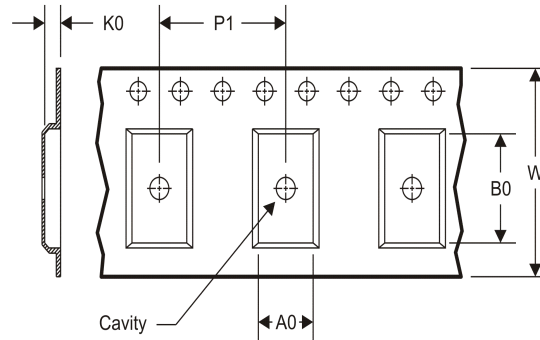
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT162601DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ABT162601DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

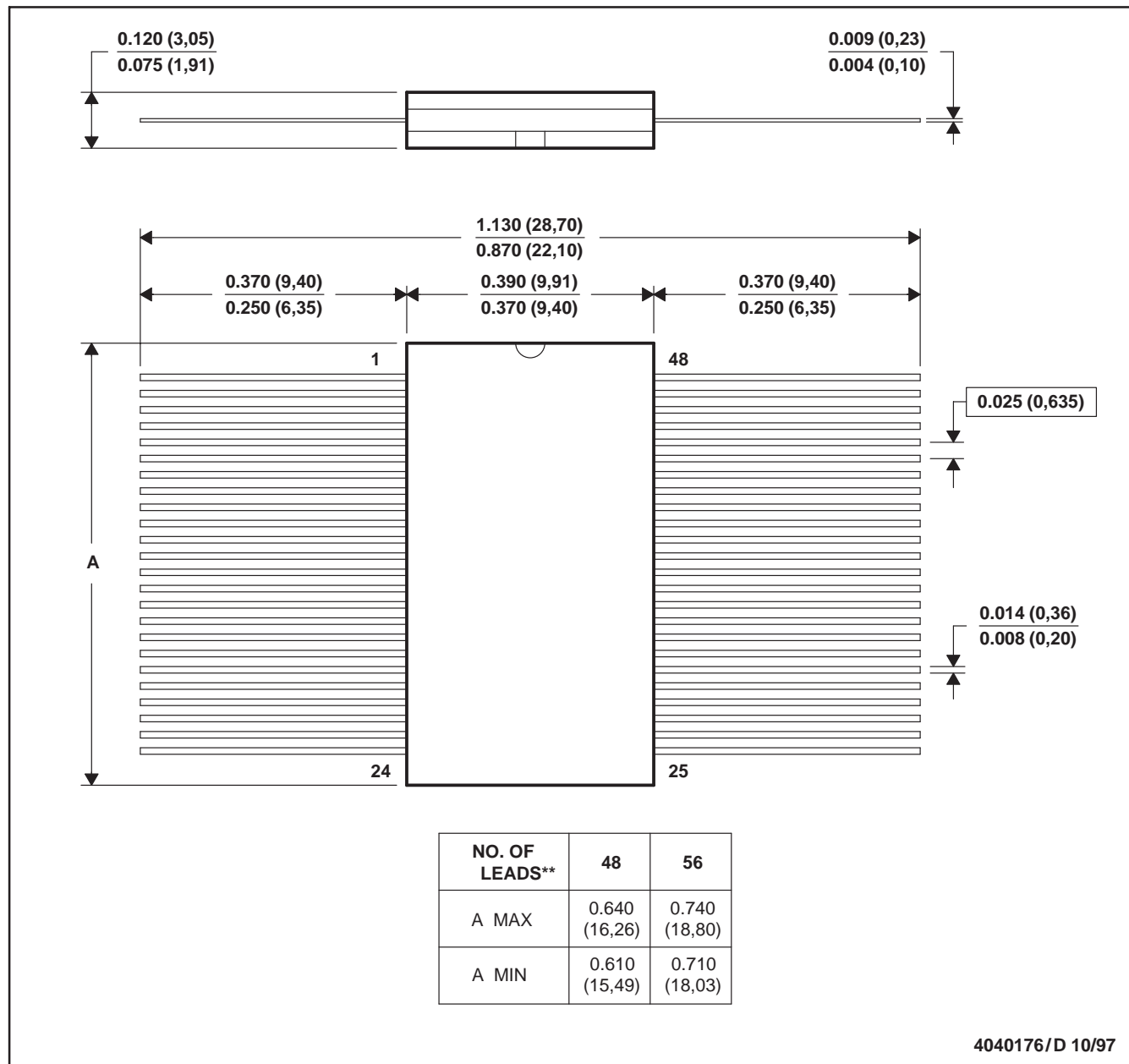

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT162601DGGR | TSSOP | DGG | 56 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ABT162601DLR | SSOP | DL | 56 | 1000 | 367.0 | 367.0 | 55.0 |

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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