

## MULTIPOINT-LVDS LINE DRIVER AND RECEIVER

### FEATURES

- **Low-Voltage Differential 30-Ω to 55-Ω Line Drivers and Receivers for Signaling Rates (1) Up to 100 Mbps, Clock Frequencies up to 50 MHz**
- **Type-1 Receivers Incorporate 25 mV of Hysteresis (200A, 202A)**
- **Type-2 Receivers Provide an Offset(100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions (204A, 205A)**
- **Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange**
- **Power Up/Down Glitch Free**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **–1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer With 2 V of Ground Noise**
- **Bus Pins High Impedance When Disabled or  $V_{CC} \leq 1.5$  V**
- **200-Mbps Devices Available (SN65MLVD201, 203, 206, 207)**
- **Bus Pin ESD Protection Exceeds 8 kV**
- **Package in 8-Pin SOIC (200A, 204A) and 14-Pin SOIC (202A, 205A)**
- **Improved Alternatives to the SN65MLVD200, 202, 204, and 205**

### APPLICATIONS

- **Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485**
  - **Backplane or Cabled Multipoint Data and Clock Transmission**
  - **Cellular Base Stations**
  - **Central-Office Switches**
  - **Network Switches and Routers**
- (1) The signaling rate of a line, is the number of voltage transitions that are made per second expressed in the nits bps (bits per second).

### DESCRIPTION

The SN65MLVD200A, 202A, 204A, and 205A are multipoint-low-voltage differential (M-LVDS) line drivers and receivers, which are optimized to operate at signaling rates up to 100 Mbps. All parts comply with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of –1 V to 3.4 V. The Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. Type-2 receivers include an offset threshold to provide a known output state under open-circuit, idle-bus, and other fault conditions.

The SN65MLVD200A, 202A, 204A, and 205A have enhancements over their predecessors. Improved features include better controlled slew rate on the driver output to help minimize reflections while improving overall signal integrity (SI) resulting in better jitter performance. Additionally, 8-kV ESD protection on the bus pins for more robustness. The same footprint definition was maintained making for an easy drop-in replacement for a system performance upgrade.

The devices are characterized for operation from –40°C to 85°C.



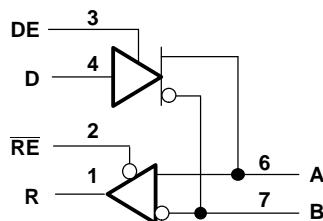
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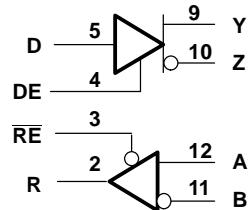
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## LOGIC DIAGRAM (POSITIVE LOGIC)

SN65MLVD200A, SN65MLVD204A



SN65MLVD202A, SN65MLVD205A



## ORDERING INFORMATION

PART NUMBER <sup>(1)</sup>	FOOTPRINT	RECEIVER TYPE	PACKAGE MARKING
SN65MLVD200AD	SN75176	Type 1	MF200A
SM65MLVD202AD	SN75ALS180	Type 1	MLVD202A
SN65MLVD204AD	SN75176	Type 2	MF204A
SM65MLVD205AD	SN75ALS180	Type 2	MLVD205A

(1) Available tape and reeled. To order a tape and reeled part, add the suffix R to the part number (e.g., SN65MLVD200ADR).

## PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D(8)	532 mW	4.6 mW/ $^\circ\text{C}$	254 mW
D(14)	940 mW	8.2 mW/ $^\circ\text{C}$	450 mW

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

		SN65MLVD200A, 202A, 204A, and 205A	
Supply voltage range <sup>(2)</sup> , $V_{CC}$		-0.5 V to 4 V	
Input voltage range	D, DE, $\overline{RE}$	-0.5 V to 4 V	
	A, B (200A, 204A)	-1.8 V to 4 V	
	A, B (202A, 205A)	-4 V to 6 V	
Output voltage range	R	-0.3 V to 4 V	
	Y, Z, A, or B	-1.8 V to 4 V	
Electrostatic discharge	Human Body Model <sup>(3)</sup>	A, B, Y, and Z	$\pm 8$ kV
		All pins	$\pm 4$ kV
	Charged-Device Model <sup>(4)</sup>	All pins	$\pm 1500$ V
Continuous power dissipation		See Dissipation Rating Table	
Storage temperature range		-65 $^\circ\text{C}$ to 150 $^\circ\text{C}$	

(1) Stresses beyond those listed *under absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated *under recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.3	3.6	V
$V_{IH}$	High-level input voltage	2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	GND		0.8	V
	Voltage at any bus terminal $V_A$ , $V_B$ , $V_Y$ or $V_Z$	-1.4		3.8	V
$ V_{ID} $	Magnitude of differential input voltage	0.05		$V_{CC}$	V
$R_L$	Differential load resistance	30	50		$\Omega$
$1/t_{UI}$	Signaling rate			100	Mbps
$T_A$	Operating free-air temperature	-40		85	$^{\circ}\text{C}$

## DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$I_{CC}$	Supply current	Driver only		13	22	mA	
		Both disabled	$\overline{RE}$ at $V_{CC}$ , DE at 0 V, $R_L$ = No Load, All others open		1		4
		Both enabled	$\overline{RE}$ at 0 V, DE at $V_{CC}$ , $R_L$ = 50 $\Omega$ , All others open		16		24
		Receiver only	$\overline{RE}$ at 0 V, DE at 0 V, All others open		4		13
$P_D$	Device power dissipation	$R_L$ = 50 $\Omega$ , Input to D is a 50-MHz 50% duty cycle square wave, DE = high, $\overline{RE}$ = low, $T_A$ = 85 $^{\circ}\text{C}$			94	mW	

(1) All typical values are at 25 $^{\circ}\text{C}$  and with a 3.3-V supply voltage.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX	UNIT	
$ V_{AB} $ or $ V_{YZ} $	Differential output voltage magnitude	See Figure 2		480	650	mV
$\Delta V_{AB} $ or $\Delta V_{YZ} $	Change in differential output voltage magnitude between logic states			-50	50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3		0.8	1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states			-50	50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$ or $V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7		0	2.4	V
$V_{Z(OC)}$ or $V_{B(OC)}$	Maximum steady-state open-circuit output voltage			0	2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			1.2 $V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output			-0.2 $V_{SS}$		V
$I_{IH}$	High-level input current (D, DE)	$V_{IH} = 2\text{ V to }V_{CC}$		0	10	$\mu\text{A}$
$I_{IL}$	Low-level input current (D, DE)	$V_{IL} = \text{GND to }0.8\text{ V}$		0	10	$\mu\text{A}$
$ I_{OS} $	Differential short-circuit output current magnitude	See Figure 4			24	mA
$I_{OZ}$	High-impedance state output current (driver only)	$-1.4\text{ V} \leq (V_Y \text{ or } V_Z) \leq 3.8\text{ V}$ , Other output = 1.2 V		-15	10	$\mu\text{A}$
$I_{O(OFF)}$	Power-off output current	$-1.4\text{ V} \leq (V_Y \text{ or } V_Z) \leq 3.8\text{ V}$ , Other output = 1.2 V, $0\text{ V} \leq V_{CC} \leq 1.5\text{ V}$		-10	10	$\mu\text{A}$
$C_Y$ or $C_Z$	Output capacitance	$V_I = 0.4 \sin(30E6\pi t) + 0.5\text{ V}$ , <sup>(3)</sup> Other input at 1.2 V, driver disabled			3	pF
$C_{YZ}$	Differential output capacitance	$V_{AB} = 0.4 \sin(30E6\pi t)\text{ V}$ , <sup>(3)</sup> Driver disabled			2.5	pF
$C_{Y/Z}$	Output capacitance balance, ( $C_Y/C_Z$ )			0.99	1.01	

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.  
(2) All typical values are at 25°C and with a 3.3-V supply voltage.  
(3) HP4194A impedance analyzer (or equivalent)

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IT+</sub>	Positive-going differential input voltage threshold	Type 1			50	mV	
		Type 2			150		
V <sub>IT-</sub>	Negative-going differential input voltage threshold	Type 1	See Figure 9, Table 1 and Table 2	-50		mV	
		Type 2		50			
V <sub>HYS</sub>	Differential input voltage hysteresis, (V <sub>IT+</sub> - V <sub>IT-</sub> )	Type 1			25		mV
		Type 2			0		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -8 mA	2.4			V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 8 mA			0.4	V	
I <sub>IH</sub>	High-level input current ( $\overline{RE}$ )	V <sub>IH</sub> = 2 V to V <sub>CC</sub>	-10		0	μA	
I <sub>IL</sub>	Low-level input current ( $\overline{RE}$ )	V <sub>IL</sub> = GND to 0.8 V	-10		0	μA	
I <sub>OZ</sub>	High-impedance output current	V <sub>O</sub> = 0 V or 3.6 V	-10		15	μA	
C <sub>A</sub> or C <sub>B</sub>	Input capacitance	V <sub>I</sub> = 0.4 sin(30E6πt) + 0.5 V, <sup>(2)</sup> Other input at 1.2 V		3		pF	
C <sub>AB</sub>	Differential input capacitance	V <sub>AB</sub> = 0.4 sin(30E6πt) V <sup>(2)</sup>			2.5	pF	
C <sub>A/B</sub>	Input capacitance balance, (C <sub>A</sub> /C <sub>B</sub> )		0.99		1.01		

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

## BUS INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>A</sub>	Receiver or transceiver with driver disabled input current	V <sub>A</sub> = 3.8 V, V <sub>B</sub> = 1.2 V,	0		32	μA
		V <sub>A</sub> = 0 V or 2.4 V, V <sub>B</sub> = 1.2 V	-20		20	
		V <sub>A</sub> = -1.4 V, V <sub>B</sub> = 1.2 V	-32		0	
I <sub>B</sub>	Receiver or transceiver with driver disabled input current	V <sub>B</sub> = 3.8 V, V <sub>A</sub> = 1.2 V	0		32	μA
		V <sub>B</sub> = 0 V or 2.4 V, V <sub>A</sub> = 1.2 V	-20		20	
		V <sub>B</sub> = -1.4 V, V <sub>A</sub> = 1.2 V	-32		0	
I <sub>AB</sub>	Receiver or transceiver with driver disabled differential input current (I <sub>A</sub> - I <sub>B</sub> )	V <sub>A</sub> = V <sub>B</sub> , 1.4 ≤ V <sub>A</sub> ≤ 3.8 V	-4		4	μA
I <sub>A(OFF)</sub>	Receiver or transceiver power-off input current	V <sub>A</sub> = 3.8 V, V <sub>B</sub> = 1.2 V, 0 V ≤ V <sub>CC</sub> ≤ 1.5 V	0		32	μA
		V <sub>A</sub> = 0 V or 2.4 V, V <sub>B</sub> = 1.2 V, 0 V ≤ V <sub>CC</sub> ≤ 1.5 V	-20		20	
		V <sub>A</sub> = -1.4 V, V <sub>B</sub> = 1.2 V, 0 V ≤ V <sub>CC</sub> ≤ 1.5 V	-32		0	
I <sub>B(OFF)</sub>	Receiver or transceiver power-off input current	V <sub>B</sub> = 3.8 V, V <sub>A</sub> = 1.2 V, 0 V ≤ V <sub>CC</sub> ≤ 1.5 V	0		32	μA
		V <sub>B</sub> = 0 V or 2.4 V, V <sub>A</sub> = 1.2 V, 0 V ≤ V <sub>CC</sub> ≤ 1.5 V	-20		20	
		V <sub>B</sub> = -1.4 V, V <sub>A</sub> = 1.2 V, 0 V ≤ V <sub>CC</sub> ≤ 1.5 V	-32		0	
I <sub>AB(OFF)</sub>	Receiver input or transceiver power-off differential input current (I <sub>A</sub> - I <sub>B</sub> )	V <sub>A</sub> = V <sub>B</sub> , 0 V ≤ V <sub>CC</sub> ≤ 1.5 V, -1.4 ≤ V <sub>A</sub> ≤ 3.8 V	-4		4	μA
C <sub>A</sub>	Transceiver with driver disabled input capacitance	V <sub>A</sub> = 0.4 sin(30E6πt) + 0.5 V <sup>(2)</sup> , V <sub>B</sub> = 1.2 V		5		pF
C <sub>B</sub>	Transceiver with driver disabled input capacitance	V <sub>B</sub> = 0.4 sin(30E6πt) + 0.5 V <sup>(2)</sup> , V <sub>A</sub> = 1.2 V		5		pF
C <sub>AB</sub>	Transceiver with driver disabled differential input capacitance	V <sub>AB</sub> = 0.4 sin(30E6πt) V <sup>(2)</sup>			3	pF
C <sub>A/B</sub>	Transceiver with driver disabled input capacitance balance, (C <sub>A</sub> /C <sub>B</sub> )		0.99		1.01	

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pLH}$	Propagation delay time, low-to-high-level output	See Figure 5	2	2.5	3.5	ns
$t_{pHL}$	Propagation delay time, high-to-low-level output		2	2.5	3.5	ns
$t_r$	Differential output signal rise time		2	2.6	3.2	ns
$t_f$	Differential output signal fall time		2	2.6	3.2	ns
$t_{sk(p)}$	Pulse skew ( $t_{pHL} - t_{pLH}$ )				30	150
$t_{sk(pp)}$	Part-to-part skew				0.9	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) <sup>(2)</sup>	50 MHz clock input <sup>(3)</sup>		2	3	ps
$t_{jit(pp)}$	Peak-to-peak jitter <sup>(2)(4)</sup>	100 Mbps 2 <sup>15</sup> -1 PRBS input <sup>(5)</sup>		55	150	ps
$t_{PHZ}$	Disable time, high-level-to-high-impedance output	See Figure 6		4	7	ns
$t_{PLZ}$	Disable time, low-level-to-high-impedance output			4	7	ns
$t_{PZH}$	Enable time, high-impedance-to-high-level output			4	7	ns
$t_{PZL}$	Enable time, high-impedance-to-low-level output			4	7	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(3)  $t_r = t_f = 0.5$  ns (10% to 90%), measured over 30 k samples.

(4) Peak-to-peak jitter includes jitter due to pulse skew ( $t_{sk(p)}$ ).

(5)  $t_r = t_f = 0.5$  ns (10% to 90%), measured over 100 k samples.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup> (1)	MAX	UNIT
$t_{pLH}$	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, See Figure 10	2	3.6	6	ns
$t_{pHL}$	Propagation delay time, high-to-low-level output		2	3.6	6	ns
$t_r$	Output signal rise time		1		2.3	ns
$t_f$	Output signal fall time		1		2.3	ns
$t_{sk(p)}$	Pulse skew ( $t_{pHL} - t_{pLH}$ )		Type 1		100	300
		Type 2		300	500	ps
$t_{sk(pp)}$	Part-to-part skew <sup>(2)</sup>				1	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) <sup>(3)</sup>	50 MHz clock input <sup>(4)</sup>		4	7	ps
$t_{jit(pp)}$	Peak-to-peak jitter <sup>(3)(5)</sup>	Type 1		200	700	ps
		Type 2		225	800	ps
$t_{PHZ}$	Disable time, high-level-to-high-impedance output	See Figure 11		6	10	ns
$t_{PLZ}$	Disable time, low-level-to-high-impedance output			6	10	ns
$t_{PZH}$	Enable time, high-impedance-to-high-level output			10	15	ns
$t_{PZL}$	Enable time, high-impedance-to-low-level output			10	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2) HP4194A impedance analyzer (or equivalent)

(3) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.

(4)  $V_{ID} = 200$  mV<sub>pp</sub> (LVD200A, 202A),  $V_{ID} = 400$  mV<sub>pp</sub> (LVD204A, 205A),  $V_{cm} = 1$  V,  $t_r = t_f = 0.5$  ns (10% to 90%), measured over 30 k samples.

(5) Peak-to-peak jitter includes jitter due to pulse skew ( $t_{sk(p)}$ ).

(6)  $V_{ID} = 200$  mV<sub>pp</sub> (LVD200A, 202A),  $V_{ID} = 400$  mV<sub>pp</sub> (LVD204A, 205A),  $V_{cm} = 1$  V,  $t_r = t_f = 0.5$  ns (10% to 90%), measured over 100 k samples.

PARAMETER MEASUREMENT INFORMATION

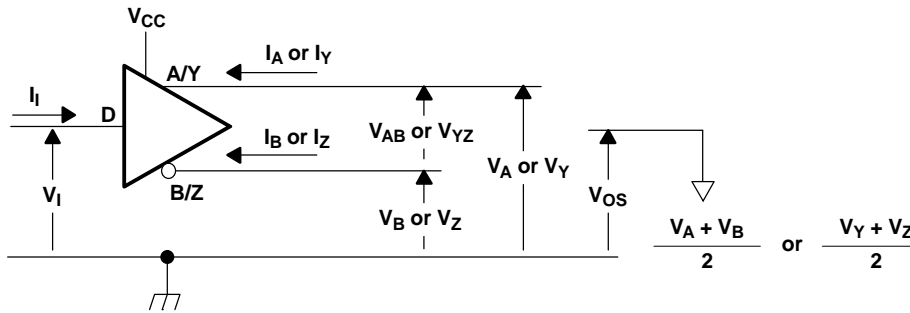
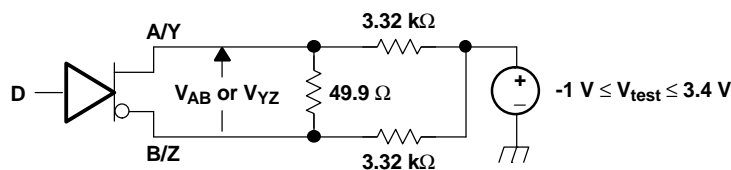
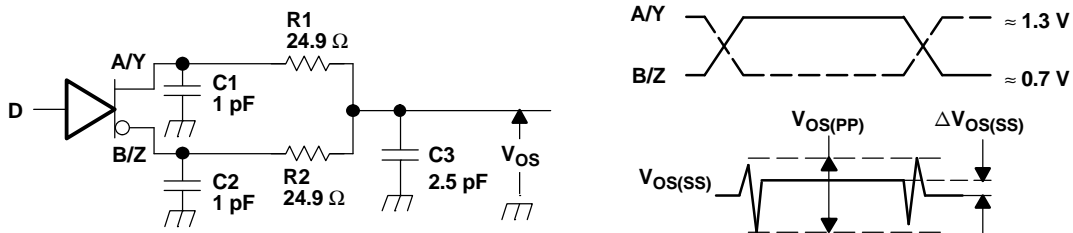


Figure 1. Driver Voltage and Current Definitions



- A. All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- C. R1 and R2 are metal film, surface mount,  $\pm 1\%$ , and located within 2 cm of the D.U.T.
- D. The measurement of  $V_{OS(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

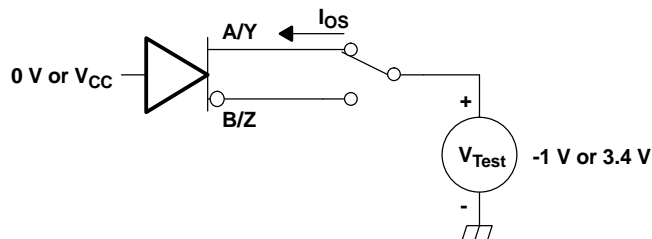
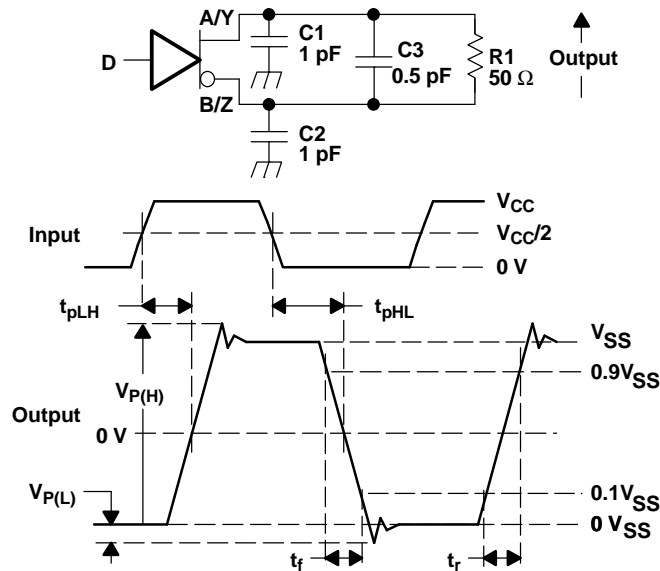


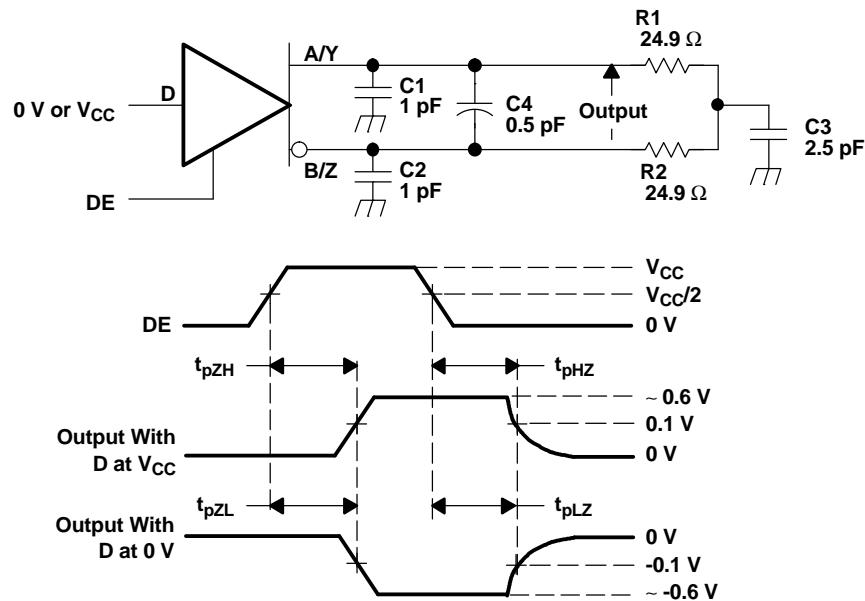
Figure 4. Driver Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

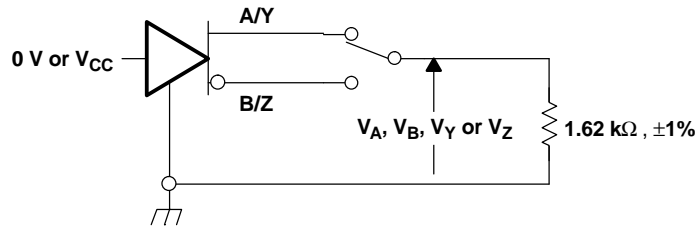
Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



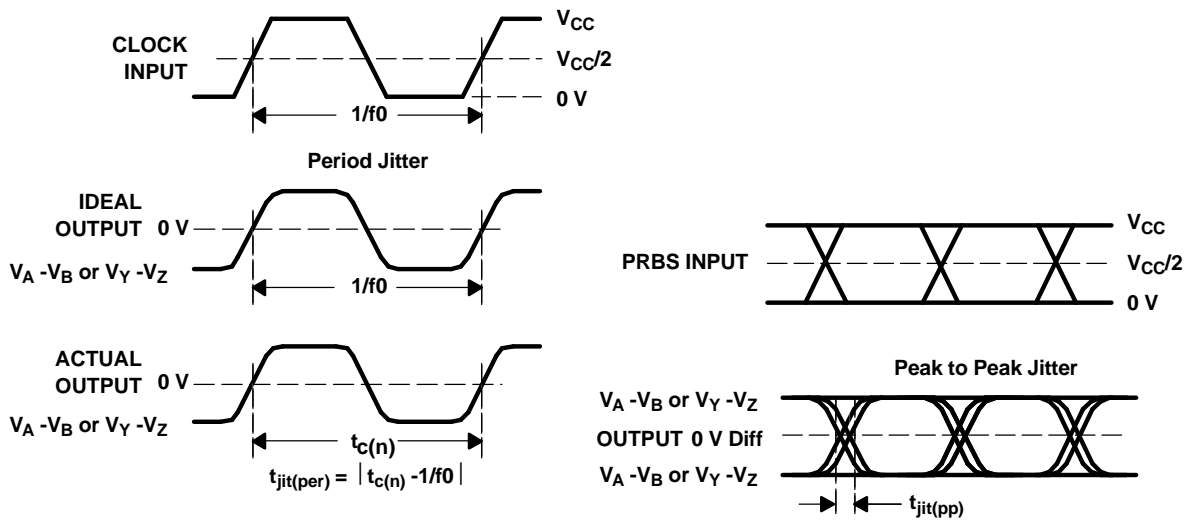
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
- C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
- D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

**PARAMETER MEASUREMENT INFORMATION (continued)**

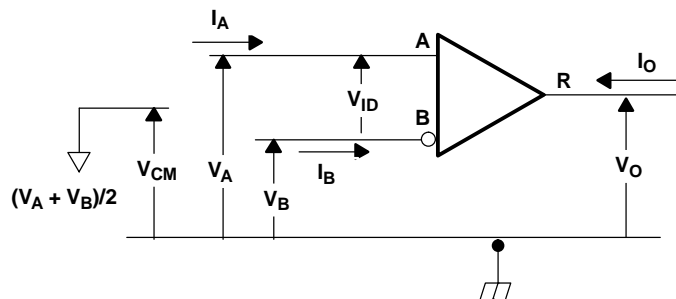


**Figure 7. Maximum Steady State Output Voltage**



- A. All input pulses are supplied by an Agilent 81250 Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 50 MHz  $50 \pm 1\%$  duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 100Mbps  $2^{15}-1$  PRBS input.

**Figure 8. Driver Jitter Measurement Waveforms**



**Figure 9. Receiver Voltage and Current Definitions**

**Table 1. Type-1 Receiver Input Threshold Test Voltages**

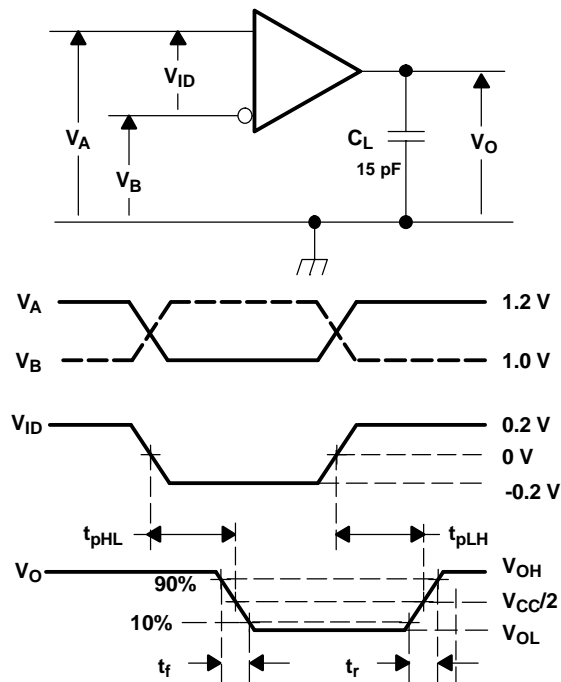
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER <sup>(1)</sup> OUTPUT
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.425	3.335	0.050	3.4	H
3.375	3.425	-0.050	3.4	L
-0.975	-1.025	0.050	-1	H
-1.025	-0.975	-0.050	-1	L

(1) H= high level, L = low level, output state assumes receiver is enabled ( $\overline{RE} = L$ )

**Table 2. Type-2 Receiver Input Threshold Test Voltages**

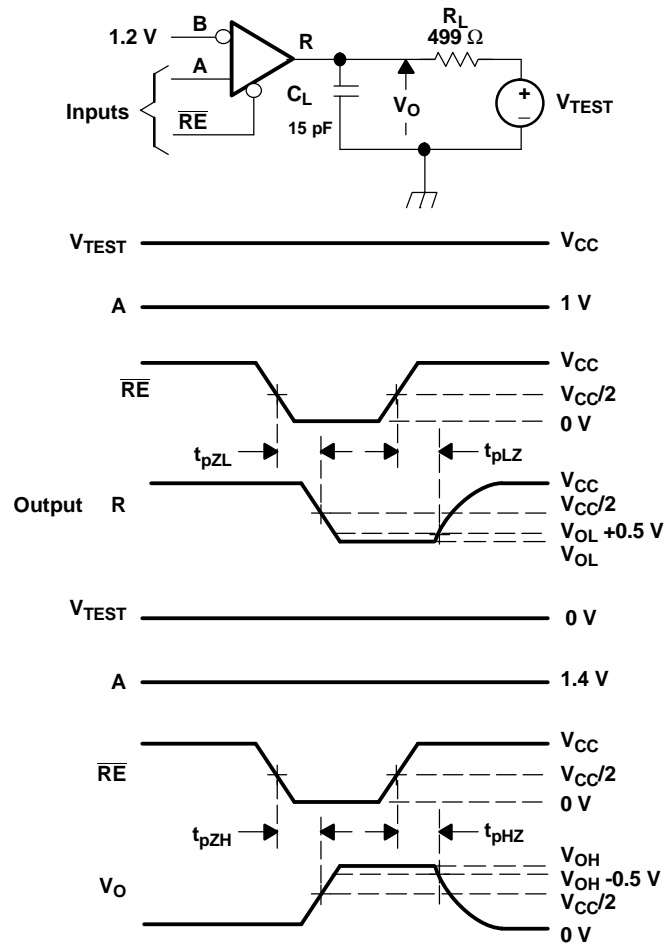
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER <sup>(1)</sup> OUTPUT
$V_{IA}$	$V_{IB}$	$V_{ID}$	$V_{IC}$	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.475	3.325	0.150	3.4	H
3.425	3.375	0.050	3.4	L
-0.925	-1.075	0.150	-1	H
-0.975	-1.025	0.050	-1	L

(1) H= high level, L = low level, output state assumes receiver is enabled ( $\overline{RE} = L$ )



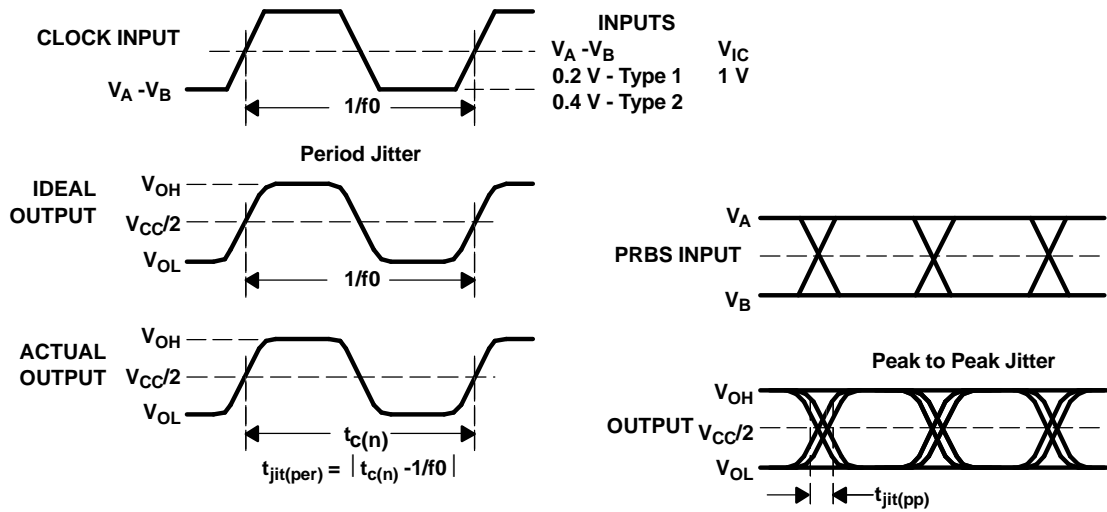
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .  $C_L$  is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
- B. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

**Figure 10. Receiver Timing Test Circuit and Waveforms**



- All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 1 MHz, duty cycle =  $50 \pm 5\%$ .
- $R_L$  is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
- $C_L$  is the instrumentation and fixture capacitance within 2 cm of the DUT and  $\pm 20\%$ .

**Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms**

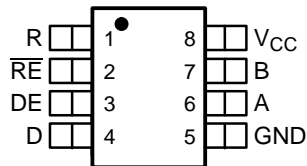


- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
- C. Period jitter is measured using a 50 MHz 50 ±1% duty cycle clock input.
- D. Peak-to-peak jitter is measured using a 100 Mbps 2<sup>15</sup>-1 PRBS input.

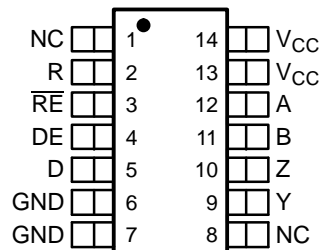
**Figure 12. Receiver Jitter Measurement Waveforms**

### PIN ASSIGNMENTS

SN65MLVD200AD (Marked as MF200A)  
 SN65MLVD204AD (Marked as MF204A)  
 (TOP VIEW)



SN65MLVD202AD (Marked as MLVD202A)  
 SN65MLVD205AD (Marked as MLVD205A)  
 (TOP VIEW)



NC - No internal connection

DEVICE FUNCTION TABLES

TYPE-1 RECEIVER (200A, 202A)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50 \text{ mV}$	L	H
$-50 \text{ mV} < V_{ID} < 50 \text{ mV}$	L	?
$V_{ID} \leq -50 \text{ mV}$	L	L
X	H	Z
X	Open	Z
Open Circuit	L	?

TYPE-2 RECEIVER (204A, 205A)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 150 \text{ mV}$	L	H
$50 \text{ mV} < V_{ID} < 150 \text{ mV}$	L	?
$V_{ID} \leq 50 \text{ mV}$	L	L
X	H	Z
X	Open	Z
Open Circuit	L	L

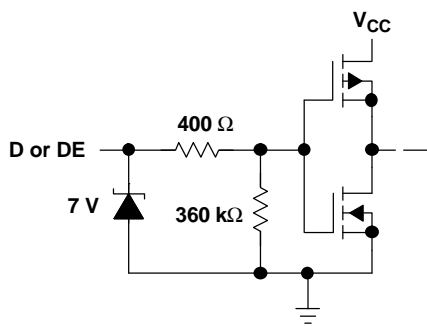
DRIVER

INPUT	ENABLE	OUTPUTS	
		A OR Y	B OR Z
D	DE	A OR Y	B OR Z
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

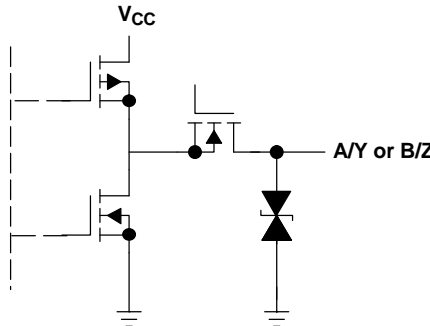
H = high level, L = low level, Z = high impedance, X = Don't care, ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

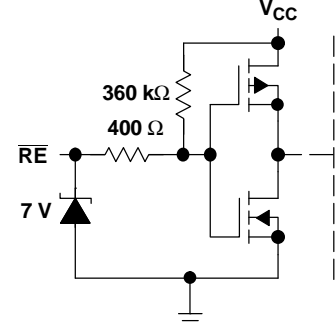
DRIVER INPUT AND DRIVER ENABLE



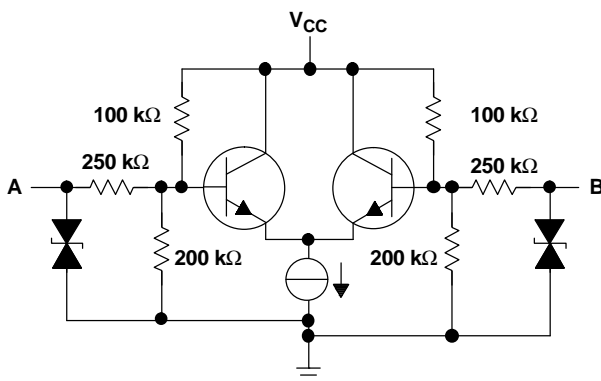
DRIVER OUTPUT



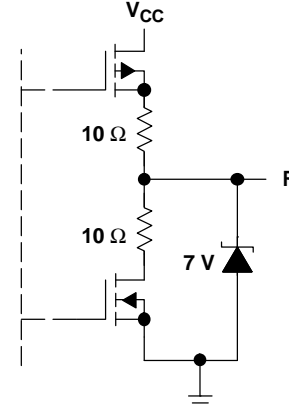
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



TYPICAL CHARACTERISTICS

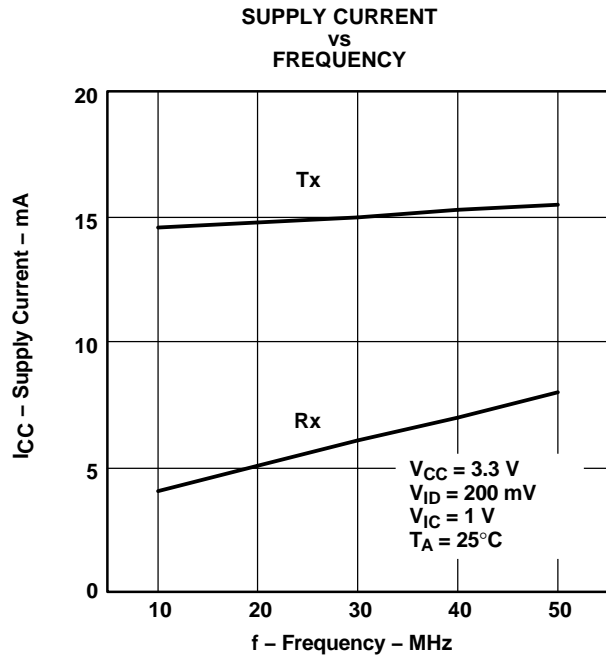


Figure 13.

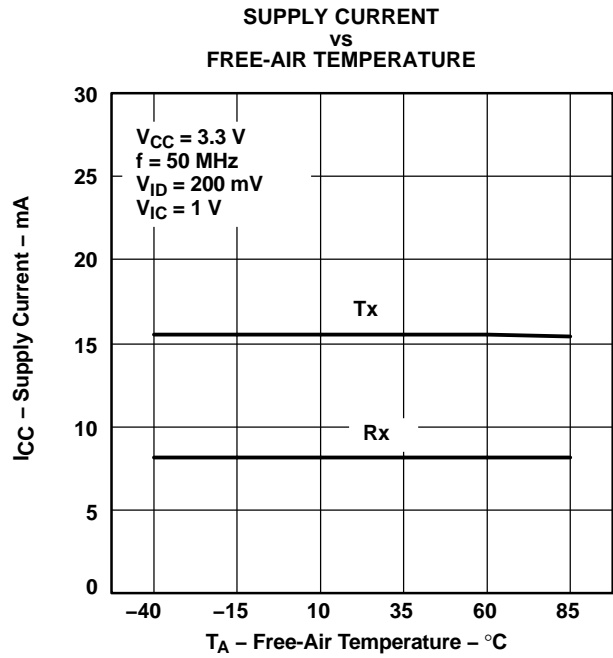


Figure 14.

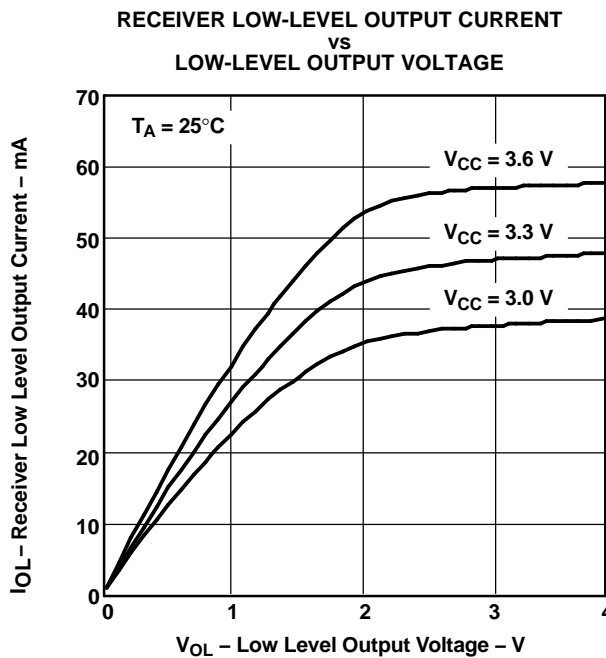


Figure 15.

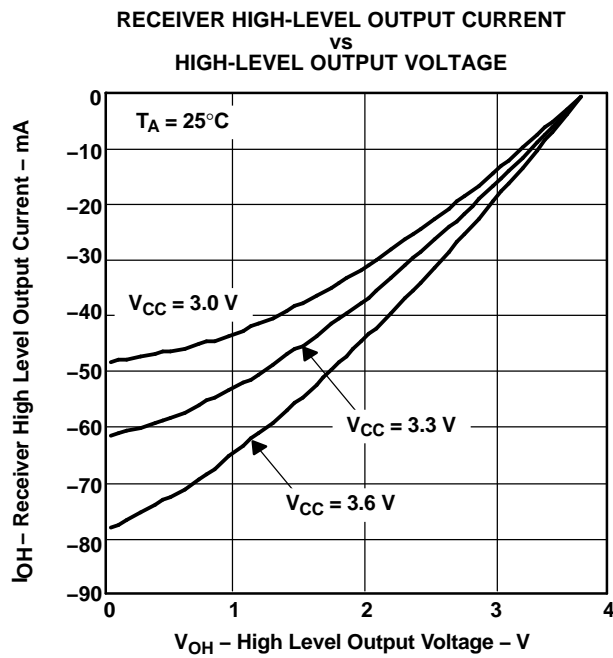


Figure 16.

**TYPICAL CHARACTERISTICS (continued)**

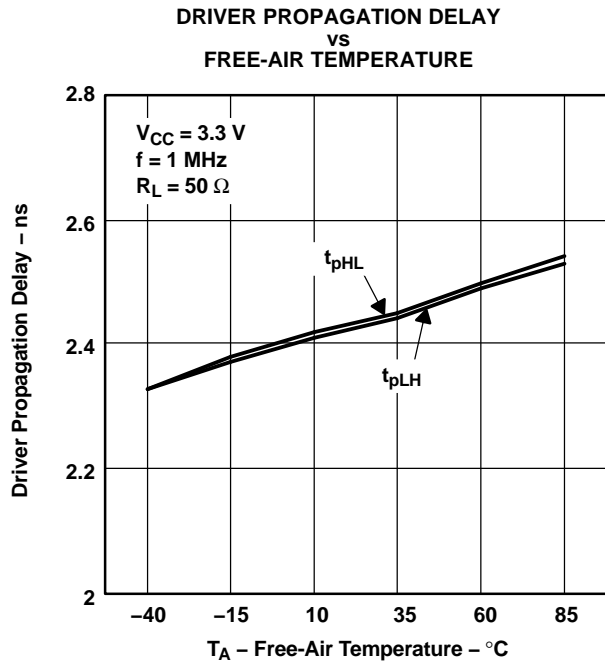


Figure 17.

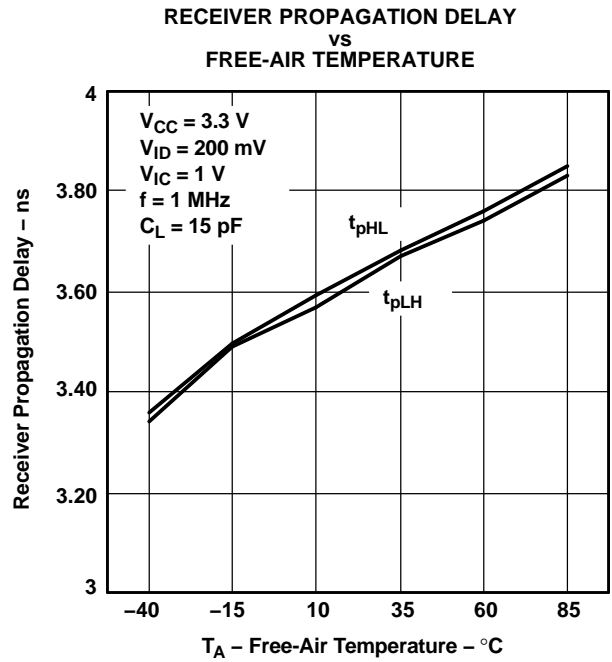


Figure 18.

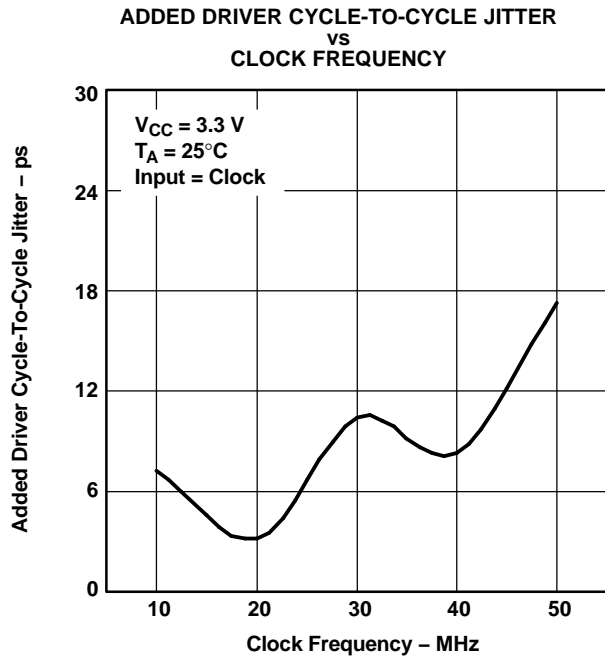


Figure 19.

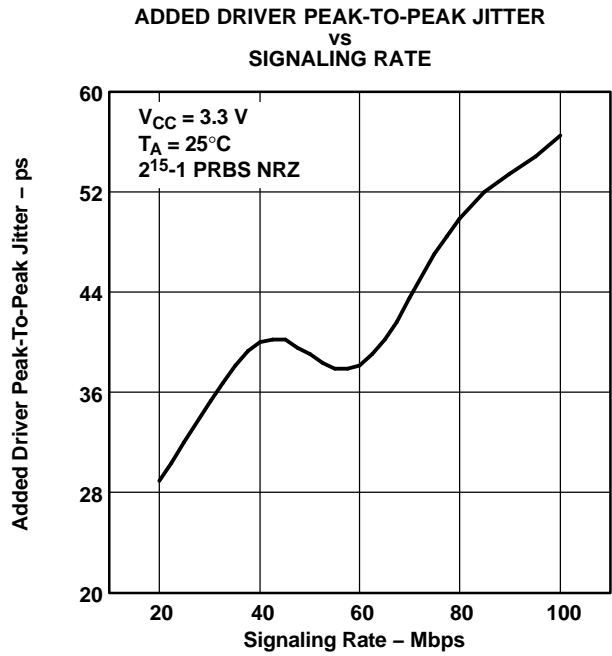


Figure 20.

TYPICAL CHARACTERISTICS (continued)

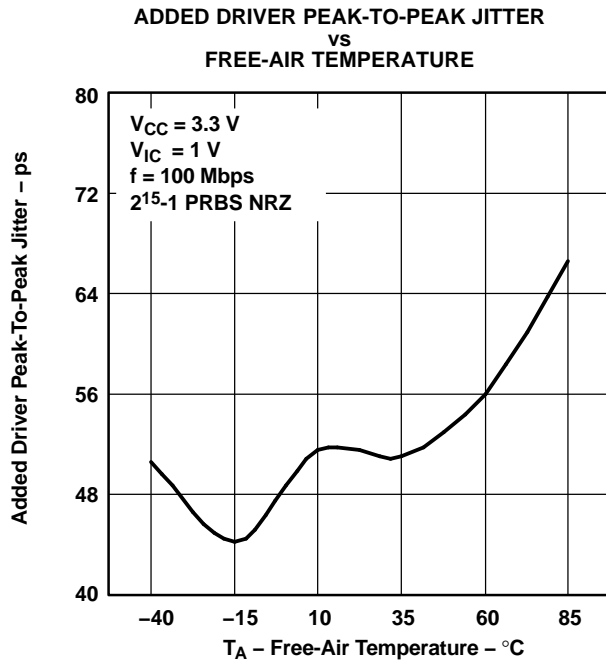


Figure 21.

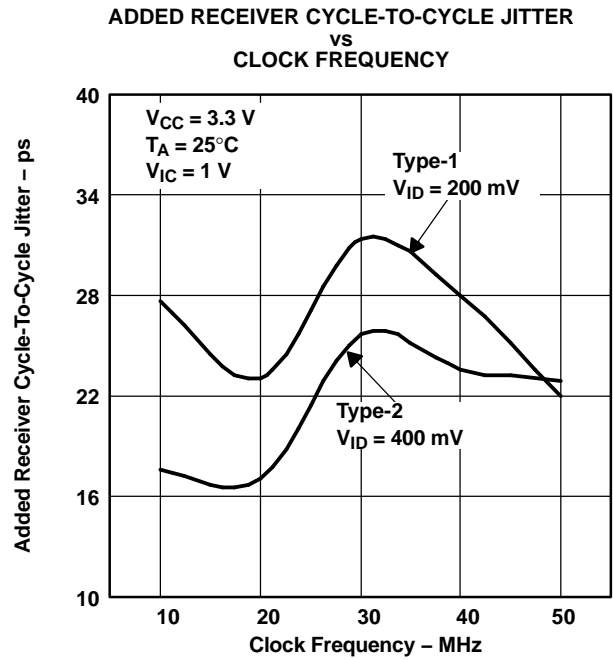


Figure 22.

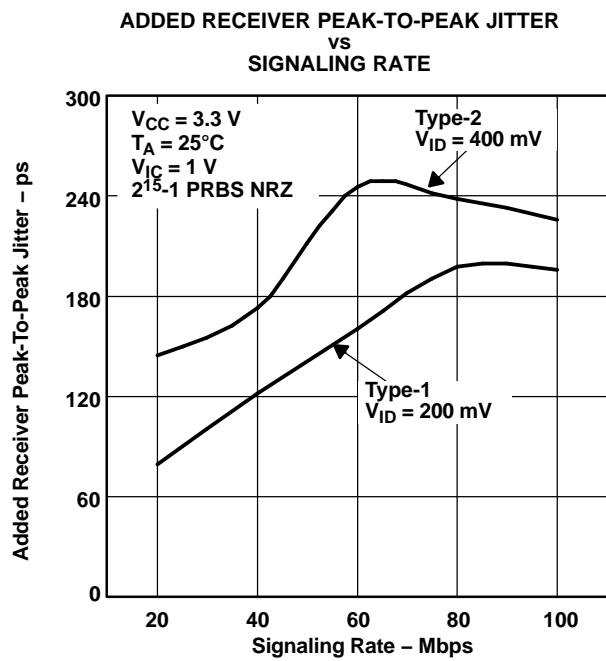


Figure 23.

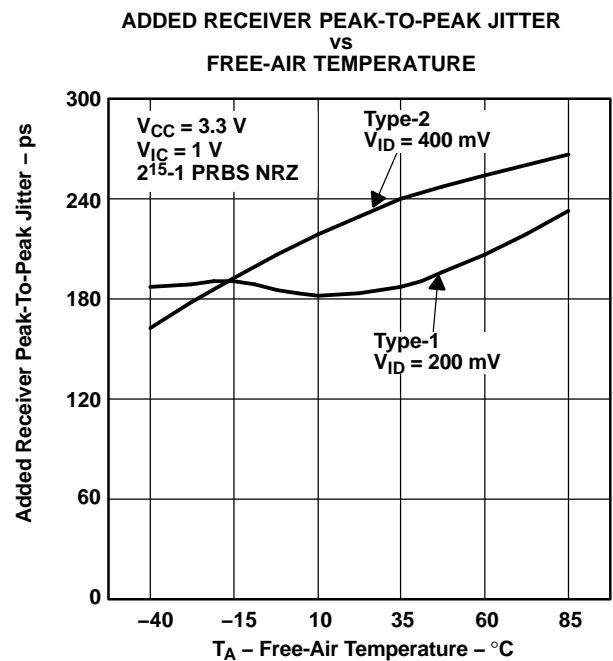
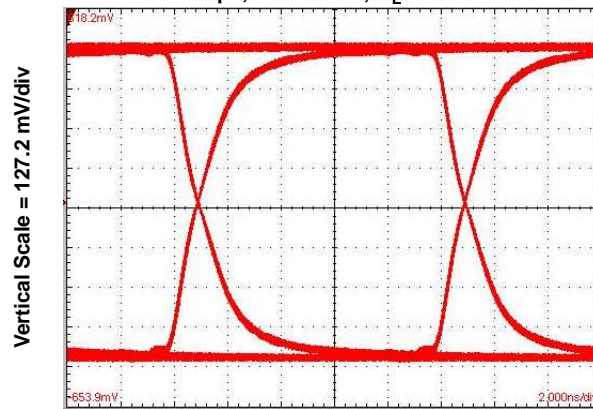


Figure 24.

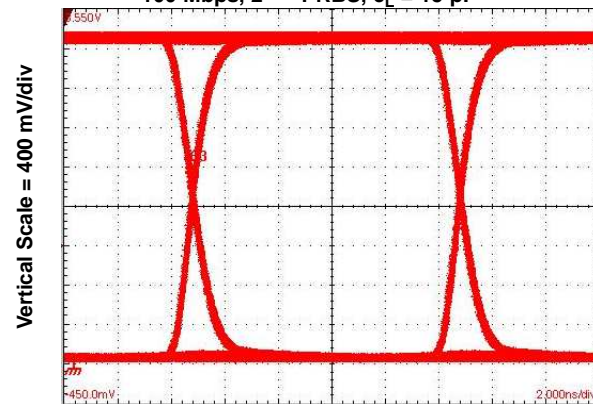
### TYPICAL CHARACTERISTICS (continued)

SN65MLVD200A DRIVER OUTPUT EYE PATTERN  
vs  
100 Mbps,  $2^{15-1}$  PRBS,  $R_L = 50 \Omega$



Horizontal Scale = 2 ns/div  
Figure 25.

SN65MLVD200A RECEIVER OUTPUT EYE PATTERN  
vs  
100 Mbps,  $2^{15-1}$  PRBS,  $c_L = 15 \text{ pF}$



Horizontal Scale = 2 ns/div  
Figure 26.

**APPLICATION INFORMATION**

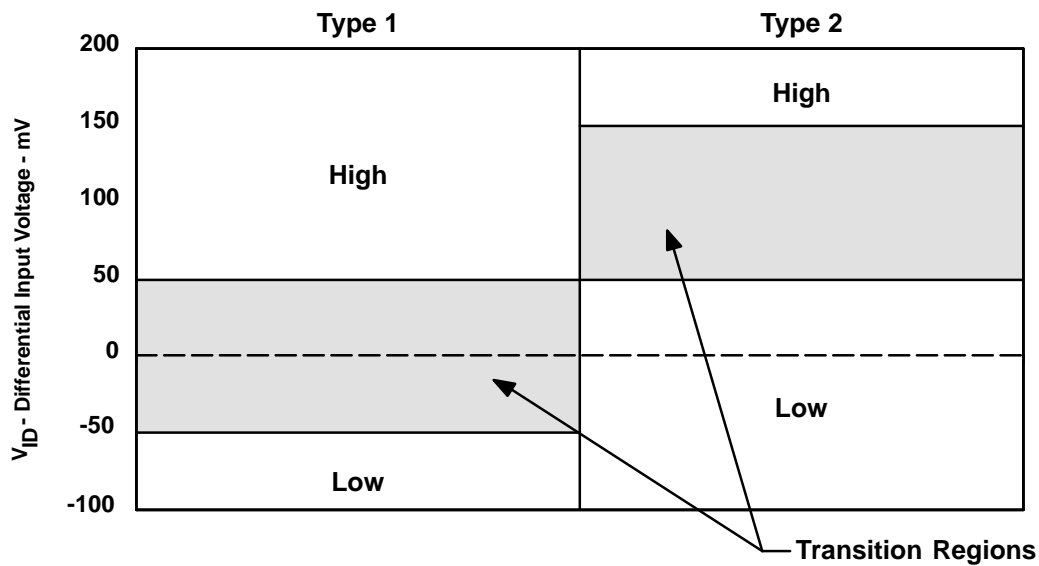
**COMPARISON OF MLVD TO TIA/EIA-485**

**Receiver Input Threshold (Failsafe)**

The MLVD standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in [Table 3](#) and [Figure 27](#).

**Table 3. Receiver Input Voltage Threshold Requirements**

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\text{ V} \leq V_{ID} \leq -0.05\text{ V}$	$0.05\text{ V} \leq V_{ID} \leq 2.4\text{ V}$
Type 2	$-2.4\text{ V} \leq V_{ID} \leq 0.05\text{ V}$	$0.15\text{ V} \leq V_{ID} \leq 2.4\text{ V}$



**Figure 27. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD200AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	<a href="#">Samples</a>
SN65MLVD200ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	<a href="#">Samples</a>
SN65MLVD200ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	<a href="#">Samples</a>
SN65MLVD200ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF200A	<a href="#">Samples</a>
SN65MLVD202AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD202A	<a href="#">Samples</a>
SN65MLVD202ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD202A	<a href="#">Samples</a>
SN65MLVD202ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD202A	<a href="#">Samples</a>
SN65MLVD204AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	<a href="#">Samples</a>
SN65MLVD204ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	<a href="#">Samples</a>
SN65MLVD204ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	<a href="#">Samples</a>
SN65MLVD204ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MF204A	<a href="#">Samples</a>
SN65MLVD205AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD205A	<a href="#">Samples</a>
SN65MLVD205ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD205A	<a href="#">Samples</a>
SN65MLVD205ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MLVD205A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

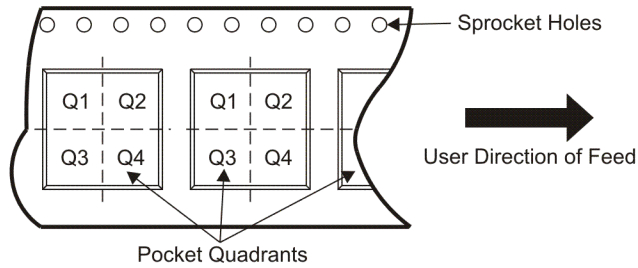
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**TAPE AND REEL INFORMATION**



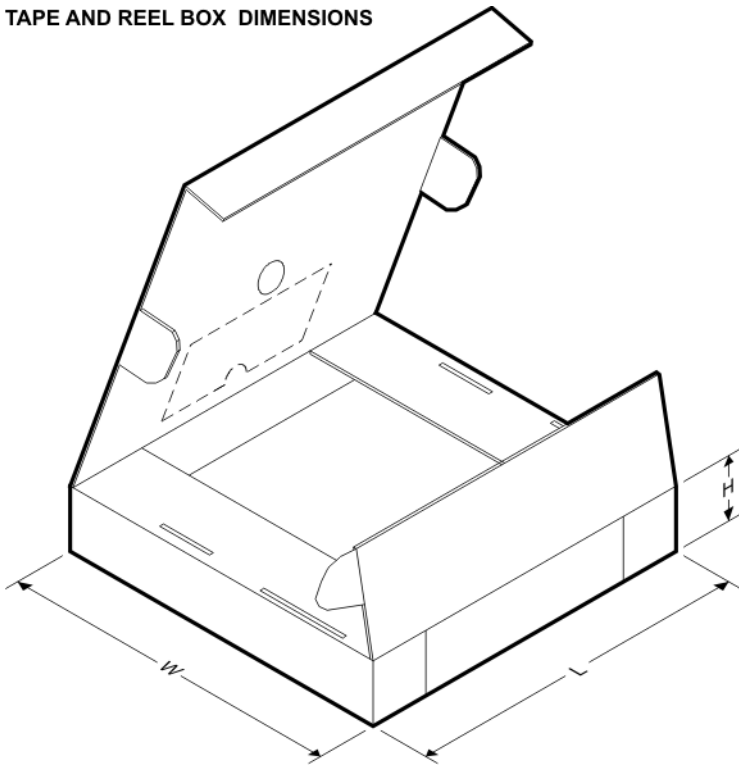
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD200ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD202ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65MLVD204ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65MLVD205ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

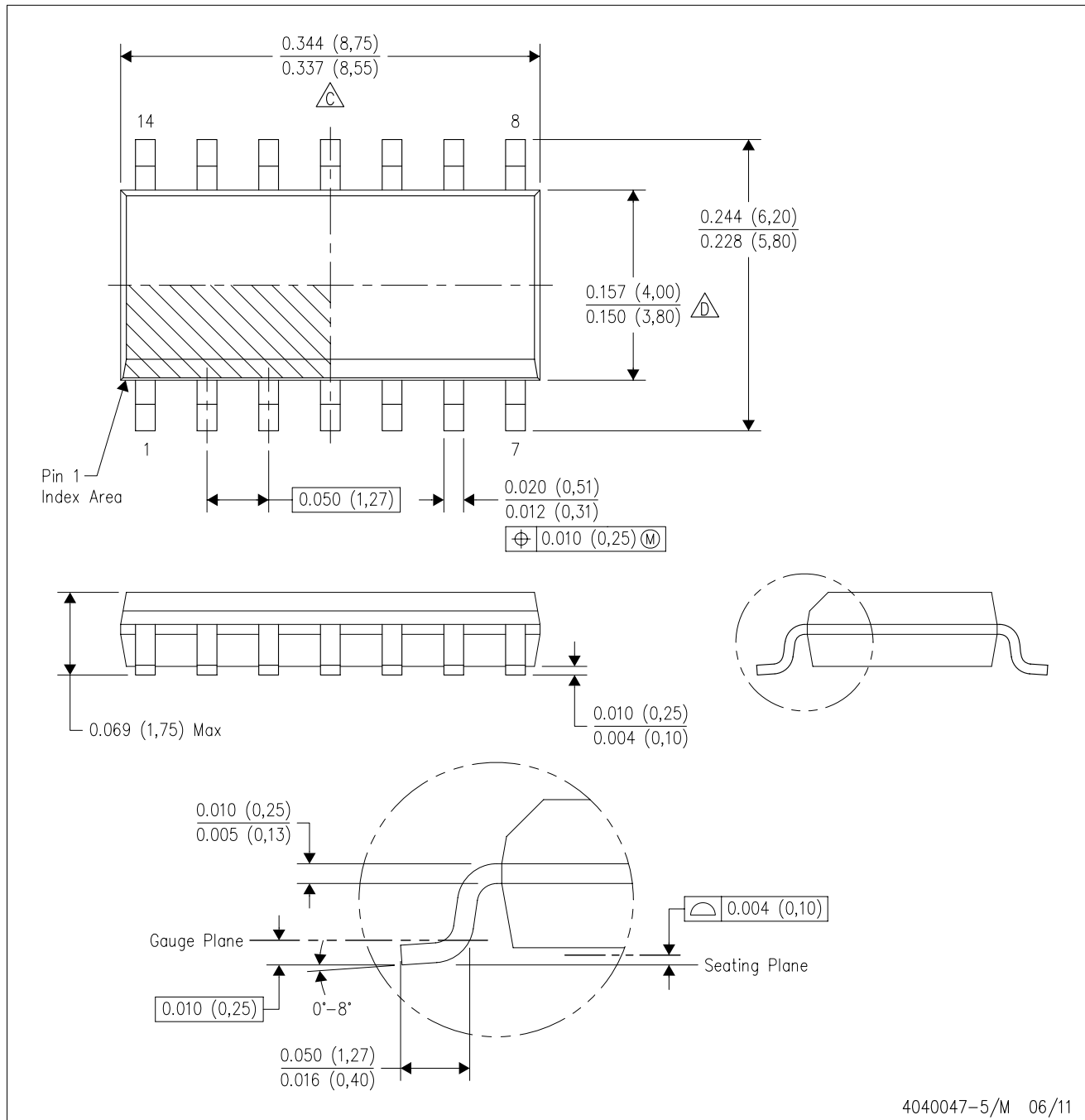


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD200ADR	SOIC	D	8	2500	340.5	338.1	20.6
SN65MLVD202ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN65MLVD204ADR	SOIC	D	8	2500	340.5	338.1	20.6
SN65MLVD205ADR	SOIC	D	14	2500	333.2	345.9	28.6

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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