

HIGH-SPEED DIFFERENTIAL LINE DRIVER/RECEIVERS

FEATURES

- Meets or Exceeds the ANSI TIA/EIA-644A Standard
- Designed for Signaling Rates

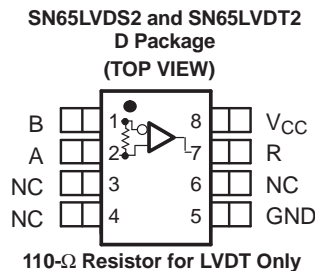
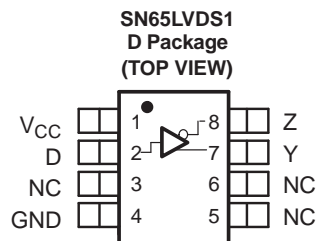
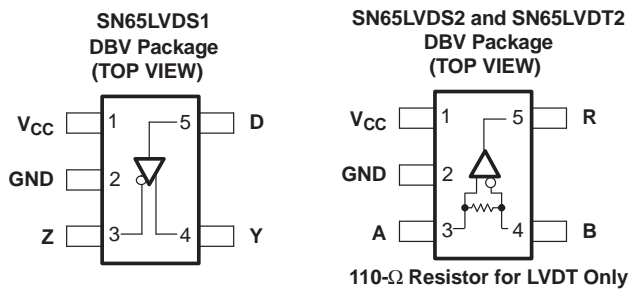
The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

up to:

- 630 Mbps Drivers
- 400 Mbps Receivers
- Operates From a 2.4-V to 3.6-V Supply
- Available in SOT-23 and SOIC Packages
- Bus-Terminal ESD Exceeds 9 kV
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV Into a 100-Ω Load
- Propagation Delay Times
 - 1.7 ns Typical Driver
 - 2.5 ns Typical Receiver
- Power Dissipation at 200 MHz
 - 25 mW Typical Driver
 - 60 mW Typical Receiver
- LVDT Receiver Includes Line Termination
- Low Voltage TTL (LVTTTL) Level Driver Input Is 5-V Tolerant
- Driver Is Output High Impedance With $V_{CC} < 1.5 V$
- Receiver Output and Inputs Are High Impedance With $V_{CC} < 1.5 V$
- Receiver Open-Circuit Fail Safe
- Differential Input Voltage Threshold Less Than 100 mV

DESCRIPTION

The SN65LVDS1, SN65LVDS2, and SN65LVDT2 are single, low-voltage, differential line drivers and receivers in the small-outline transistor package. The outputs comply with the TIA/EIA-644A standard and provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load at signaling rates up to 630 Mbps for drivers and 400 Mbps for receivers.



AVAILABLE OPTIONS

| PART NUMBER | INTEGRATED TERMINATION | PACKAGE | PACKAGE MARKING |
|--------------|------------------------|---------|-----------------|
| SN65LVDS1DBV | | SOT23-5 | SAAI |
| SN65LVDS1D | | SOIC-8 | LVDS1 |
| SN65LVDS2DBV | | SOT23-5 | SABI |
| SN65LVDS2D | | SOIC-8 | LVDS2 |
| SN65LVDT2DBV | √ | SOT23-5 | SACI |
| SN65LVDT2D | √ | SOIC-8 | LVDT2 |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

When the SN65LVDS1 is used with an LVDS receiver (such as the SN65LVDT2) in a point-to-point connection, data or clocking signals can be transmitted over printed-circuit-board traces or cables at very high rates with very low electromagnetic emissions and power consumption. The packaging, low power, low EMI, high ESD tolerance, and wide supply voltage range make the device ideal for battery-powered applications.

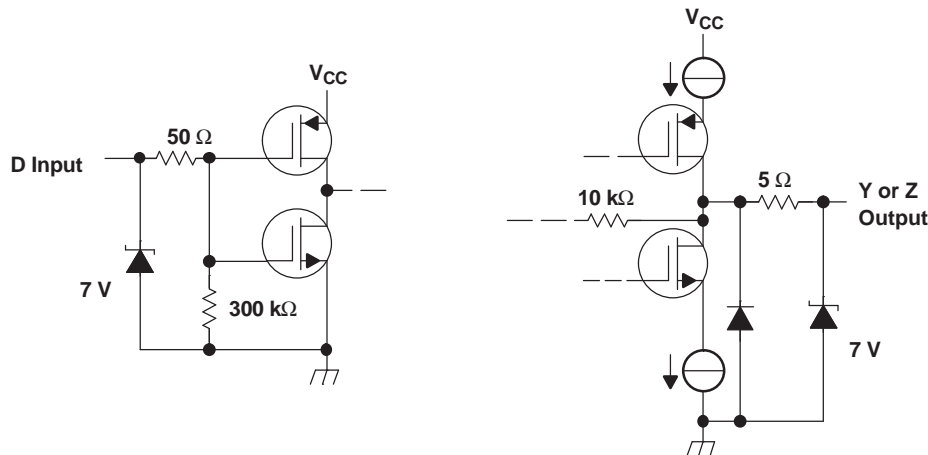
The SN65LVDS1, SN65LVDS2, and SN65LVDT2 are characterized for operation from -40°C to 85°C .

FUNCTION TABLES

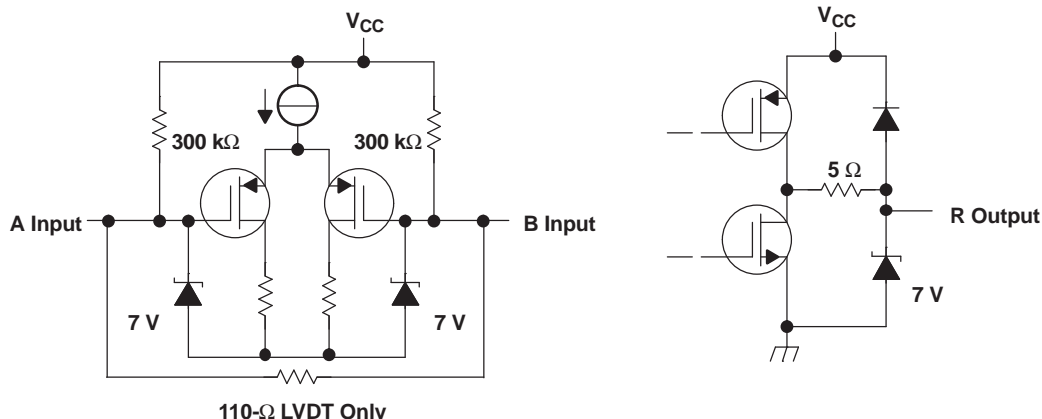
| DRIVER | | | RECEIVER | |
|--------|---------|---|---|--------|
| INPUT | OUTPUTS | | INPUTS | OUTPUT |
| D | Y | Z | $V_{ID} = V_A - V_B$ | R |
| H | H | L | $V_{ID} \geq 100 \text{ mV}$ | H |
| L | L | H | $-100 \text{ mV} < V_{ID} < 100 \text{ mV}$ | ? |
| Open | L | H | $V_{ID} \leq -100 \text{ mV}$ | L |
| | | | Open | H |

H = high level, L = low level, ? = indeterminate

DRIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



RECEIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | RATINGS |
|--|-----------------------|------------------------------|
| Supply voltage range, V_{CC} ⁽²⁾ | | -0.5 V to 4 V |
| Input voltage range, V_I | (A or B) | -0.5 V to 4 V |
| | (D) | -0.5 V to $V_{CC} + 2$ V |
| Output voltage, V_O | (Y or Z) | -0.5 V to 4 V |
| Differential input voltage magnitude, $ V_{ID} $ | SN65LVDT2 only | 1 V |
| Receiver output current, I_O | | -12 mA to 12 mA |
| Human-body model electrostatic discharge, HBM ESD ⁽³⁾ | | |
| | All pins | 4000 V |
| | Bus pins (A, B, Y, Z) | 9000 V |
| Machine-model electrostatic discharge, MM ESD ⁽⁴⁾ | | 400 V |
| Field-induced-charge device model electrostatic discharge, FCDM ESD ⁽⁵⁾ | | 1500 V |
| Continuous total power dissipation, P_D | | See Dissipation Rating Table |
| Storage Temperature Range (non operating) | | -65°C to 150°C |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
- (3) Test method based upon JEDEC Standard 22, Test Method A114-A. Bus pins stressed with respect to GND and V_{CC} separately.
- (4) Test method based upon JEDEC Standard 22, Test Method A114-A.
- (5) Test method based upon EIA-JEDEC JESD22-C101C.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ ⁽¹⁾ | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---|--|--|
| D | 725 mW | 5.8 mW/°C | 402 mW |
| DBV | 385 mW | 3.1 mW/°C | 200 mW |

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-K) and with no air flow.

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | MIN | NOM | MAX | UNIT |
|------------|---|-----|-----|--------------|------|
| V_{CC} | Supply voltage | 2.4 | 3.3 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | 5 | V |
| V_{IL} | Low-level input voltage | 0 | | 0.8 | V |
| T_A | Operating free-air temperature | –40 | | 85 | °C |
| $ V_{ID} $ | Magnitude of differential input voltage | 0.1 | | 0.6 | V |
| | Input voltage (any combination of input or common-mode voltage) | 0 | | $V_{CC}-0.8$ | V |

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX | UNIT |
|----------------------|--|--|--------------------|--------------------|-------|------|
| V _{OD} | Differential output voltage magnitude | R _L = 100 Ω, 2.4 ≤ V _{CC} <3 V | 200 | 350 | 454 | mV |
| | | R _L = 100 Ω, 3 ≤ V _{CC} <3.6 V | 247 | 350 | 454 | |
| Δ V _{OD} | Change in differential output voltage magnitude between logic states | See Figure 2 | –50 | | 50 | |
| V _{OC(SS)} | Steady-state common-mode output voltage | See Figure 2 | 1.125 | | 1.375 | V |
| ΔV _{OC(SS)} | Change in steady-state common-mode output voltage between logic states | | –50 | | 50 | mV |
| V _{OC(PP)} | Peak-to-peak common-mode output voltage | | | 25 | | 100 |
| I _{CC} | Supply current | V _I = 0 V or V _{CC} , No load | | 2 | 4 | mA |
| | | V _I = 0 V or V _{CC} , R _L = 100 Ω | | 5.5 | 8 | |
| I _{IH} | High-level input current | V _{IH} = 5 V | | 2 | 20 | μA |
| I _{IL} | Low-level input current | V _{IL} = 0.8 V | | 2 | 10 | μA |
| I _{OS} | Short-circuit output current | V _{OY} or V _{OZ} = 0 V | | 3 | 10 | mA |
| | | V _{OD} = 0 V | | | 10 | |
| I _{O(OFF)} | Power-off output current | V _{CC} = 1.5 V, V _O = 3.6 V | –1 | | 1 | μA |
| C _i | Input capacitance | V _I = 0.4 Sin (4E6πt)+0.5 V | | 3 | | pF |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------|--|---|-----|--------------------|-----|------|
| t _{PLH} | Propagation delay time, low-to-high-level output | R _L = 100 Ω, C _L = 10 pF, See Figure 5 | | 1.5 | 3.1 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | | | 1.8 | 3.1 | ns |
| t _r | Differential output signal rise time | | | 0.6 | 1 | ns |
| t _f | Differential output signal fall time | | | 0.7 | 1 | ns |
| t _{sk(p)} | Pulse skew (t _{PHL} - t _{PLH}) ⁽²⁾ | | | 0.3 | | ns |

(1) All typical values are at 25°C and with a 3.3-V supply.

 (2) t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN ⁽¹⁾ | TYP ⁽²⁾ | MAX | UNIT | |
|---------------------|---|--|--|--------------------|-----|------|----|
| V _{ITH+} | Positive-going differential input voltage threshold | See Figure 3 | | | 100 | mV | |
| V _{ITH-} | Negative-going differential input voltage threshold | | -100 | | | | |
| V _{OH} | High-level output voltage | I _{OH} = -8 mA, V _{CC} = 2.4 V | 1.9 | | | V | |
| | | I _{OH} = -8 mA, V _{CC} = 3 V | 2.4 | | | | |
| V _{OL} | Low-level output voltage | I _{OL} = 8 mA | | 0.25 | 0.4 | V | |
| I _{CC} | Supply current | No load, Steady state | | 4 | 7 | mA | |
| I _I | Input current (A or B inputs) | LVDS2 | V _I = 0 V, other input = 1.2 V | -20 | | -2 | μA |
| | | | V _I = 2.2 V, other input = 1.2 V, V _{CC} = 3.0 V | | -3 | -1.2 | |
| | | LVDT2 | V _I = 0 V, other input open | -40 | | -4 | |
| | | | V _I = 2.2 V, other input open, V _{CC} = 3.0 V | | -6 | -2.4 | |
| I _{ID} | Differential input current (I _{IA} - I _{IB}) | LVDS2 | V _{IA} = 2.4 V V _{IB} = 2.3 V | -2 | | 2 | μA |
| I _{I(OFF)} | Power-off input current (A or B inputs) | LVDS2 | V _{CC} = 0 V, V _{IA} = V _{IB} = 2.4 V | | | 20 | μA |
| | | LVDT2 | V _{CC} = 0 V, V _{IA} = V _{IB} = 2.4 V | | | 40 | |
| R _T | Differential input resistance | LVDT2 | V _{IA} = 2.4 V V _{IB} = 2.2 V | 90 | 111 | 132 | Ω |
| C _I | Input Capacitance | | V _I = 0.4sin(4E6πt) + 0.5V | | | 5.8 | pF |
| C _O | Output Capacitance | | V _I = 0.4sin(4E6πt) + 0.5V | | | 3.4 | pF |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.

(2) All typical values are at 25°C and with a 2.7-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ₁ | MAX | UNIT |
|----------------------|--|--------------------------------------|-----|------------------|-----|------|
| t _{PLH} | Propagation delay time, low-to-high-level output | C _L = 10 pF, See Figure 6 | 1.4 | 2.6 | 3.6 | ns |
| t _{PHL} | Propagation delay time, high-to-low-level output | | 1.4 | 2.5 | 3.6 | ns |
| t _{sk(p)} | Pulse skew (t _{pHL} - t _{pLH}) ⁽²⁾ | | 0.1 | 0.6 | | ns |
| t _r | Output signal rise time | | 0.8 | 1.4 | | ns |
| t _f | Output signal fall time | | 0.8 | 1.4 | | ns |
| t _{r(slew)} | Output slew rate (rising) | V _{CC} = 3.0 V - 3.6 V | 2.2 | 3 | 5.5 | V/ns |
| | | V _{CC} = 2.4 V - 2.7 V | 1.5 | 1.9 | 2.9 | V/ns |
| t _{f(slew)} | Output slew rate (falling) | V _{CC} = 3.0 V - 3.6 V | 2.7 | 3.8 | 6 | V/ns |
| | | V _{CC} = 2.4 V - 2.7 V | 2.1 | 2.3 | 3.9 | V/ns |

(1) All typical values are at 25°C and with a 2.7-V supply.

(2) t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

PARAMETER MEASUREMENT INFORMATION

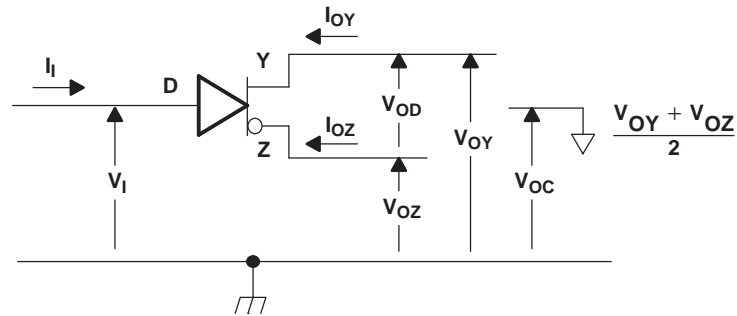
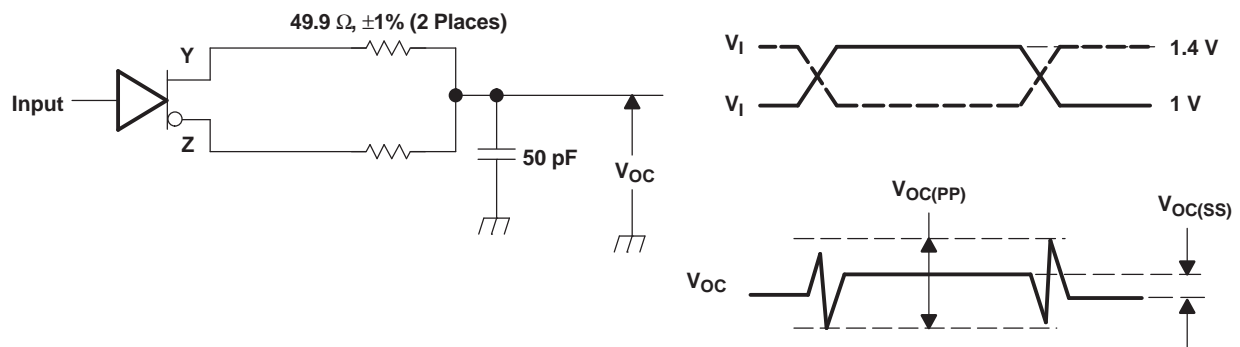


Figure 1. Driver Voltage and Current Definitions



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 2. Driver Test Circuit and Definitions for the Driver Common-Mode Output Voltage

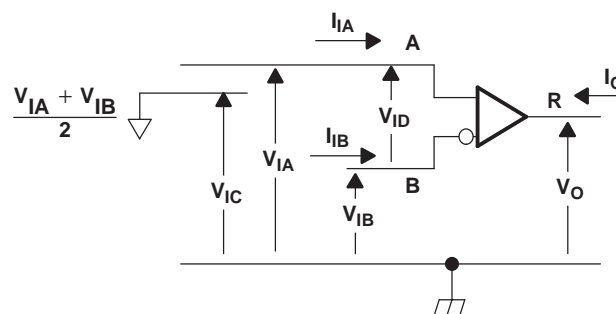
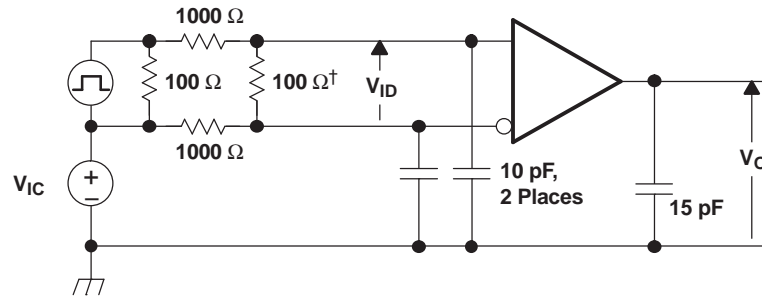


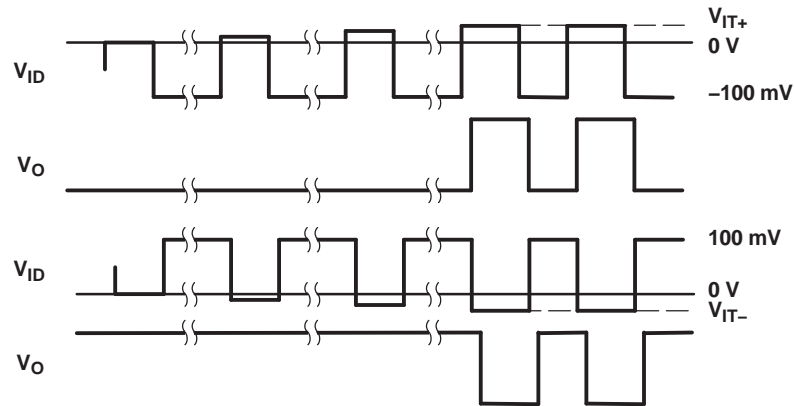
Figure 3. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



† Remove for testing LVDT device.

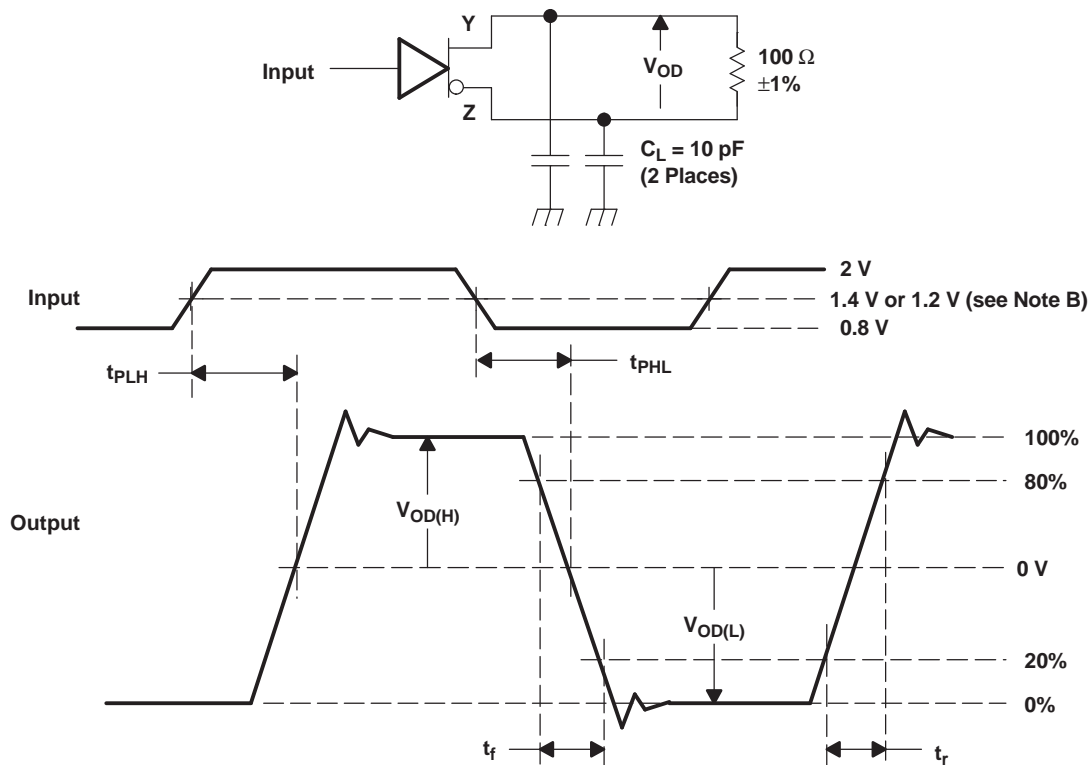
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of < 1 ns.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of < 1 ns.

Figure 4. V_{IT+} and V_{IT-} Input Voltage Threshold Test Circuit and Definitions

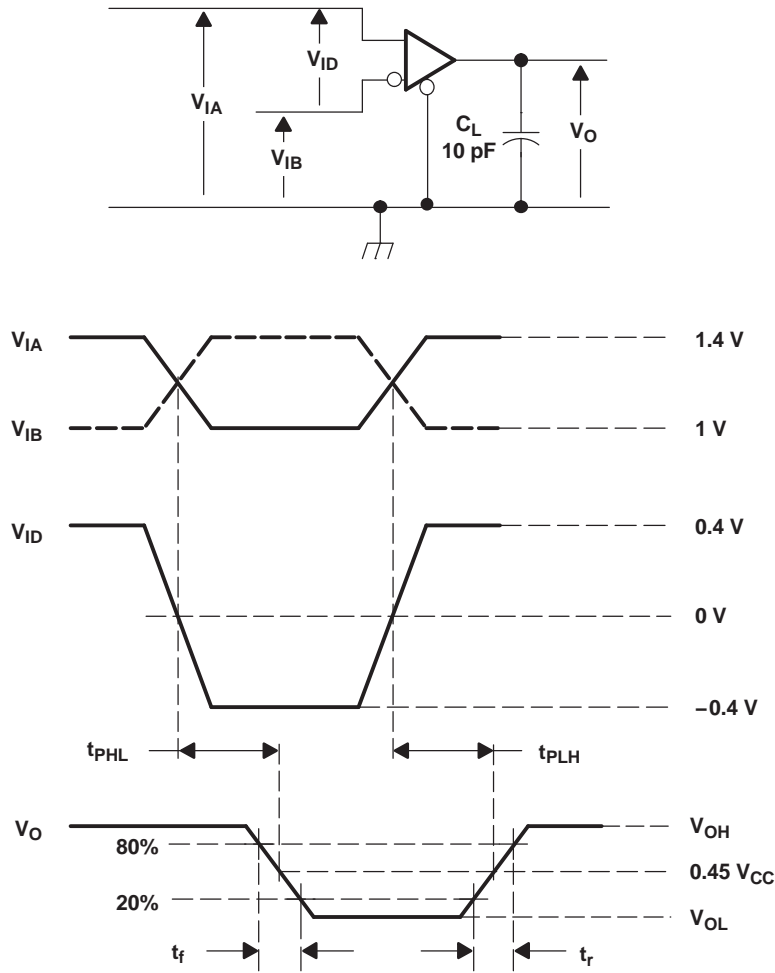
PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.
- B. This point is 1.4 V with $V_{CC} = 3.3$ V or 1.2 V with $V_{CC} = 2.7$ V.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Receiver Timing Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

DRIVER HIGH-TO-LOW LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

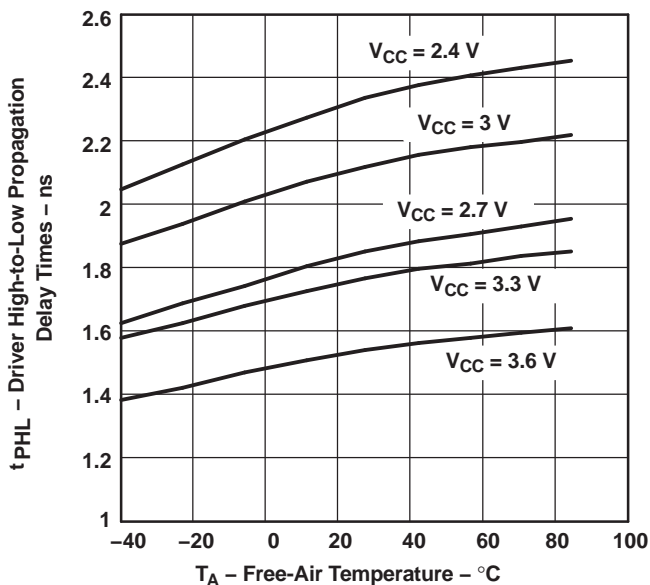


Figure 7.

DRIVER LOW-TO-HIGH LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

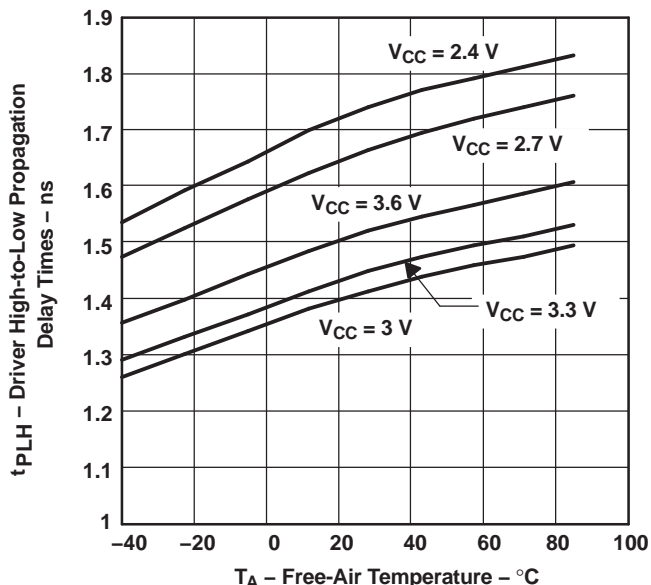


Figure 8.

RECEIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

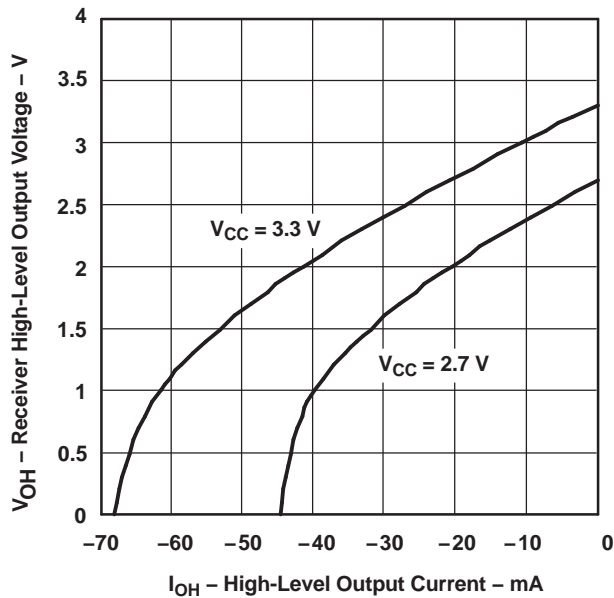


Figure 9.

RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

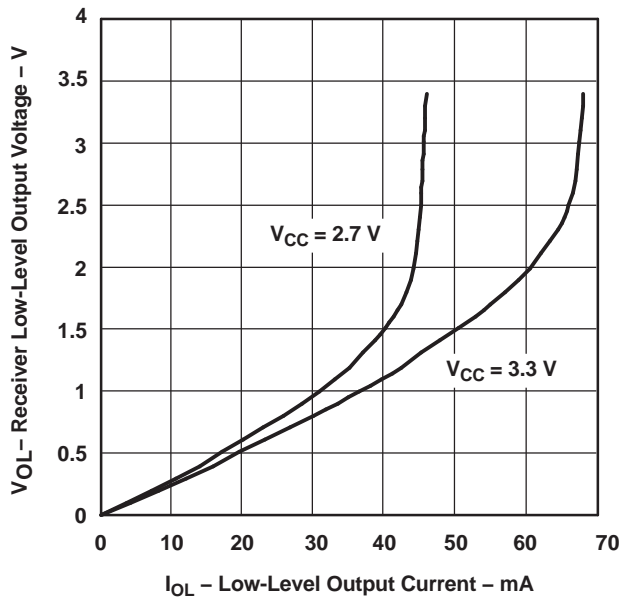


Figure 10.

TYPICAL CHARACTERISTICS (continued)

RECEIVER HIGH-TO-LOW LEVEL
 PROPAGATION DELAY TIMES
 vs
 FREE-AIR TEMPERATURE

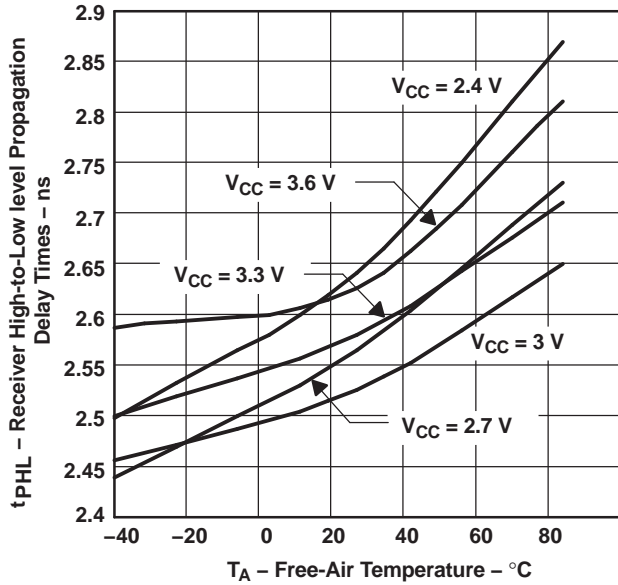


Figure 11.

RECEIVER LOW-TO-HIGH LEVEL
 PROPAGATION DELAY TIMES
 vs
 FREE-AIR TEMPERATURE

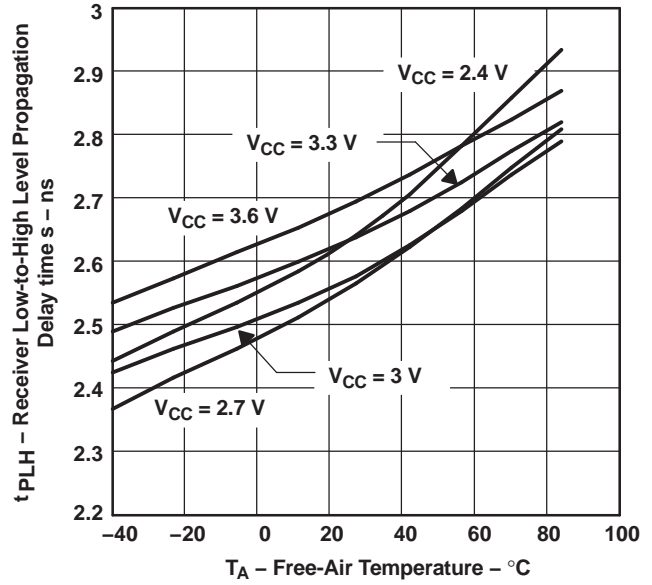


Figure 12.

RISE/FALL TIME
 vs
 CAPACITIVE LOAD

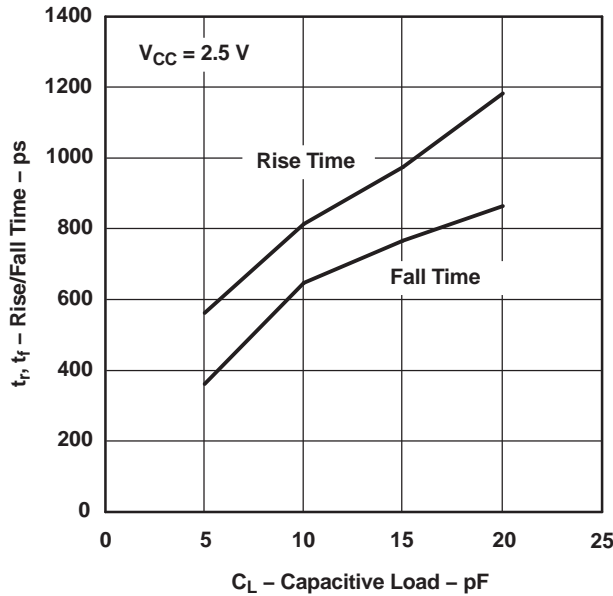


Figure 13.

RISE/FALL TIME
 vs
 CAPACITIVE LOAD

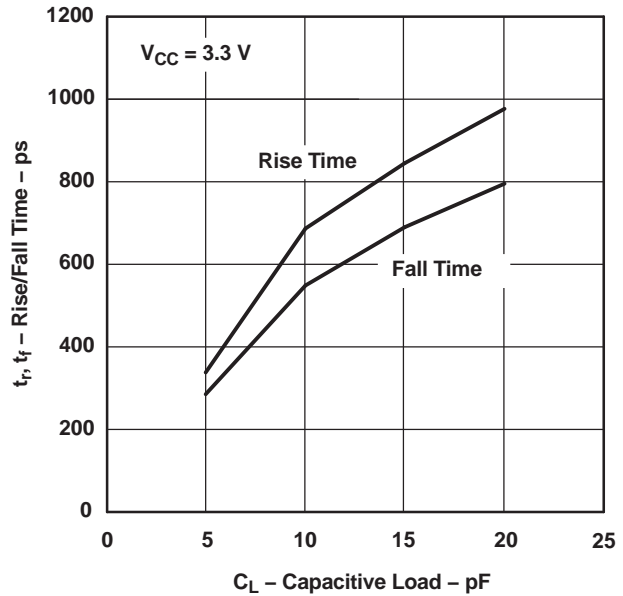


Figure 14.

APPLICATION INFORMATION

FAIL-SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV and within its recommended input common-mode voltage range. However, TI's LVDS receiver is different in how it handles the open-input circuit situation.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors as shown in Figure 15. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level regardless of the differential input voltage.

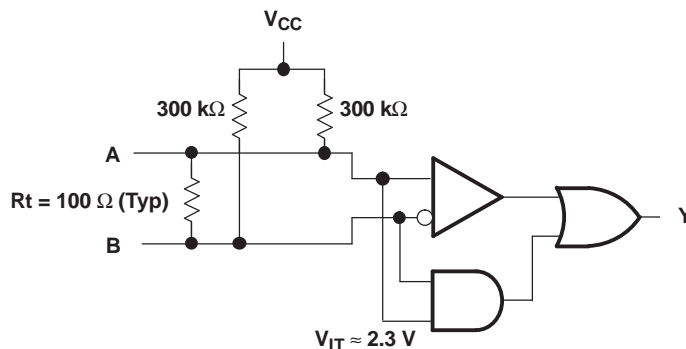


Figure 15. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

Parallel Terminated



Point to Point



Multidrop

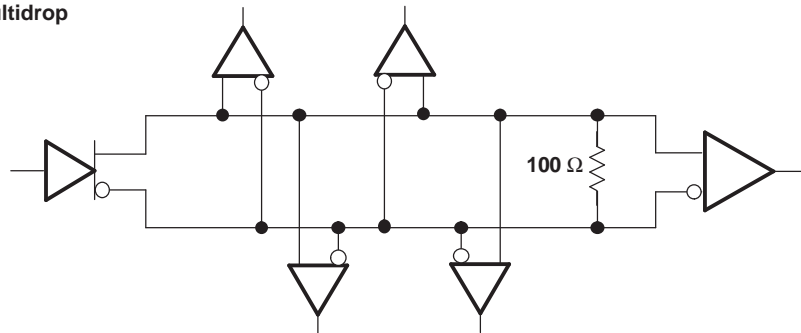


Figure 16. Typical Application Circuits

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN65LVDS1D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS1DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS2DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDT2DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

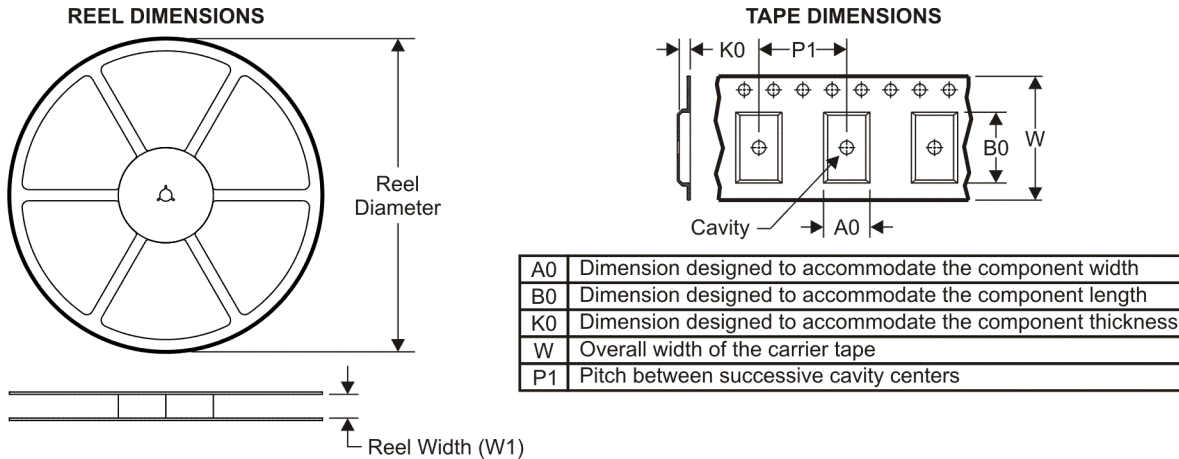
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

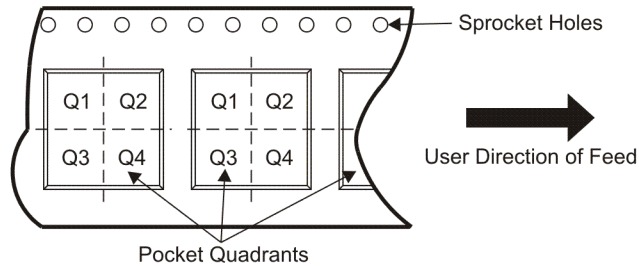
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TAPE AND REEL INFORMATION



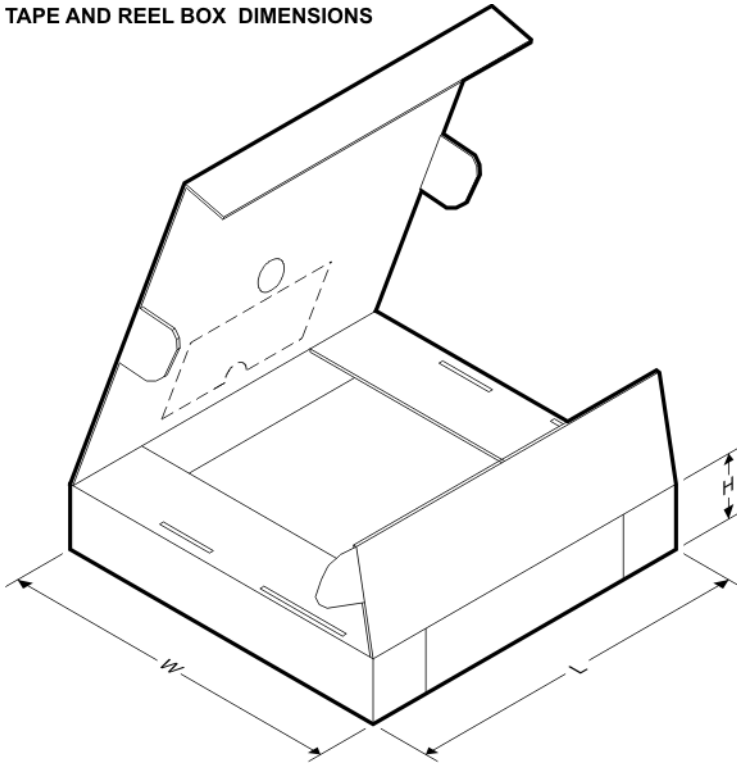
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LVDS1DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN65LVDS1DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN65LVDS1DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65LVDS2DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN65LVDS2DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN65LVDS2DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN65LVDT2DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN65LVDT2DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN65LVDT2DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

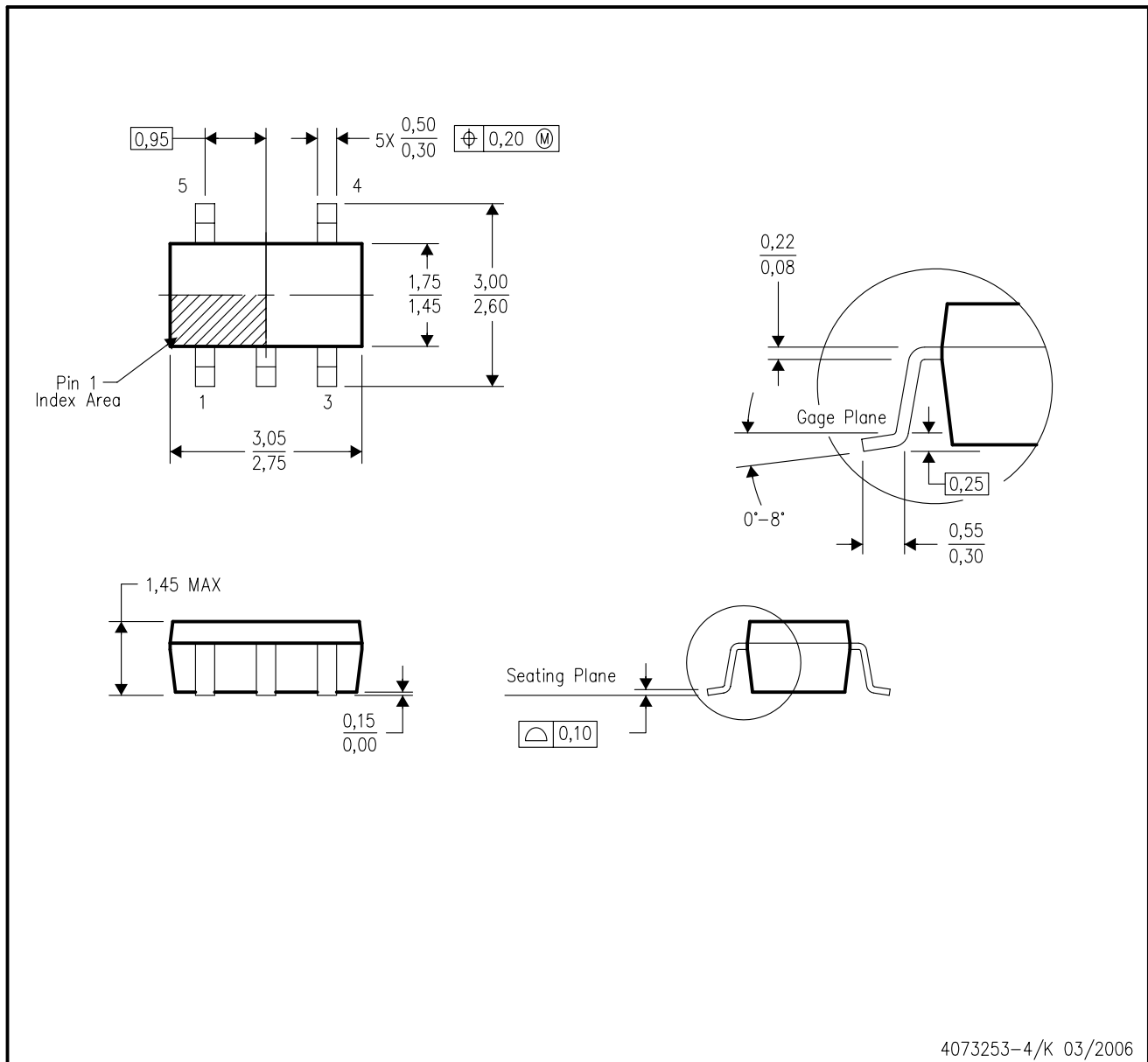


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVDS1DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| SN65LVDS1DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| SN65LVDS1DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65LVDS2DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| SN65LVDS2DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| SN65LVDS2DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN65LVDT2DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| SN65LVDT2DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| SN65LVDT2DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

DBV (R-PDSO-G5)

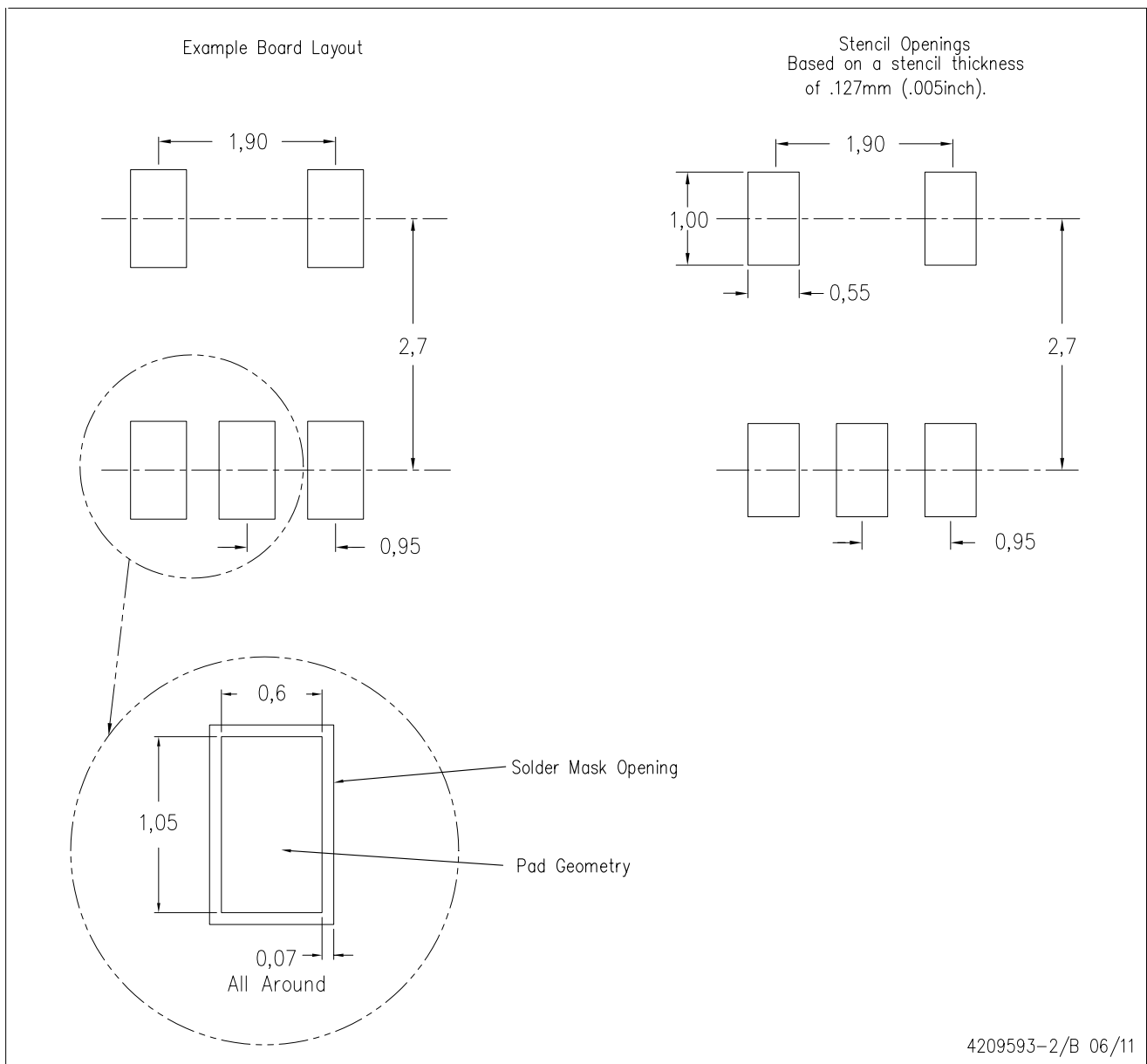
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

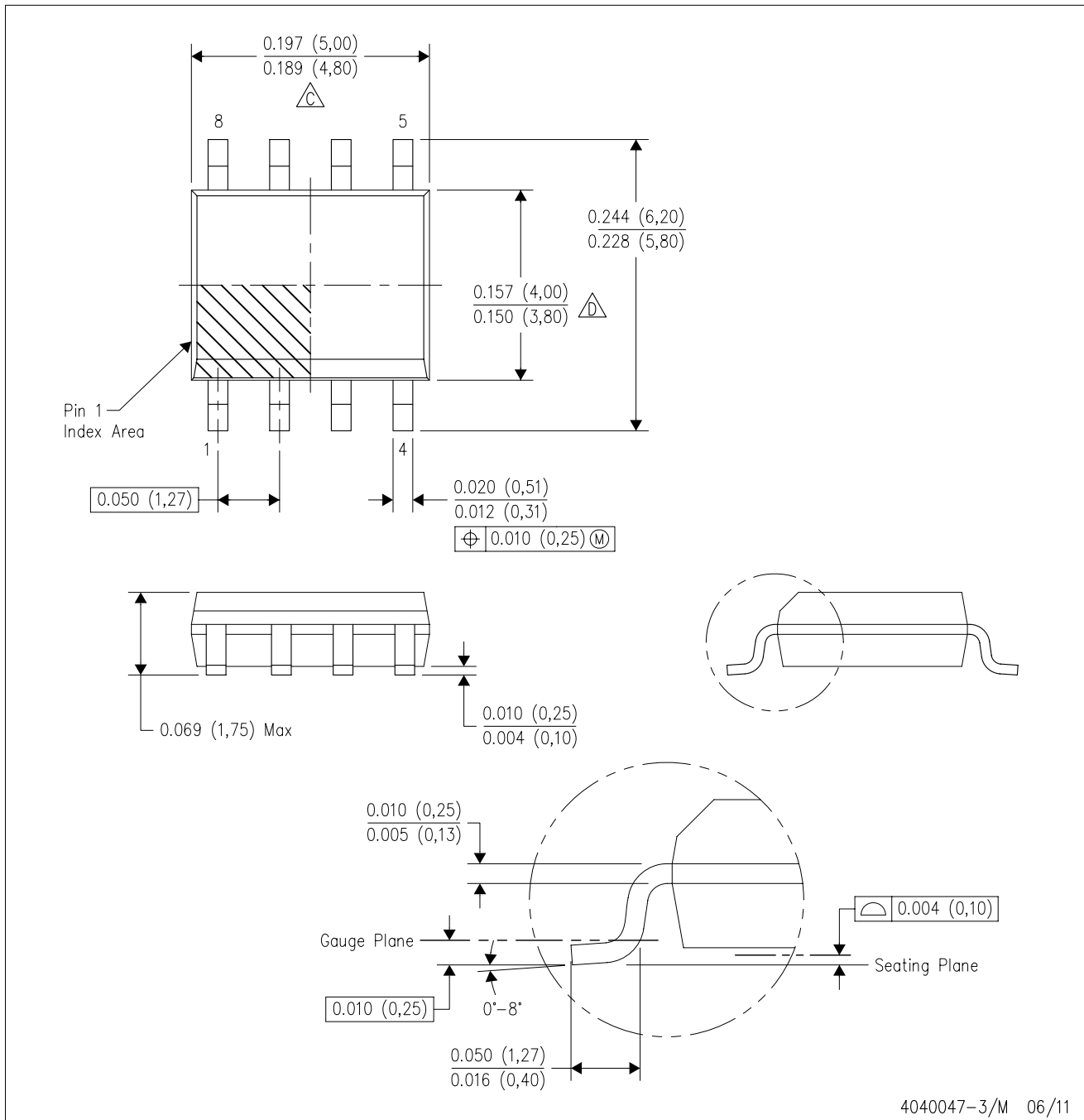
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

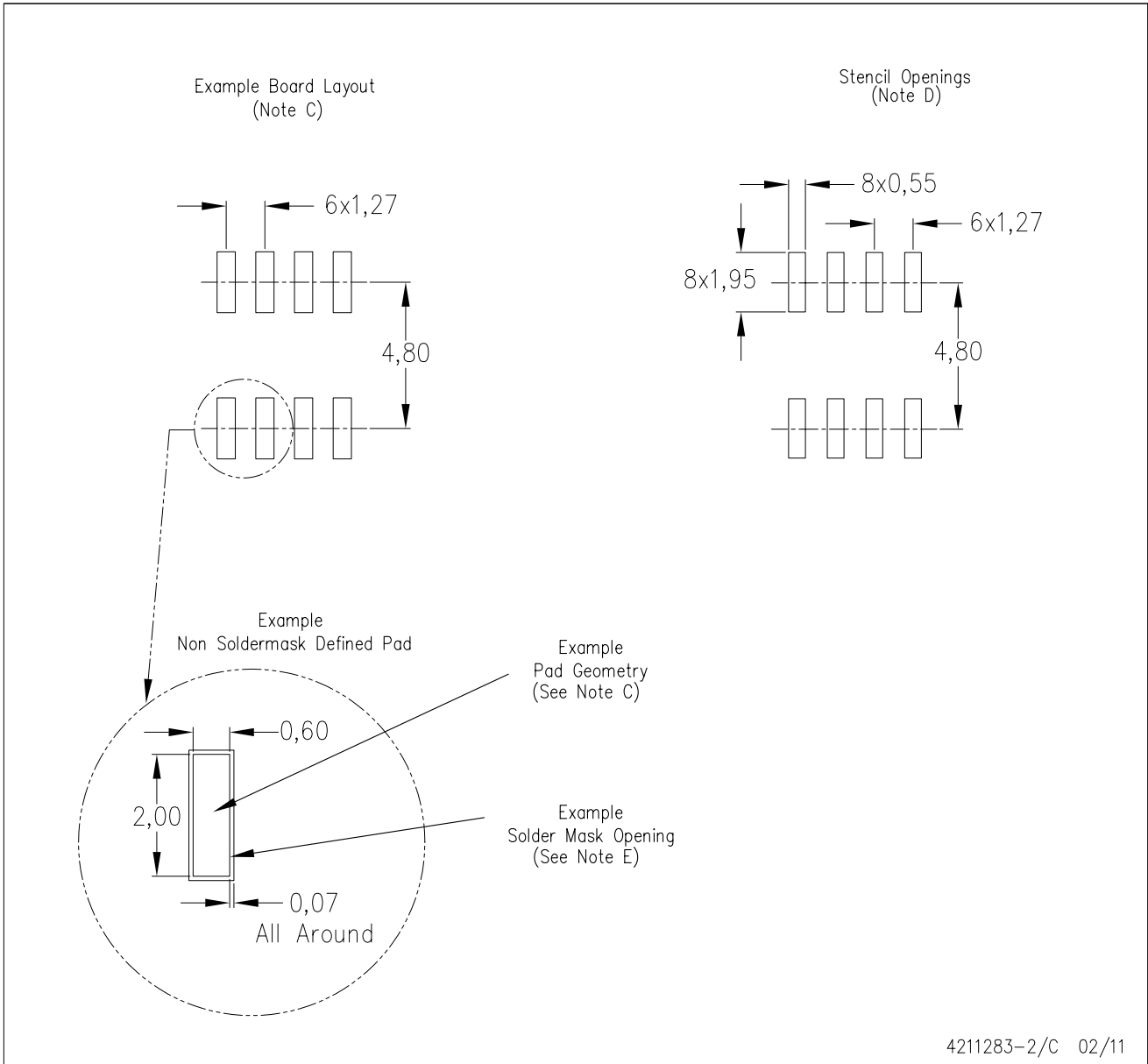
D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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