

2.7V to 6.0V Single Supply CMOS Op Amps

Features

- Single-Supply: 2.7V to 6.0V
- Rail-to-Rail Output
- Input Range Includes Ground
- Gain Bandwidth Product: 2.8 MHz (typical)
- Unity-Gain Stable
- Low Quiescent Current: 230 μ A/amplifier (typical)
- Chip Select ($\overline{\text{CS}}$): **MCP603 only**
- Temperature Ranges:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +125°C
- Available in Single, Dual, and Quad

Typical Applications

- Portable Equipment
- A/D Converter Driver
- Photo Diode Pre-amp
- Analog Filters
- Data Acquisition
- Notebooks and PDAs
- Sensor Interface

Available Tools

- SPICE Macro Models
- FilterLab[®] Software
- Mindi[™] Simulation Tool
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Description

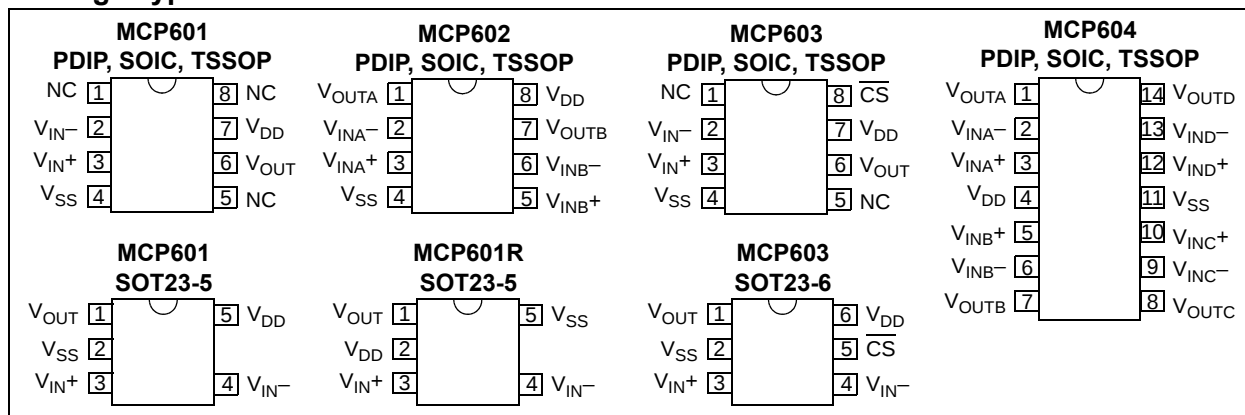
The Microchip Technology Inc. MCP601/1R/2/3/4 family of low-power operational amplifiers (op amps) are offered in single (MCP601), single with Chip Select ($\overline{\text{CS}}$) (MCP603), dual (MCP602), and quad (MCP604) configurations. These op amps utilize an advanced CMOS technology that provides low bias current, high-speed operation, high open-loop gain, and rail-to-rail output swing. This product offering operates with a single supply voltage that can be as low as 2.7V, while drawing 230 μ A (typical) of quiescent current per amplifier. In addition, the common mode input voltage range goes 0.3V below ground, making these amplifiers ideal for single-supply operation.

These devices are appropriate for low power, battery operated circuits due to the low quiescent current, for A/D convert driver amplifiers because of their wide bandwidth or for anti-aliasing filters by virtue of their low input bias current.

The MCP601, MCP602, and MCP603 are available in standard 8-lead PDIP, SOIC, and TSSOP packages. The MCP601 and MCP601R are also available in a standard 5-lead SOT-23 package, while the MCP603 is available in a standard 6-lead SOT-23 package. The MCP604 is offered in standard 14-lead PDIP, SOIC, and TSSOP packages.

The MCP601/1R/2/3/4 family is available in the Industrial and Extended temperature ranges and has a power supply range of 2.7V to 6.0V.

Package Types



MCP601/1R/2/3/4

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$	7.0V
Current at Input Pins	± 2 mA
Analog Inputs (V_{IN+} , V_{IN-}) ††	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All Other Inputs and Outputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage	$ V_{DD} - V_{SS} $
Output Short Circuit Current	Continuous
Current at Output and Supply Pins	± 30 mA
Storage Temperature.....	-65°C to $+150^{\circ}\text{C}$
Maximum Junction Temperature (T_J)	$+150^{\circ}\text{C}$
ESD Protection On All Pins (HBM; MM)	≥ 3 kV; 200V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage and Current Limits”**.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, $T_A = +25^{\circ}\text{C}$, $V_{DD} = +2.7V$ to $+5.5V$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, and $R_L = 100$ k Ω to V_L , and CS is tied low. (Refer to Figure 1-2 and Figure 1-3).						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2	± 0.7	+2	mV	
Industrial Temperature	V_{OS}	-3	± 1	+3	mV	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 1)
Extended Temperature	V_{OS}	-4.5	± 1	+4.5	mV	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (Note 1)
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	± 2.5	—	$\mu\text{V}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Power Supply Rejection	PSRR	80	88	—	dB	$V_{DD} = 2.7V$ to $5.5V$
Input Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature	I_B	—	20	60	pA	$T_A = +85^{\circ}\text{C}$ (Note 1)
Extended Temperature	I_B	—	450	5000	pA	$T_A = +125^{\circ}\text{C}$ (Note 1)
Input Offset Current	I_{OS}	—	± 1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	$10^{13} 6$	—	ΩpF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13} 3$	—	ΩpF	
Common Mode						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$	—	$V_{DD} - 1.2$	V	
Common Mode Rejection Ratio	CMRR	75	90	—	dB	$V_{DD} = 5.0V$, $V_{CM} = -0.3V$ to $3.8V$
Open-loop Gain						
DC Open-loop Gain (large signal)	A_{OL}	100	115	—	dB	$R_L = 25$ k Ω to V_L , $V_{OUT} = 0.1V$ to $V_{DD} - 0.1V$
	A_{OL}	95	110	—	dB	$R_L = 5$ k Ω to V_L , $V_{OUT} = 0.1V$ to $V_{DD} - 0.1V$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	$V_{SS} + 15$	—	$V_{DD} - 20$	mV	$R_L = 25$ k Ω to V_L , Output overdrive = $0.5V$
	V_{OL}, V_{OH}	$V_{SS} + 45$	—	$V_{DD} - 60$	mV	$R_L = 5$ k Ω to V_L , Output overdrive = $0.5V$
Linear Output Voltage Swing	V_{OUT}	$V_{SS} + 100$	—	$V_{DD} - 100$	mV	$R_L = 25$ k Ω to V_L , $A_{OL} \geq 100$ dB
	V_{OUT}	$V_{SS} + 100$	—	$V_{DD} - 100$	mV	$R_L = 5$ k Ω to V_L , $A_{OL} \geq 95$ dB
Output Short Circuit Current	I_{SC}	—	± 22	—	mA	$V_{DD} = 5.5V$
	I_{SC}	—	± 12	—	mA	$V_{DD} = 2.7V$
Power Supply						
Supply Voltage	V_{DD}	2.7	—	6.0	V	(Note 2)
Quiescent Current per Amplifier	I_Q	—	230	325	μA	$I_O = 0$

Note 1: These specifications are not tested in either the SOT-23 or TSSOP packages with date codes older than YYWW = 0408. In these cases, the minimum and maximum values are by design and characterization only.

Note 2: All parts with date codes November 2007 and later have been screened to ensure operation at $V_{DD}=6.0V$. However, the other minimum and maximum specifications are measured at $1.4V$ and/or $5.5V$.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.7\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, and $R_L = 100\text{ k}\Omega$ to V_L , $C_L = 50\text{ pF}$, and $\overline{\text{CS}}$ is tied low. (Refer to [Figure 1-2](#) and [Figure 1-3](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
Gain Bandwidth Product	GBWP	—	2.8	—	MHz	
Phase Margin	PM	—	50	—	°	$G = +1\text{ V/V}$
Step Response						
Slew Rate	SR	—	2.3	—	$\text{V}/\mu\text{s}$	$G = +1\text{ V/V}$
Settling Time (0.01%)	t_{settle}	—	4.5	—	μs	$G = +1\text{ V/V}$, 3.8V step
Noise						
Input Noise Voltage	E_{ni}	—	7	—	$\mu\text{V}_{\text{P-P}}$	$f = 0.1\text{ Hz to }10\text{ Hz}$
Input Noise Voltage Density	e_{ni}	—	29	—	$\text{nV}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$
	e_{ni}	—	21	—	$\text{nV}/\sqrt{\text{Hz}}$	$f = 10\text{ kHz}$
Input Noise Current Density	i_{ni}	—	0.6	—	$\text{fA}/\sqrt{\text{Hz}}$	$f = 1\text{ kHz}$

MCP603 CHIP SELECT ($\overline{\text{CS}}$) CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +2.7\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, and $R_L = 100\text{ k}\Omega$ to V_L , $C_L = 50\text{ pF}$, and $\overline{\text{CS}}$ is tied low. (Refer to [Figure 1-2](#) and [Figure 1-3](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{\text{CS}}$ Low Specifications						
$\overline{\text{CS}}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2 V_{DD}$	V	
$\overline{\text{CS}}$ Input Current, Low	I_{CSL}	-1.0	—	—	μA	$\overline{\text{CS}} = 0.2V_{DD}$
$\overline{\text{CS}}$ High Specifications						
$\overline{\text{CS}}$ Logic Threshold, High	V_{IH}	$0.8 V_{DD}$	—	V_{DD}	V	
$\overline{\text{CS}}$ Input Current, High	I_{CSH}	—	0.7	2.0	μA	$\overline{\text{CS}} = V_{DD}$
Shutdown V_{SS} current	I_{Q_SHDN}	-2.0	-0.7	—	μA	$\overline{\text{CS}} = V_{DD}$
Amplifier Output Leakage in Shutdown	I_{O_SHDN}	—	1	—	nA	
Timing						
$\overline{\text{CS}}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	3.1	10	μs	$\overline{\text{CS}} \leq 0.2V_{DD}$, $G = +1\text{ V/V}$
$\overline{\text{CS}}$ High to Amplifier Output High-Z Time	t_{OFF}	—	100	—	ns	$\overline{\text{CS}} \geq 0.8V_{DD}$, $G = +1\text{ V/V}$, No load.
Hysteresis	V_{HYST}	—	0.4	—	V	$V_{DD} = 5.0\text{V}$

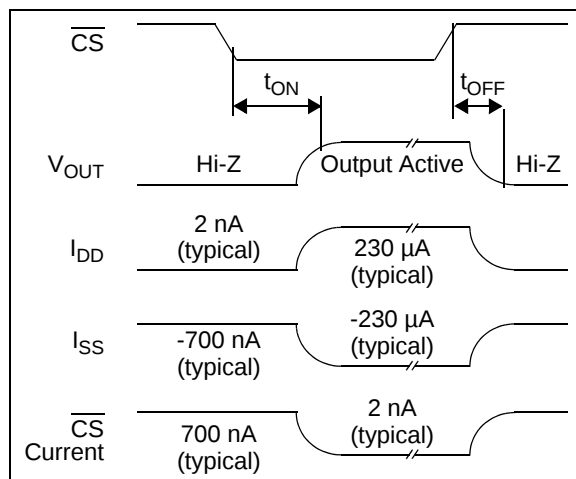


FIGURE 1-1: MCP603 Chip Select ($\overline{\text{CS}}$) Timing Diagram.

MCP601/1R/2/3/4

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{DD} = +2.7V$ to $+5.5V$ and $V_{SS} = GND$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	Industrial temperature parts
	T_A	-40	—	+125	°C	Extended temperature parts
Operating Temperature Range	T_A	-40	—	+125	°C	Note
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 6L-SOT23	θ_{JA}	—	230	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The Industrial temperature parts operate over this extended range, but with reduced performance. The Extended temperature specs do not apply to Industrial temperature parts. In any case, the internal Junction temperature (T_J) must not exceed the absolute maximum specification of 150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in [Figure 1-2](#) and [Figure 1-2](#). The bypass capacitors are laid out according to the rules discussed in [Section 4.5 “Supply Bypass”](#).

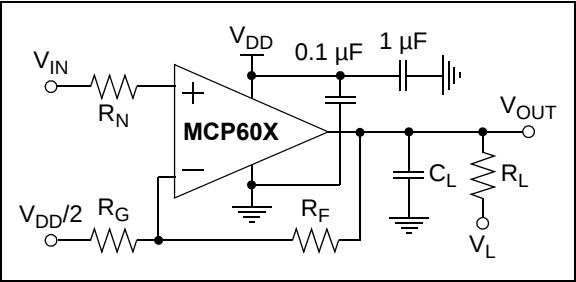


FIGURE 1-2: AC and DC Test Circuit for Most Non-Inverting Gain Conditions.

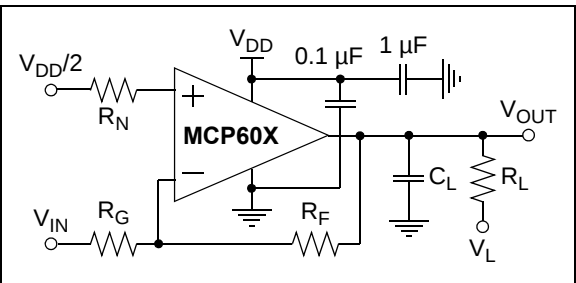
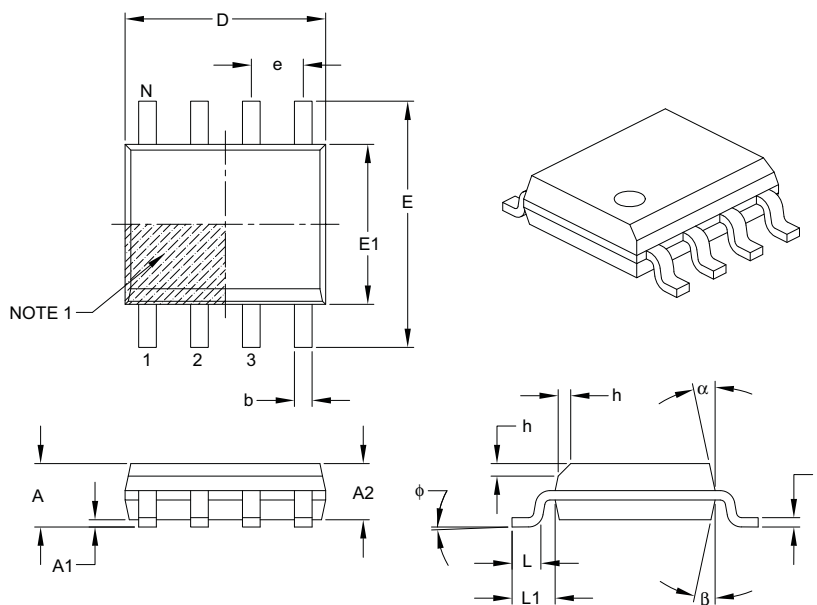


FIGURE 1-3: AC and DC Test Circuit for Most Inverting Gain Conditions.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

