

## Low-Noise, Very Low Drift, Precision Voltage Reference

Check for Samples: [REF5010](#), [REF5020](#), [REF5025](#), [REF5030](#), [REF5040](#), [REF5045](#), [REF5050](#)

### FEATURES

- **LOW TEMPERATURE DRIFT:**
  - High-Grade: 3ppm/°C (max)
  - Standard-Grade: 8ppm/°C (max)
- **HIGH ACCURACY:**
  - High-Grade: 0.05% (max)
  - Standard-Grade: 0.1% (max)
- **LOW NOISE:** 3μV<sub>PP</sub>/V
- **EXCELLENT LONG-TERM STABILITY:**
  - 45ppm/1000hr (typ) after 1000 hours
- **HIGH OUTPUT CURRENT:** ±10mA
- **TEMPERATURE RANGE:** –40°C to +125°C

### APPLICATIONS

- 16-BIT DATA ACQUISITION SYSTEMS
- ATE EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- OPTICAL CONTROL SYSTEMS
- PRECISION INSTRUMENTATION

### DESCRIPTION

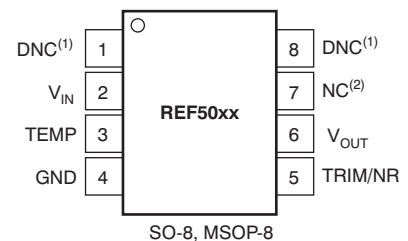
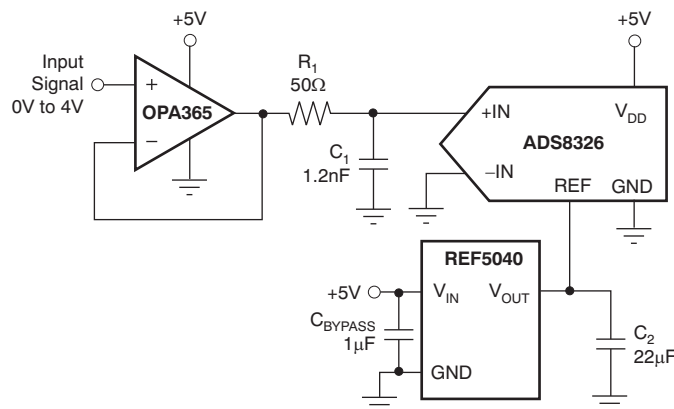
The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

Excellent temperature drift (3ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very low noise, make the REF50xx family ideal for use in high-precision data acquisition systems.

Each reference voltage is available in both standard- and high-grade versions. They are offered in MSOP-8 and SO-8 packages, and are specified from –40°C to +125°C.

**REF50xx Family**

MODEL	OUTPUT VOLTAGE
REF5020	2.048V
REF5025	2.5V
REF5030	3.0V
REF5040	4.096V
REF5045	4.5V
REF5050	5.0V
REF5010	10.0V



NOTES: (1) DNC = Do not connect.  
(2) NC = No internal connection.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	OUTPUT VOLTAGE
<b>STANDARD GRADE (8ppm, 0.1%)</b>	
REF5020A	2.048V
REF5025A	2.5V
REF5030A	3.0V
REF5040A	4.096V
REF5045A	4.5V
REF5050A	5.0V
REF5010A	10.0V
<b>HIGH GRADE (3ppm, 0.05%)</b>	
REF5020I	2.048V
REF5025I	2.5V
REF5030I	3.0V
REF5040I	4.096V
REF5045I	4.5V
REF5050I	5.0V
REF5010I	10.0V

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the [device product folder](#) at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		REF50xx	UNIT
Input Voltage		+18	V
Output Short-Circuit		30	mA
Operating Temperature Range		-55 to +125	°C
Storage Temperature Range		-65 to +150	°C
Junction Temperature (T <sub>J</sub> max)		+150	°C
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## ELECTRICAL CHARACTERISTICS: PER DEVICE

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $C_L = 1\mu\text{F}$ , and  $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$  to 18V, unless otherwise noted.

PARAMETER	CONDITIONS	PER DEVICE			UNIT
		MIN	TYP	MAX	
<b>REF5020 (<math>V_{\text{OUT}} = 2.048\text{V}</math>)<sup>(1)</sup></b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$ $2.7\text{V} < V_{\text{IN}} < 18\text{V}$		2.048		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		6		$\mu\text{V}_{\text{PP}}$
<b>REF5025 (<math>V_{\text{OUT}} = 2.5\text{V}</math>)</b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$		2.5		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		7.5		$\mu\text{V}_{\text{PP}}$
<b>REF5030 (<math>V_{\text{OUT}} = 3.0\text{V}</math>)</b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$		3.0		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		9		$\mu\text{V}_{\text{PP}}$
<b>REF5040 (<math>V_{\text{OUT}} = 4.096\text{V}</math>)</b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$		4.096		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		12		$\mu\text{V}_{\text{PP}}$
<b>REF5045 (<math>V_{\text{OUT}} = 4.5\text{V}</math>)</b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$		4.5		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		13.5		$\mu\text{V}_{\text{PP}}$
<b>REF5050 (<math>V_{\text{OUT}} = 5.0\text{V}</math>)</b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$		5.0		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		15		$\mu\text{V}_{\text{PP}}$
<b>REF5010 (<math>V_{\text{OUT}} = 10.0\text{V}</math>)</b>					
<b>OUTPUT VOLTAGE</b>					
Output Voltage	$V_{\text{OUT}}$		10.0		V
Initial Accuracy:	High-Grade	-0.05		0.05	%
	Standard-Grade	-0.1		0.1	%
<b>NOISE</b>					
Output Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		30		$\mu\text{V}_{\text{PP}}$

(1) For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimum supply voltage is 2.7V.

## ELECTRICAL CHARACTERISTICS: ALL DEVICES

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $I_{\text{LOAD}} = 0$ ,  $C_L = 1\mu\text{F}$ , and  $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$  to 18V, unless otherwise noted.

PARAMETER	CONDITIONS	REF50xx			UNIT
		MIN	TYP	MAX	
<b>OUTPUT VOLTAGE TEMPERATURE DRIFT</b>					
Output Voltage Temperature Drift	$dV_{\text{OUT}}/dT$				
High-Grade			2.5	3	ppm/ $^{\circ}\text{C}$
Standard-Grade			3	8	ppm/ $^{\circ}\text{C}$
<b>LINE REGULATION</b>					
Line Regulation	$dV_{\text{OUT}}/dV_{\text{IN}}$				
REF5020 <sup>(1)</sup> Only	$V_{\text{IN}} = 2.7\text{V}$ to 18V		0.1	1	ppm/V
All Other Devices	$V_{\text{IN}} = V_{\text{OUT}} + 0.2\text{V}$		0.1	1	ppm/V
<b>Over Temperature</b>			<b>0.2</b>	<b>1</b>	<b>ppm/V</b>
<b>LOAD REGULATION</b>					
Load Regulation	$dV_{\text{OUT}}/dI_{\text{LOAD}}$	$-10\text{mA} < I_{\text{LOAD}} < +10\text{mA}$			
REF5020 Only	$V_{\text{IN}} = 3\text{V}$		20	30	ppm/mA
All Other Devices	$V_{\text{IN}} = V_{\text{OUT}} + 0.75\text{V}$		20	30	ppm/mA
<b>Over Temperature</b>				<b>50</b>	<b>ppm/mA</b>
<b>SHORT-CIRCUIT CURRENT</b>					
Short-Circuit Current	$I_{\text{SC}}$	$V_{\text{OUT}} = 0$		25	mA
<b>THERMAL HYSTERESIS</b> <sup>(2)</sup> <sup>(3)</sup>					
High-Grade	MSOP-8	Cycle 1	50		ppm
Standard-Grade	MSOP-8	Cycle 1	70		ppm
High-Grade	SO-8	Cycle 1	70		ppm
Standard-Grade	SO-8	Cycle 1	90		ppm
High-Grade	MSOP-8	Cycle 2	40		ppm
Standard-Grade	MSOP-8	Cycle 2	40		ppm
High-Grade	SO-8	Cycle 2	50		ppm
Standard-Grade	SO-8	Cycle 2	50		ppm
<b>LONG-TERM STABILITY</b> <sup>(3)</sup>					
MSOP-8		0 to 1000 hours	125		ppm/1000 hr
MSOP-8		1000 to 2000 hours	45		ppm/1000 hr
SO-8		0 to 1000 hours	100		ppm/1000 hr
SO-8		1000 to 2000 hours	50		ppm/1000 hr
<b>TEMP PIN</b>					
Voltage Output		At $T_A = +25^{\circ}\text{C}$	575		mV
<b>Temperature Sensitivity</b>			<b>2.64</b>		<b>mV/<math>^{\circ}\text{C}</math></b>
<b>TURN-ON SETTLING TIME</b>					
Turn-On Settling Time		To 0.1% with $C_L = 1\mu\text{F}$	200		$\mu\text{s}$
<b>POWER SUPPLY</b>					
Supply Voltage	$V_S$	See Note <sup>(1)</sup>	$V_{\text{OUT}} + 0.2$ <sup>(1)</sup>	18	V
Quiescent Current			0.8	1	mA
<b>Over Temperature</b>				<b>1.2</b>	<b>mA</b>
<b>TEMPERATURE RANGE</b>					
Specified Range			-40	+125	$^{\circ}\text{C}$
Operating Range			-55	+125	$^{\circ}\text{C}$
Thermal Resistance	$\theta_{\text{JA}}$				
MSOP-8			150		$^{\circ}\text{C}/\text{W}$
SO-8			150		$^{\circ}\text{C}/\text{W}$

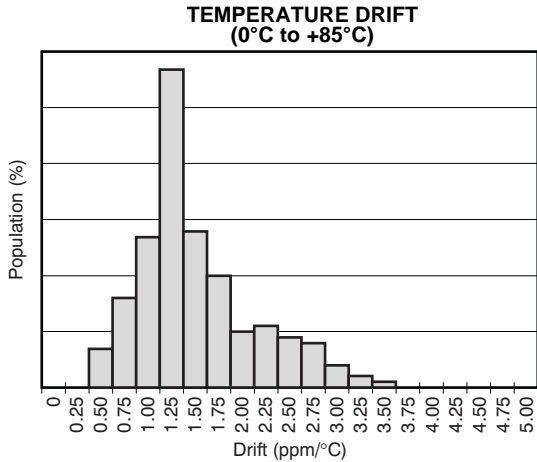
(1) For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimal supply voltage is 2.7V.

(2) The thermal hysteresis procedure is explained in more detail in the [Application Information](#) section.

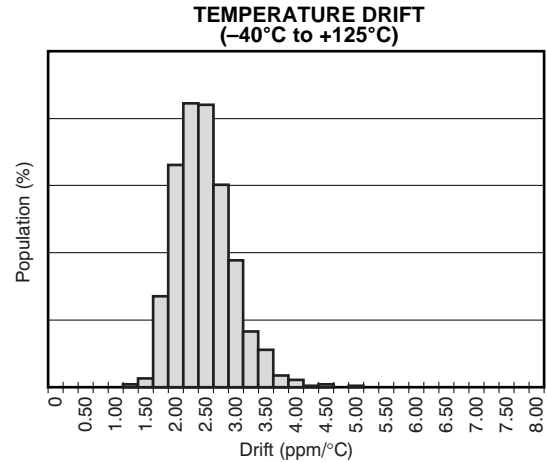
(3) Data collected using devices soldered onto the text board.

**TYPICAL CHARACTERISTICS**

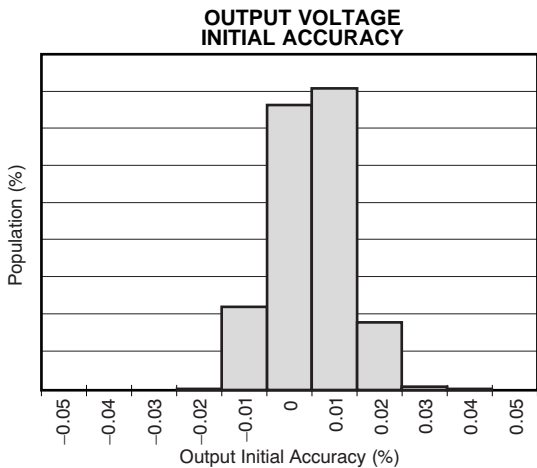
At  $T_A = +25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimum supply voltage is 2.7V.



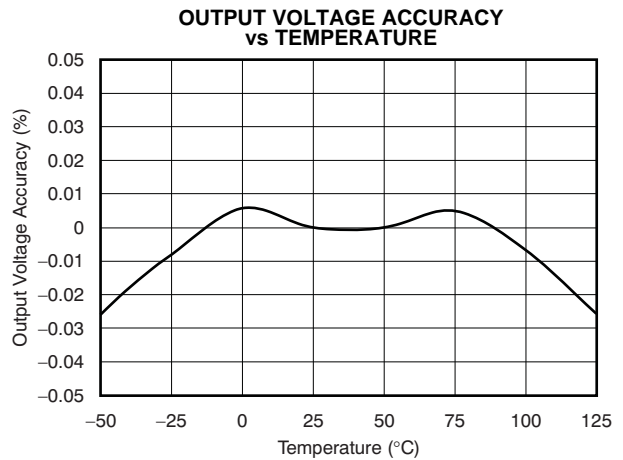
**Figure 1.**



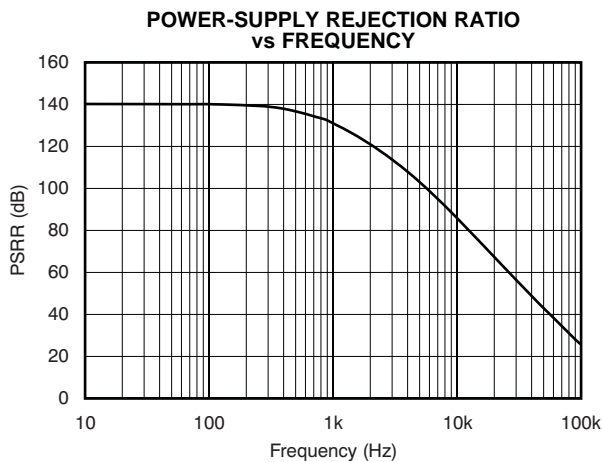
**Figure 2.**



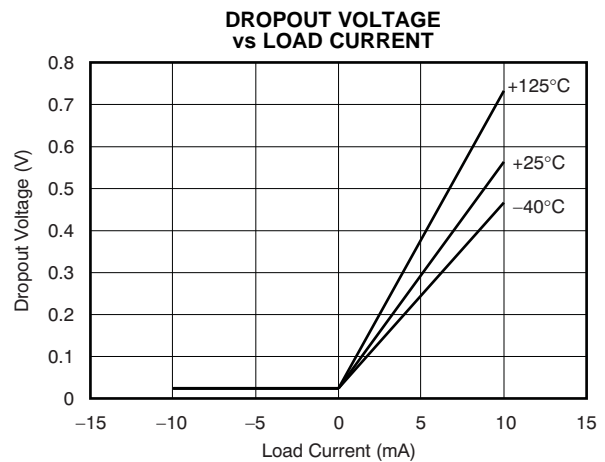
**Figure 3.**



**Figure 4.**



**Figure 5.**



**Figure 6.**

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimum supply voltage is 2.7V.

**REF5025 OUTPUT VOLTAGE vs LOAD CURRENT**

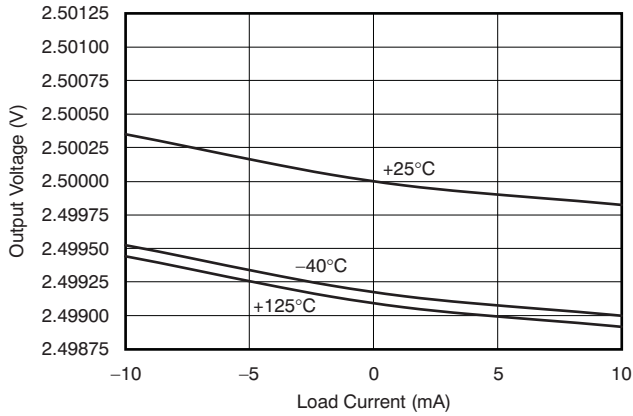


Figure 7.

**TEMP PIN OUTPUT VOLTAGE vs TEMPERATURE**

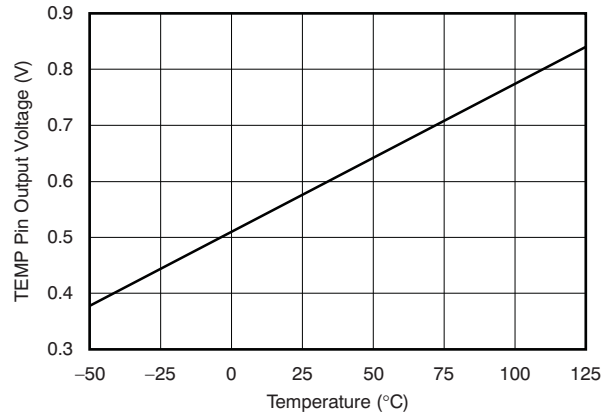


Figure 8.

**QUIESCENT CURRENT vs TEMPERATURE**

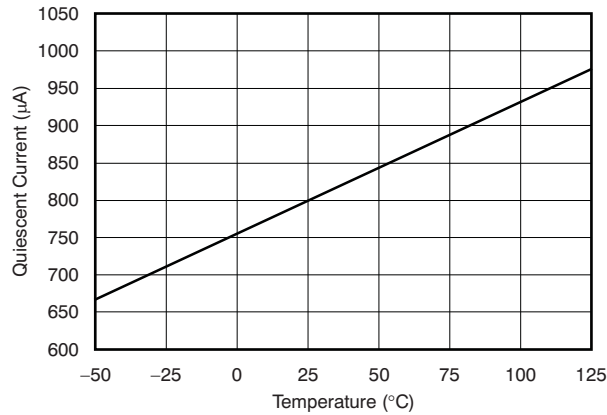


Figure 9.

**QUIESCENT CURRENT vs INPUT VOLTAGE**

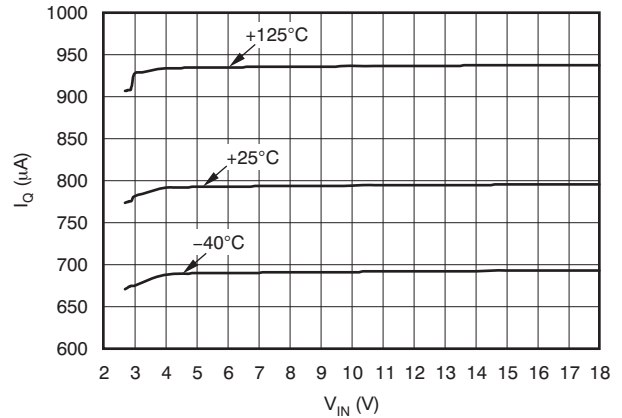


Figure 10.

**LINE REGULATION vs TEMPERATURE**

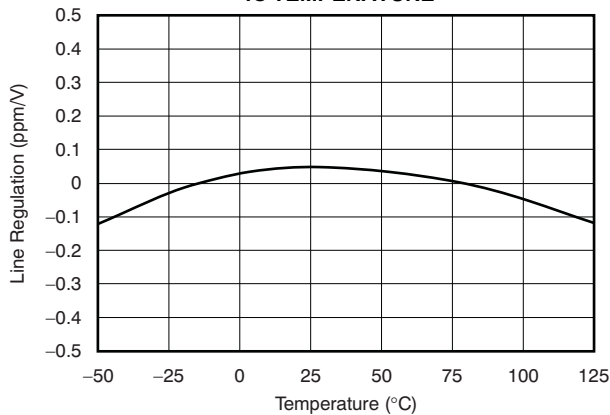


Figure 11.

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**

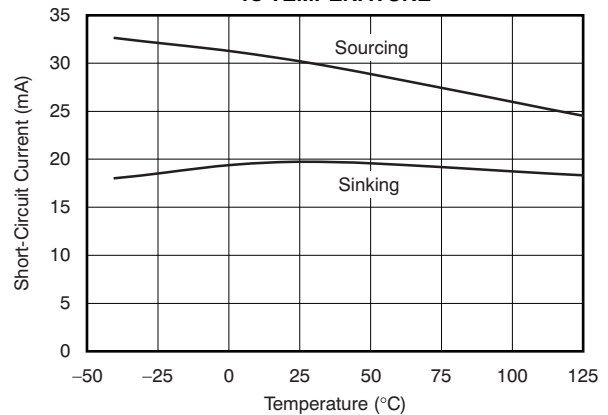


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimum supply voltage is 2.7V.

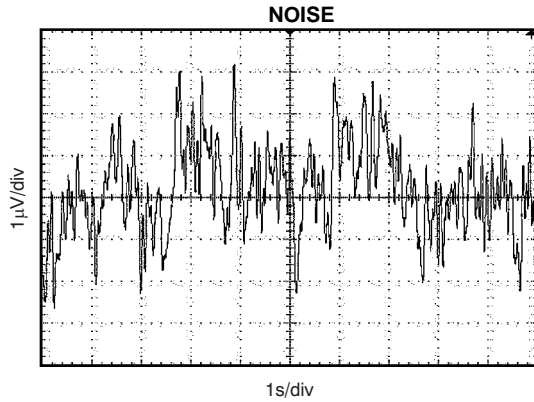


Figure 13.

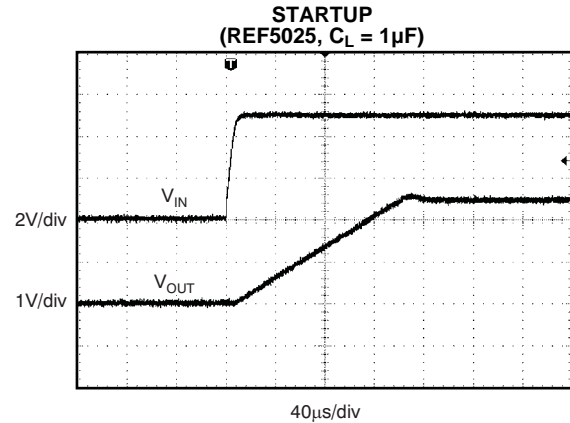


Figure 14.

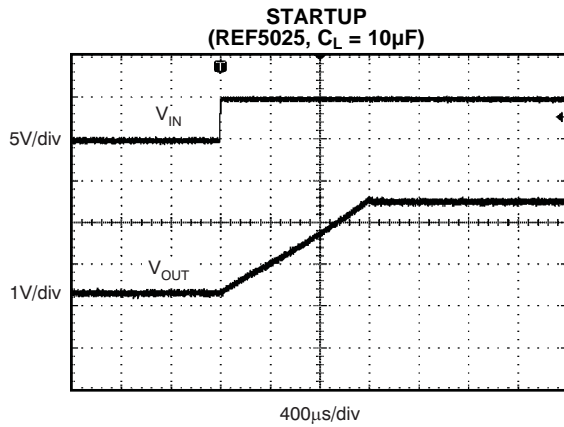


Figure 15.

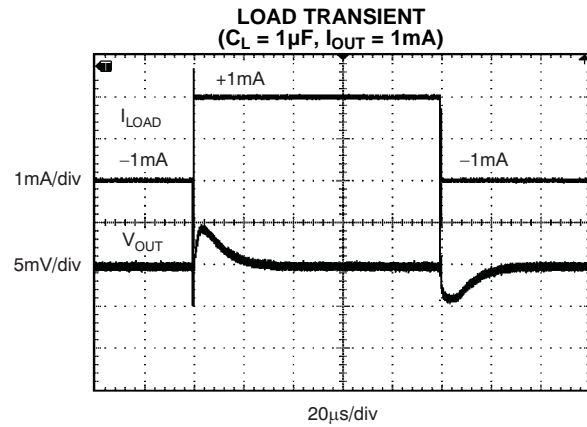


Figure 16.

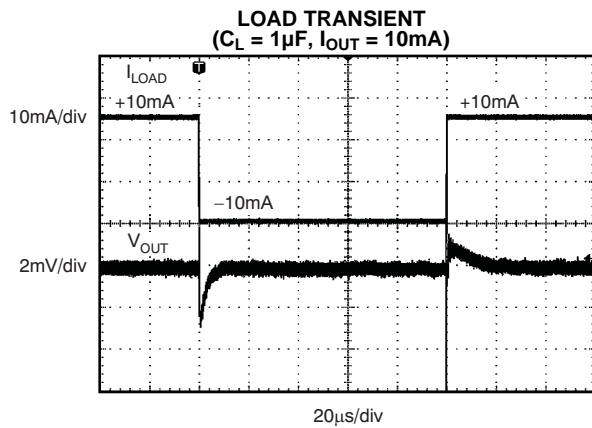


Figure 17.

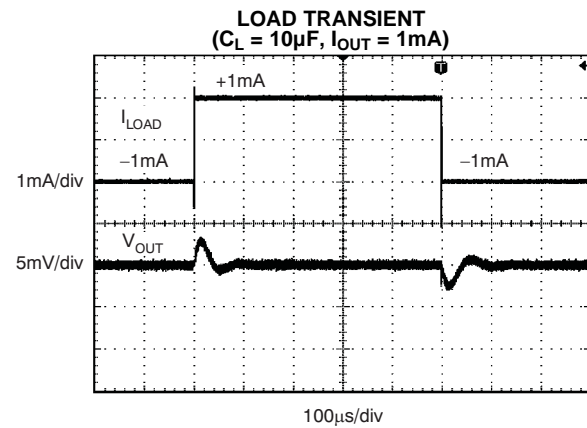


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimum supply voltage is 2.7V.

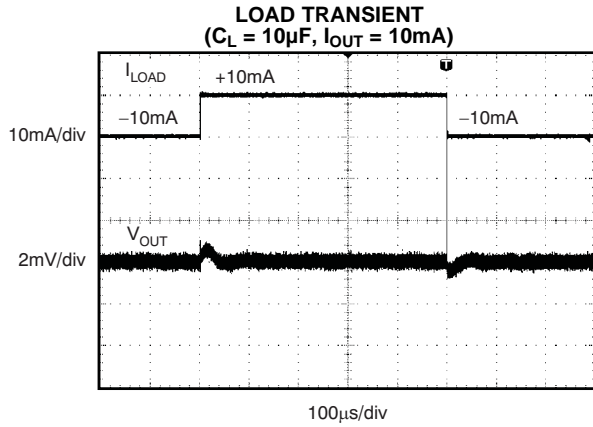


Figure 19.

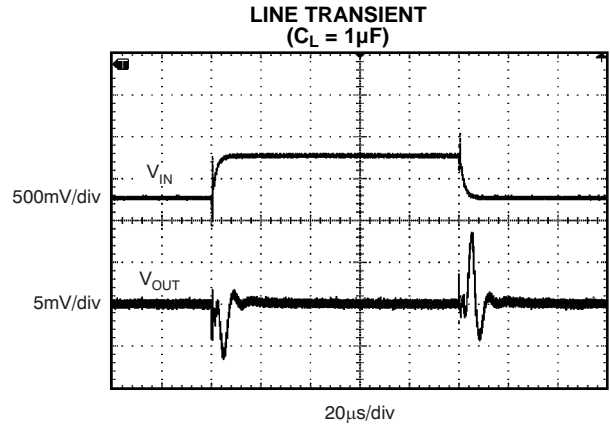


Figure 20.

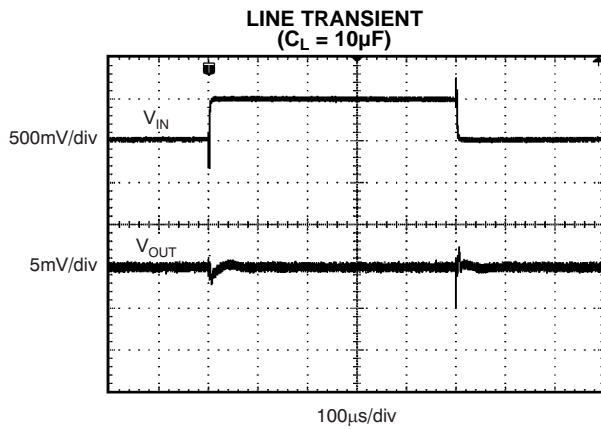


Figure 21.

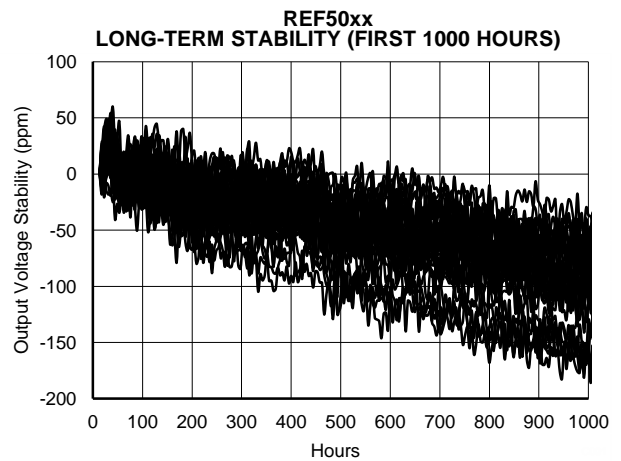


Figure 22.

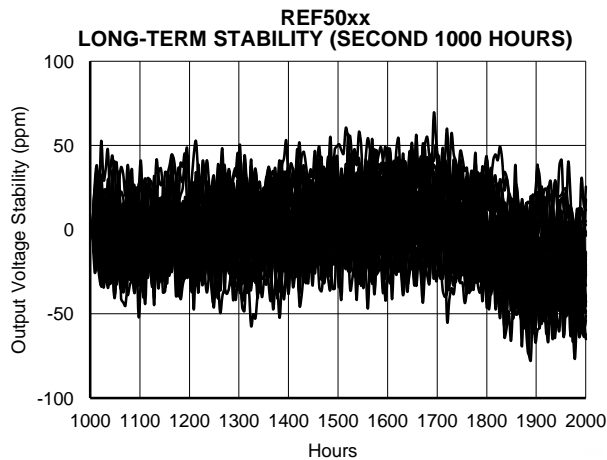


Figure 23.

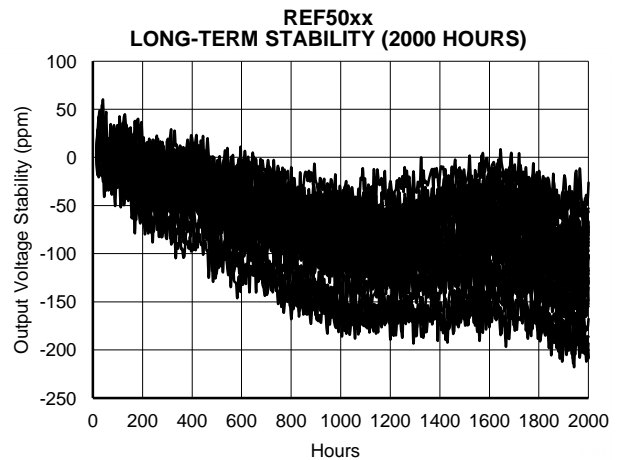
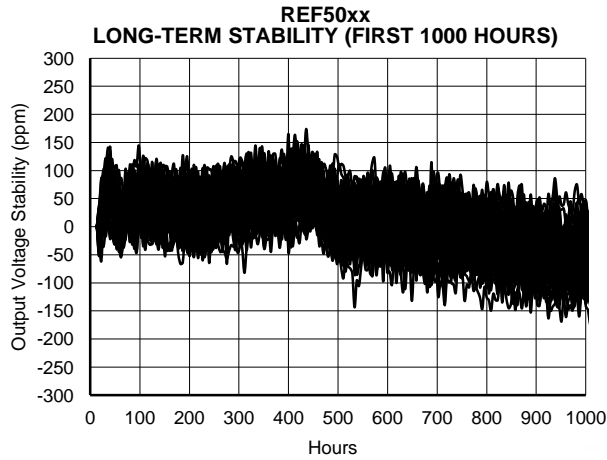


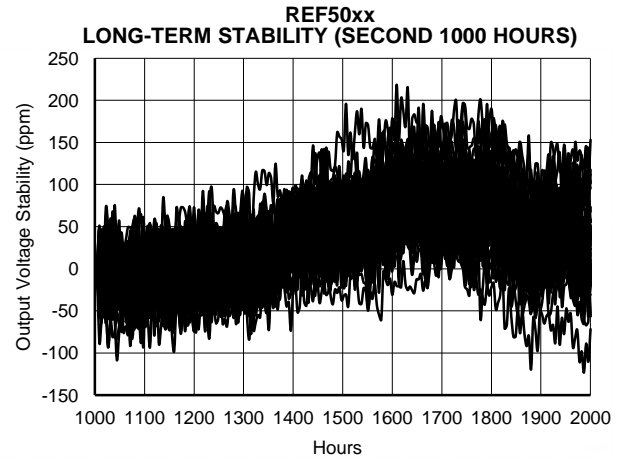
Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

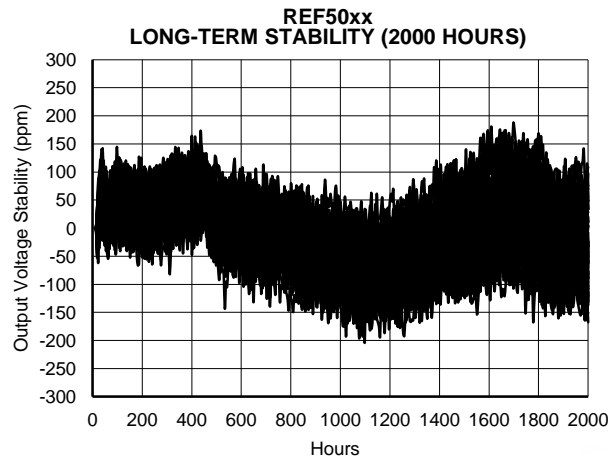
At  $T_A = +25^\circ\text{C}$ ,  $I_{\text{LOAD}} = 0$ , and  $V_S = V_{\text{OUT}} + 0.2\text{V}$ , unless otherwise noted. For  $V_{\text{OUT}} \leq 2.5\text{V}$ , the minimum supply voltage is 2.7V.



**Figure 25.**



**Figure 26.**



**Figure 27.**

## APPLICATION INFORMATION

The REF50xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. Figure 28 shows a simplified block diagram of the REF50xx.

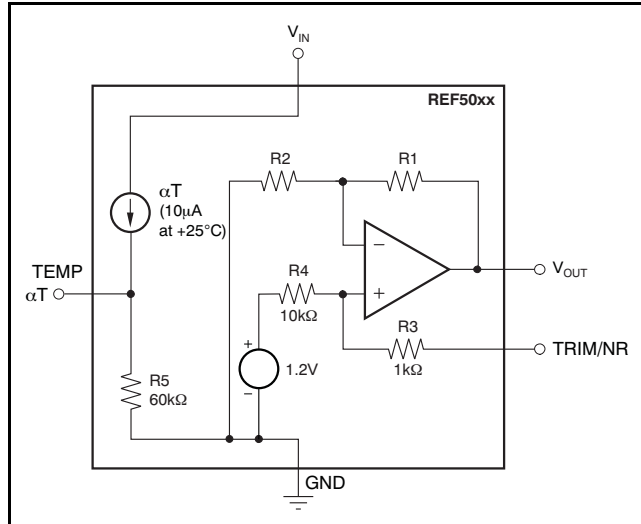


Figure 28. REF50xx Simplified Block Diagram

## BASIC CONNECTIONS

Figure 29 shows the typical connections for the REF50xx. A supply bypass capacitor ranging between 1µF to 10µF is recommended. A 1µF to 50µF output capacitor ( $C_L$ ) must be connected from  $V_{OUT}$  to GND. The ESR value of  $C_L$  must be less than or equal to 1.5Ω to ensure output stability. To minimize noise, the recommended ESR of  $C_L$  is between 1Ω and 1.5Ω.

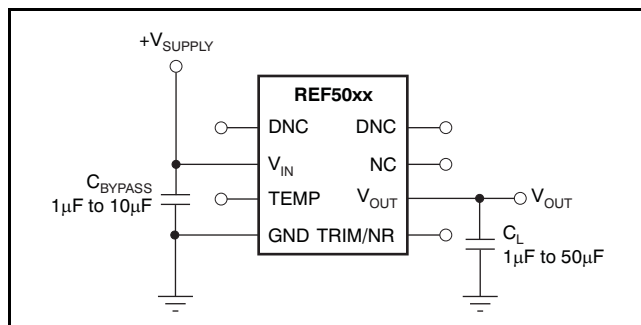


Figure 29. Basic Connections

## SUPPLY VOLTAGE

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply

requirement of 2.7V, these references can be operated with a supply of 200mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 6 of the Typical Characteristics.

## OUTPUT ADJUSTMENT USING THE TRIM/NR PIN

The REF50xx provides a very accurate, factory-trimmed voltage output. However,  $V_{OUT}$  can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). Figure 30 shows a typical circuit that allows an output adjustment of ±15mV

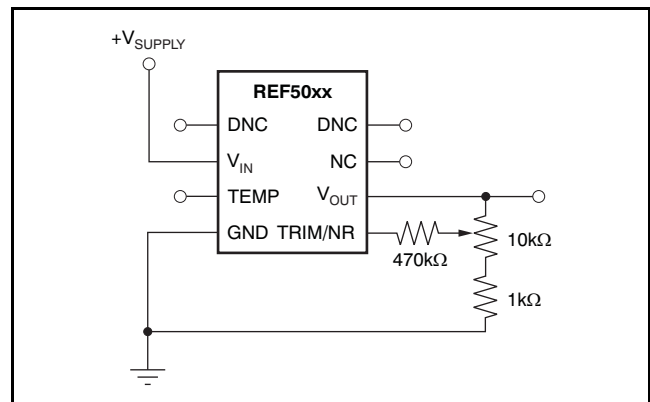


Figure 30.  $V_{OUT}$  Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (see Figure 31) in combination with the internal  $R_3$  and  $R_4$  resistors creates a low-pass filter. A capacitance of 1µF creates a low-pass filter with the corner frequency between 10Hz and 20Hz. Such a filter decreases the overall noise measured on the  $V_{OUT}$  pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Note that use of this capacitor increases startup time.

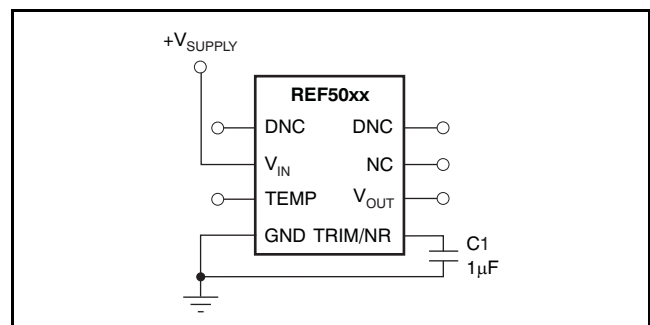


Figure 31. Noise Reduction Using the TRIM/NR Pin

## TEMPERATURE DRIFT

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left( \frac{V_{\text{OUTMAX}} - V_{\text{OUTMIN}}}{V_{\text{OUT}} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

The REF50xx features a maximum drift coefficient of 3ppm/°C for the high-grade version, and 8ppm/°C for the standard-grade.

## THERMAL HYSTERESIS

Thermal hysteresis for the REF50xx is defined as the change in output voltage after operating the device at +25°C, cycling the device through the specified temperature range, and returning to +25°C. It can be expressed as Equation 2:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 (\text{ppm}) \quad (2)$$

Where:

$V_{\text{HYST}}$  = thermal hysteresis (in units of ppm).

$V_{\text{NOM}}$  = the specified output voltage.

$V_{\text{PRE}}$  = output voltage measured at +25°C pretemperature cycling.

$V_{\text{POST}}$  = output voltage measured after the device has been cycled from +25°C through the specified temperature range of –40°C to +125°C and returned to +25°C.

## TEMPERATURE MONITORING

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60kΩ source impedance. As seen in Figure 8, the output voltage follows the nominal relationship:

$$V_{\text{TEMP PIN}} = 509\text{mV} + 2.64 \times T(^{\circ}\text{C})$$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see Figure 28). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on  $V_{\text{OUT}}$  accuracy.

To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 32.

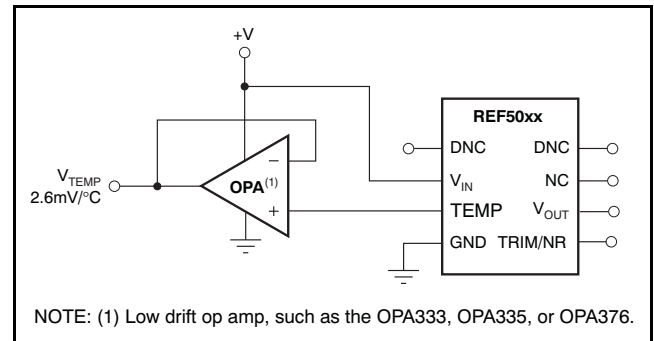


Figure 32. Buffering the TEMP Pin Output

## POWER DISSIPATION

The REF50xx family is specified to deliver current loads of ±10mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Where:

$T_J$  = Junction temperature (°C)

$T_A$  = Ambient temperature (°C)

$P_D$  = Power dissipated (W)

$\theta_{JA}$  = Junction-to-ambient thermal resistance (°C/W)

The REF50xx junction temperature must not exceed the absolute maximum rating of +150°C.

## NOISE PERFORMANCE

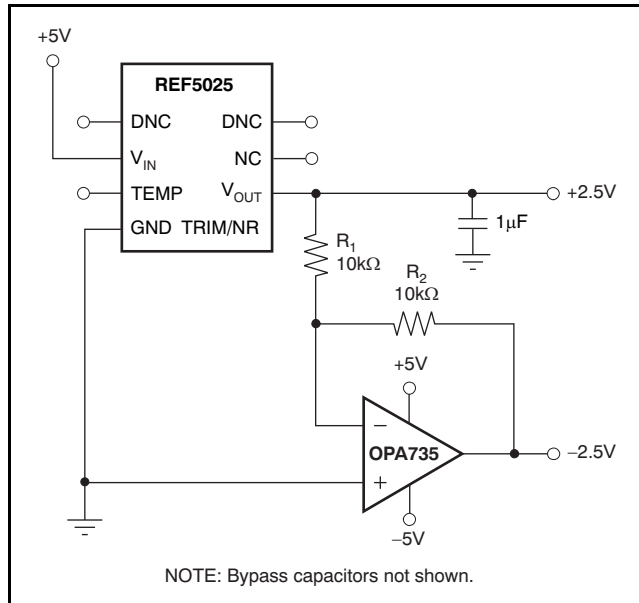
Typical 0.1Hz to 10Hz voltage noise for each member of the REF50xx family is specified in the *Electrical Characteristics: Per Device* table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications such as data converters, refer to the series of *Analog Applications Journal* articles entitled, *How a Voltage Reference Affects ADC Performance*. This three-part series is available for download from the TI website under three literature numbers: SLYT331, SLYT339, and SLYT355 for Part I, Part II, and Part III, respectively.

## APPLICATION CIRCUITS

### NEGATIVE REFERENCE VOLTAGE

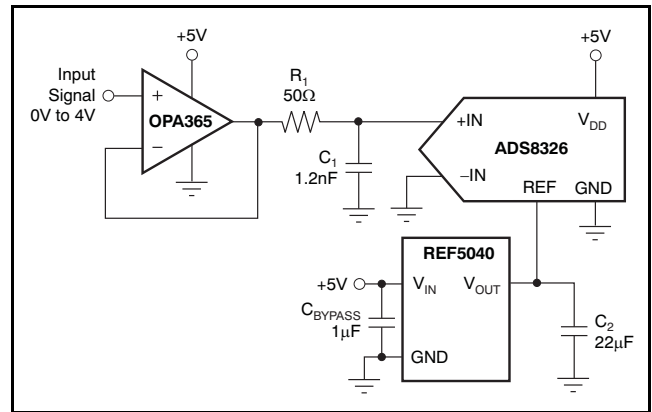
For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5V supply. Figure 33 shows the REF5025 used to provide a 2.5V supply reference voltage. The low drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of  $R_1$  and  $R_2$ .



**Figure 33. The REF5025 and OPA735 Create Positive and Negative Reference Voltages**

### DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 34 shows the REF5040 in a basic data acquisition system.



**Figure 34. Basic Data Acquisition System**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2010) to Revision F	Page
• Changed <i>Excellent Long-Term Stability</i> feature bullet .....	1
• Changed <i>Thermal Hysteresis</i> typical values .....	4
• Changed <i>Long-Term Stability</i> typical values .....	4
• Added note 3 to Electrical Characteristics .....	4
• Changed <a href="#">Figure 22</a> .....	8
• Changed <a href="#">Figure 23</a> .....	8
• Changed <a href="#">Figure 24</a> .....	8
• Changed <a href="#">Figure 25</a> .....	8
• Changed <a href="#">Figure 26</a> .....	8
• Changed <a href="#">Figure 27</a> .....	9

Changes from Revision D (April 2009) to Revision E	Page
• Updated <i>Features</i> list; added <i>Excellent Long-Term Stability</i> bullet .....	1
• Added <i>Thermal Hysteresis</i> parameters and specifications .....	4
• Added <i>Long-Term Stability</i> parameters and specifications .....	4
• Added <a href="#">Figure 22</a> through <a href="#">Figure 24</a> .....	8
• Added <a href="#">Figure 25</a> through <a href="#">Figure 27</a> .....	8
• Added <i>Thermal Hysteresis</i> section .....	11
• Revised <i>Noise Performance</i> section; added paragraph with links to applications articles .....	11

Changes from Revision C (December 2008) to Revision D	Page
• Removed all notes regarding MSOP-8 package status. MSOP-8 package released at time of document revision .....	1
• Changed <i>Storage Temperature Range</i> absolute minimum value from $-55^{\circ}\text{C}$ to $-65^{\circ}\text{C}$ .....	2
• Added test condition to <i>Line Regulation, All other devices</i> specification .....	4
• Added <i>Load Regulation</i> test condition and <i>Over Temperature</i> specifications .....	4
• Added typical characteristic graph, <i>Quiescent Current vs Input Voltage</i> ( <a href="#">Figure 10</a> ) .....	6

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5010AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A	<a href="#">Samples</a>
REF5010AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010 A	<a href="#">Samples</a>
REF5010ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5010	<a href="#">Samples</a>
REF5010IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50G	<a href="#">Samples</a>
REF5010IDR	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	REF 5010	<a href="#">Samples</a>
REF5020AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>
REF5020AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020 A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5020ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5020IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5020IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50A	<a href="#">Samples</a>
REF5020IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5020IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5020	<a href="#">Samples</a>
REF5025AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025 A	<a href="#">Samples</a>
REF5025ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5025IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5025IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>
REF5025IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5025IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5025IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5025	<a href="#">Samples</a>
REF5030AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030 A	<a href="#">Samples</a>
REF5030ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	<a href="#">Samples</a>
REF5030IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	<a href="#">Samples</a>
REF5030IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50C	<a href="#">Samples</a>
REF5030IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5030	<a href="#">Samples</a>
REF5040AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	<a href="#">Samples</a>
REF5040AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5040AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040 A	<a href="#">Samples</a>
REF5040ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5040IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5040IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50D	<a href="#">Samples</a>
REF5040IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5040IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5040	<a href="#">Samples</a>
REF5045AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045 A	<a href="#">Samples</a>
REF5045ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF5045IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50E	<a href="#">Samples</a>
REF5045IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5045	<a href="#">Samples</a>
REF5050AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	<a href="#">Samples</a>
REF5050AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	<a href="#">Samples</a>
REF5050AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050 A	<a href="#">Samples</a>
REF5050ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>
REF5050IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>
REF5050IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R50F	<a href="#">Samples</a>
REF5050IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>
REF5050IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	REF 5050	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF REF5020, REF5025, REF5040, REF5050 :**

- Enhanced Product: [REF5020-EP](#), [REF5025-EP](#), [REF5040-EP](#), [REF5050-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5010AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5010IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5010IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5020IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5025IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5030AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5030IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5040IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5045IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REF5050IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

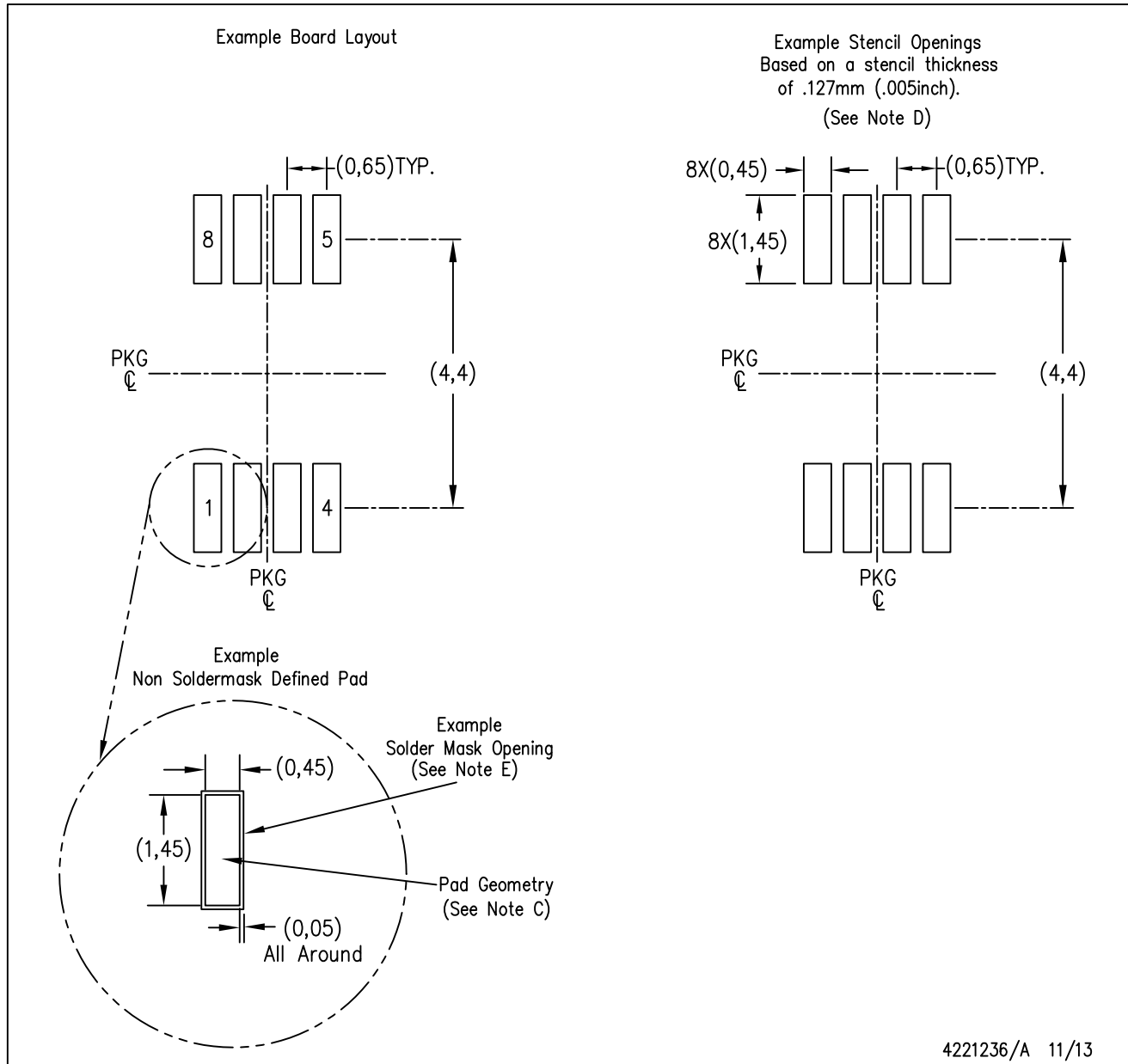
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5010AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5010AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5010IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5010IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5020IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5020IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5020IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5025IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5025IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5025IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5030AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030AIDR	SOIC	D	8	2500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5030IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5030IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5030IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5040IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5040IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5040IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5045IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5045IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5045IDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5050AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5050AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050AIDR	SOIC	D	8	2500	367.0	367.0	35.0
REF5050IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
REF5050IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
REF5050IDR	SOIC	D	8	2500	367.0	367.0	35.0

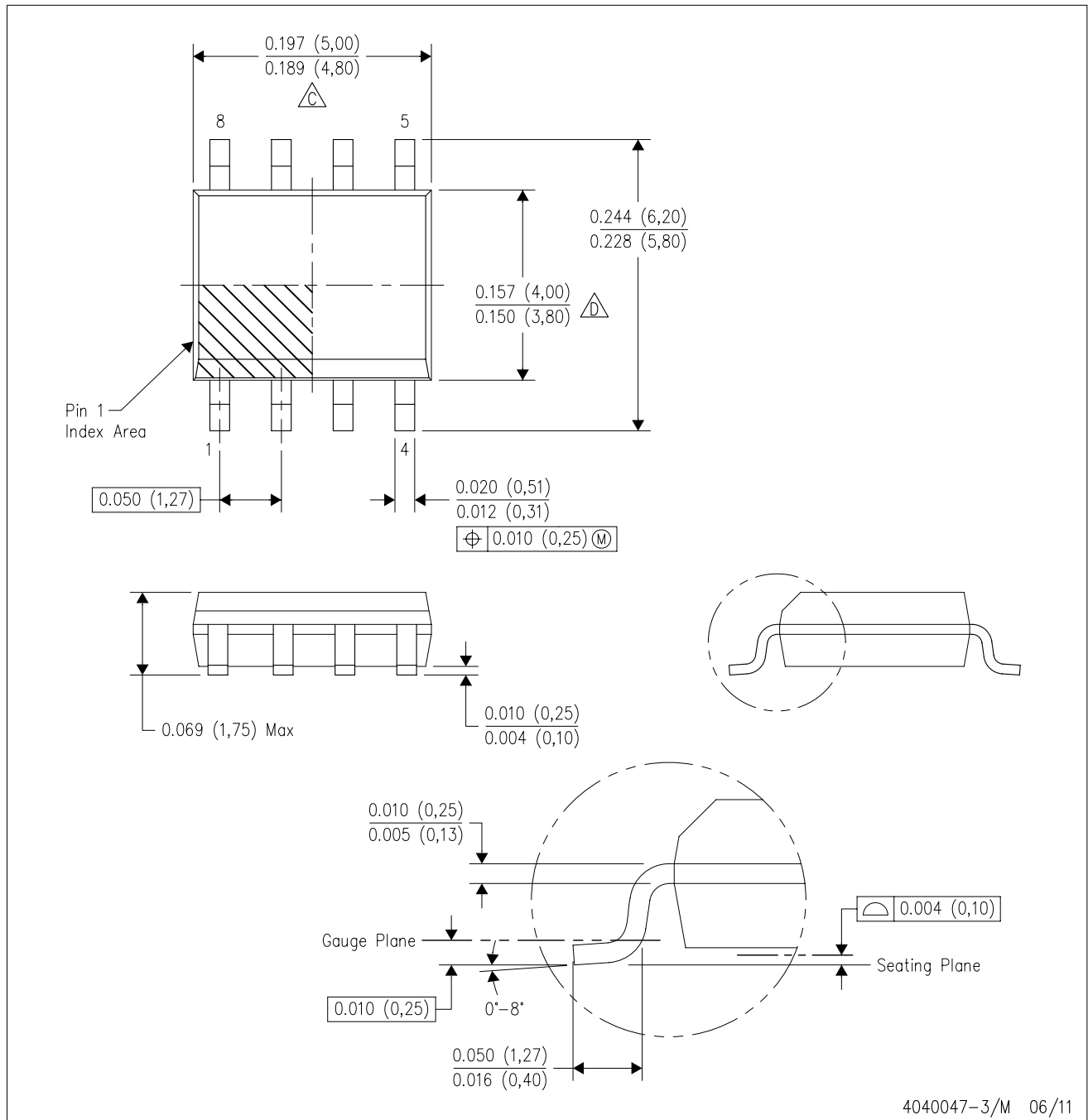




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

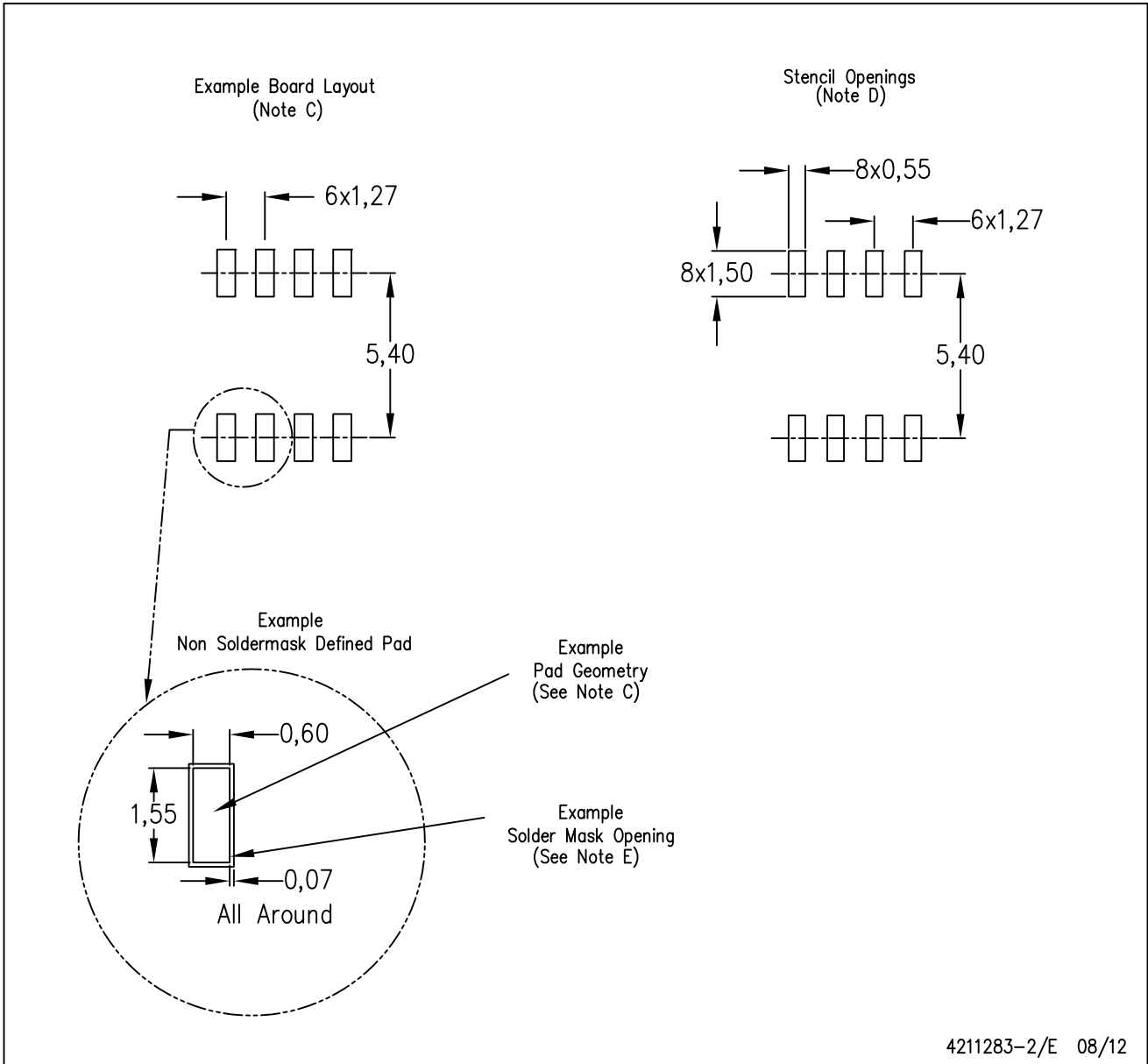


4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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