



Features

- Dual Outputs
(See Ordering Information)
- Ideal Power Source for DSPs
- 12V Input
- Outputs Adjustable
- Remote Sensing (V_{O1} & V_{O2})
- Standby Function
- Soft-Start
- Internal Sequencing
- Short Circuit Protection
- 23-pin Space-Saving Package
- Solderable Copper Case

Description

The PT6980 Excalibur™ series of power modules are dual output integrated switching regulators (ISRs) specifically designed to power mixed signal ICs. Operating from a 12-V input bus, the dual output provides power for both the digital I/O logic and a DSP core from a single module. Both output voltages are internally sequenced during power-up and power-down to comply with the requirements of the latest DSP chips. Each output is independently adjustable or can be set to at least one alternative bus voltage with a simple pin-strap. The modules are made available in a space-saving solderable case. The features include output current limit and short-circuit protection.

Ordering Information

PT6981□ = +2.5/1.8 Volts
PT6982□ = +3.3/2.5 Volts
PT6983□ = +3.3/1.8 Volts
PT6984□ = +3.3/1.2 Volts
PT6985□ = +2.5/1.2 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	N	(ELF)
Horizontal	A	(ELG)
SMD	C	(ELH)

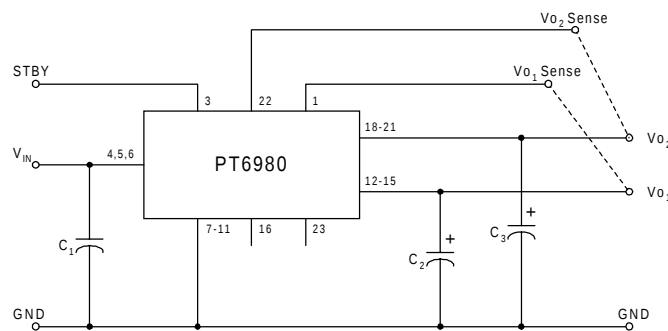
(Reference the applicable package code drawing for the dimensions and PC layout)

Pin-Out Information

Pin	Function	Pin	Function
1	V_{O1} Sense	13	V_{O1}
2	No Connect	14	V_{O1}
3	STBY	15	V_{O1}
4	V_{in}	16	V_{O1} Adjust*
5	V_{in}	17	No Connect
6	V_{in}	18	V_{O2}
7	GND	19	V_{O2}
8	GND	20	V_{O2}
9	GND	21	V_{O2}
10	GND	22	V_{O2} Sense
11	GND	23	V_{O2} Adjust*
12	V_{O1}		

* V_{O1} and V_{O2} can be pin-strapped to another voltage. See application note on output voltage adjustment.

Standard Application



C_1 = Req'd 560μF electrolytic
 C_2 = Req'd 330μF electrolytic
 C_3 = Optional 100μF electrolytic

General Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 12\text{V}$)

Characteristic	Symbol	Conditions	PT6980 Series			Units
			Min	Typ	Max	
Short Circuit Current	I_{sc}	$Io_1 + Io_2$ combined	—	19	—	A
Switching Frequency	f_o	Over V_{in} range	500	550	600	kHz
Standby (Pin 3)		Referenced to GND (pin 7)				
Input High Voltage	V_{IH}		—	—	Open ⁽¹⁾	V
Input Low Voltage	V_{IL}		-0.1	—	+0.4	
Input Low Current	I_{IL}		—	-0.5	—	mA
Standby Input Current	$I_{in\text{ standby}}$	pin 3 to GND	—	4	6	mA
External Output Capacitance	C_2 C_3		330 ⁽²⁾ 0	—	15,000 ⁽²⁾ 330	μF
Maximum Operating Temperature Range	T_a	Over V_{in} Range	-40 ⁽³⁾	—	+85 ⁽⁴⁾	$^\circ\text{C}$
Storage Temperature	T_s	—	-40	—	+125	$^\circ\text{C}$
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, 1/2 Sine, mounted	—	500	—	G's
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2 20-2000 Hz, Soldered in a PC board	—	15	—	G's
Weight	—	Vertical/Horizontal	—	26	—	grams
Flammability	—	Meets UL 94V-O	—	—	—	—

Notes: (1) The Standby (pin 3) has an internal pull-up to V_{in} , and if it is left open circuit the module will operate when input power is applied. Refer to the application notes for interface considerations.

(2) The total combined ESR of all output capacitance at 100kHz must be (less than) $<50\text{ m}\Omega$.

(3) For operating temperatures below 0°C , C_{in} and C_{out} must have stable characteristics. Use either tantalum or Oscon® capacitors.

(4) See Safe Operating Area curves for the specific output voltage combination, or contact the factory for the appropriate derating.

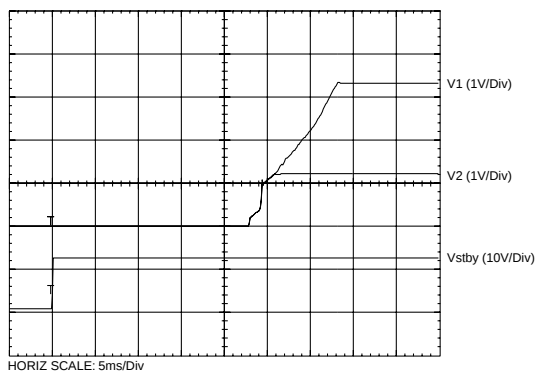
Input/Output Capacitors: The PT6980 series requires a 330 μF electrolytic capacitor at both the input and output for proper operation (300 μF for Oscon® or low ESR tantalum). In addition, the input capacitance must be rated for a minimum of 1.0Arms ripple current. For transient or dynamic load applications, additional capacitance may be required. Refer to the application notes for more information.

Power-up Sequencing and Vo_1/Vo_2 Loading

Power-up Sequencing

The PT6980 series of regulators provide two output voltages, Vo_1 and Vo_2 . Each of the output voltage combinations offered by the PT6980 series provides power for both a low-voltage processor core, and the associated digital support circuitry. In addition, each output is internally sequenced during power-up and power-down to comply with the requirements of most DSP and μP IC's, and their accompanying chipsets. Figure 1 shows the typical waveforms of the output voltages, Vo_1 and Vo_2 , from the instance that either input power is applied or the module is enabled via the Standby pin. Following a delay of about 25 milli-secs, the voltages at Vo_1 and Vo_2 rise together until Vo_2 reaches its set-point. Then Vo_1 continues to rise until both output voltages have reached full voltage.

Figure 1; PT6980 Series Power-up



Vo_1/Vo_2 Loading

The output voltages from the PT6980 series regulators are independently regulated. The voltage at Vo_1 is produced by a highly efficient switching regulator. The lower output voltage, Vo_2 , is derived from Vo_1 . The regulation method used for Vo_2 also provides control of this output voltage during power-down. Vo_2 will sink current if the voltage at Vo_1 attempts to fall below it.

The load specifications for each model of the PT6980 series gives both a 'Typical' (Typ) and 'Maximum' (Max) load current for each output. For operation within the product's rating, the load currents at Vo_1 and Vo_2 must comply with the following limits:-

- Io_2 must be less than $Io_2(\text{max})$.
- The sum-total current from both outputs ($Io_1 + Io_2$) must not exceed $Io_1(\text{max})$.

In the case that either Vo_1 or Vo_2 are adjusted to some other value than the default output voltage, the absolute maximum load current for Io_2 must be revised to comply with the following equation.

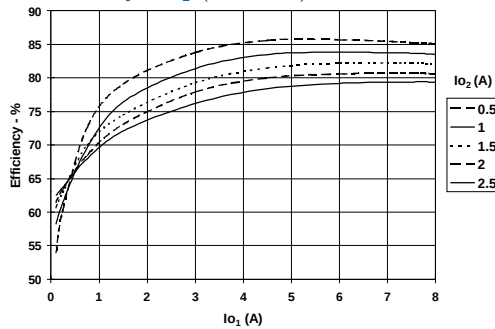
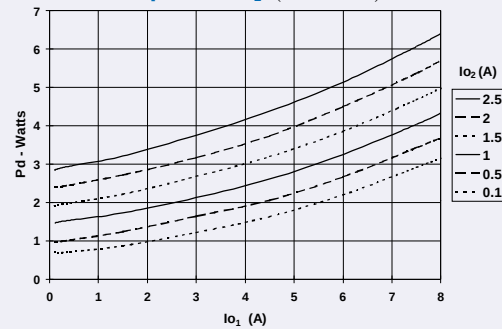
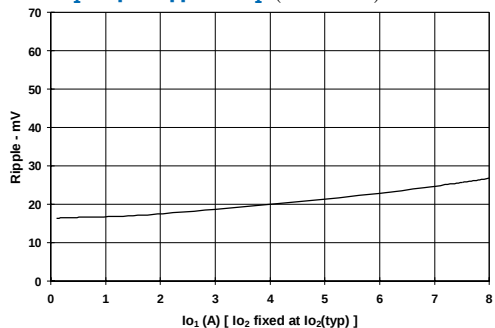
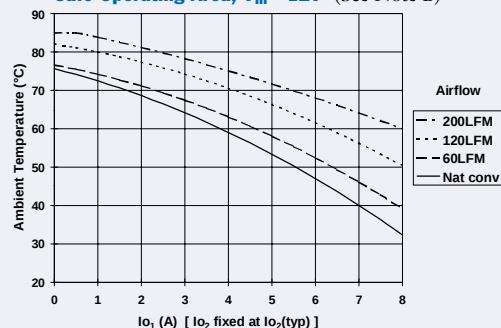
$$Io_2(\text{max}) = \frac{2.5}{Vo_1 - Vo_2} \text{ Adc}$$

Consult the specification table for each model of the series for the actual numeric values.

PT6981 Performance Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 12\text{V}$, $C_1 = 560\mu\text{F}$, $C_2 = 330\mu\text{F}$, $I_{O1} = I_{O1typ}$, and $I_{O2} = I_{O2typ}$)

Characteristic	Symbol	Conditions	PT6981 (2.5V/1.8V)			Units
			Min	Typ	Max	
Output Current	I_{O1}	$T_a = 25^\circ\text{C}$, natural convection	0.1 (i)	8 (ii)	10.5 (iii)	A
	I_{O2}		0	2.5 (ii)	2.5 (iii)	
	I_{O1}	$T_a = 60^\circ\text{C}$, 200LFM airflow	0.1 (i)	8 (ii)	10.5 (iii)	A
	I_{O2}		0	2.5 (ii)	2.5 (iii)	
Input Voltage Range	V_{in}	Over I_O Range	10.8	—	13.2	VDC
Set Point Voltage Tolerance	$V_o \text{ tol}$		V_{O1} — V_{O2} —	± 12 ± 9	± 38 ± 27	mV
Temperature Variation	Reg_{temp}	$-40^\circ > T_a > +85^\circ\text{C}$	V_{O1} — V_{O2} —	± 0.5 ± 0.5	—	% V_o
Line Regulation	Reg_{line}	Over V_{in} range	V_{O1} — V_{O2} —	± 10 ± 5	± 15 ± 7	mV
Load Regulation	Reg_{load}	Over I_O range	V_{O1} — V_{O2} —	± 10 ± 5	± 15 ± 7	mV
Total Output Voltage Variation	ΔV_{otot}	Includes set-point, line, load $-40^\circ > T_a > +85^\circ\text{C}$	V_{O1} — V_{O2} —	± 44 ± 28	—	mV
Efficiency	η		—	80	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	V_{O1} — V_{O2} —	35 35	—	mV _{pp}
Transient Response	t_{tr}	1A/ μs load step, 50% to 100% I_{Otyp}	—	60	—	μs
	ΔV_{tr}	V_o over/undershoot	V_{O1} — V_{O2} —	± 50 ± 20	—	mV

Notes: (i) $I_{O1(min)}$ current of 0.1A can be divided between both outputs, V_{O1} or V_{O2} . The module will operate at no load with reduced specifications.
(ii) The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.
(iii) The sum of I_{O1} and I_{O2} must be less than I_{O1max} , and I_{O2} must be less than I_{O2max} .

PT6981 Typical Characteristics**Efficiency vs I_{O1}** (See Note A)**Power Dissipation vs I_{O1}** (See Note A) **V_{O1} Output Ripple vs I_{O1}** (See Note A)**Safe Operating Area, $V_{in} = 12\text{V}$** (See Note B)

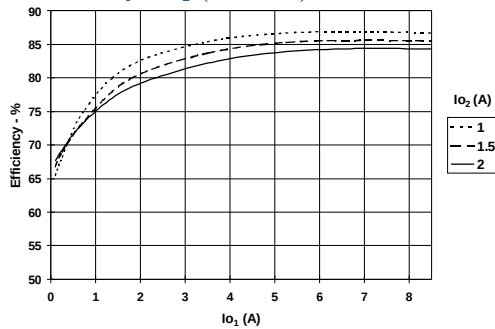
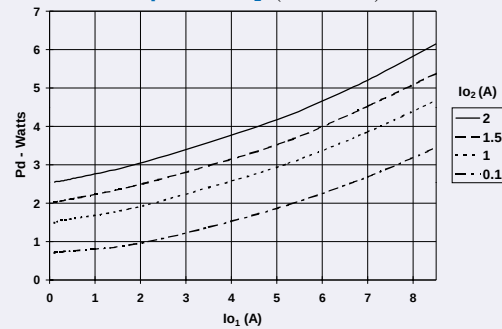
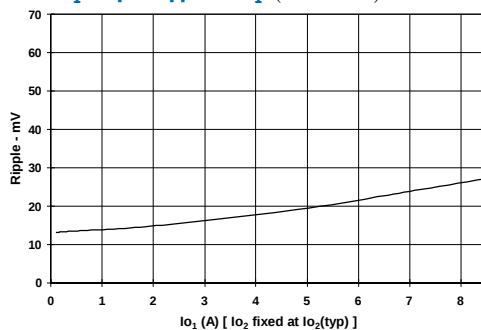
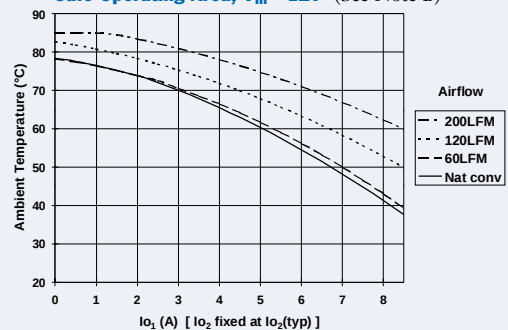
Note A: Characteristic data has been developed from actual products tested at 25°C . This data is considered typical data for the Converter.

Note B: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures.

PT6982 Performance Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 12\text{V}$, $C_1 = 560\mu\text{F}$, $C_2 = 330\mu\text{F}$, $I_{O1} = I_{O1typ}$, and $I_{O2} = I_{O2typ}$)

Characteristic	Symbol	Conditions		PT6982 (3.3V/2.5V)			Units
				Min	Typ	Max	
Output Current	I_{O1}	$T_a = 25^\circ\text{C}$, natural convection	$V_{O1} (3.3\text{V})$	0.1 (i)	8.5 (ii)	10.5 (iii)	A
	I_{O2}		$V_{O2} (2.5\text{V})$	0	2 (ii)	2.25 (iii)	
	I_{O1}	$T_a = 60^\circ\text{C}$, 200LFM airflow	$V_{O1} (3.3\text{V})$	0.1 (i)	8.5 (ii)	10.5 (iii)	A
	I_{O2}		$V_{O2} (2.5\text{V})$	0	2 (ii)	2.25 (iii)	
Input Voltage Range	V_{in}	Over I_O Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	$V_o \text{ tol}$		V_{O1}	—	± 16	± 50	mV
			V_{O2}	—	± 12	± 38	
Temperature Variation	Reg_{temp}	$-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 1.0	—	% V_o
			V_{O2}	—	± 0.5	—	
Line Regulation	Reg_{line}	Over V_{in} range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Load Regulation	Reg_{load}	Over I_O range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 10	± 13	
Total Output Voltage Variation	ΔV_{otot}	Includes set-point, line, load $-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 69	—	mV
			V_{O2}	—	± 39	—	
Efficiency	η			—	84	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	V_{O1}	—	35	—	mV _{pp}
			V_{O2}	—	35	—	
Transient Response	t_{tr}	1A/ μs load step, 50% to 100% I_{Otyp}		—	60	—	μs
	ΔV_{tr}	V_o over/undershoot	V_{O1}	—	± 50	—	mV
			V_{O2}	—	± 30	—	

Notes: (i) $I_{O1(min)}$ current of 0.1A can be divided between both outputs, V_{O1} or V_{O2} . The module will operate at no load with reduced specifications.
(ii) The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.
(iii) The sum of I_{O1} and I_{O2} must be less than I_{O1max} , and I_{O2} must be less than I_{O2max} .

PT6982 Typical Characteristics**Efficiency vs I_{O1}** (See Note A)**Power Dissipation vs I_{O1}** (See Note A) **V_{O1} Output Ripple vs I_{O1}** (See Note A)**Safe Operating Area, $V_{in} = 12\text{V}$** (See Note B)

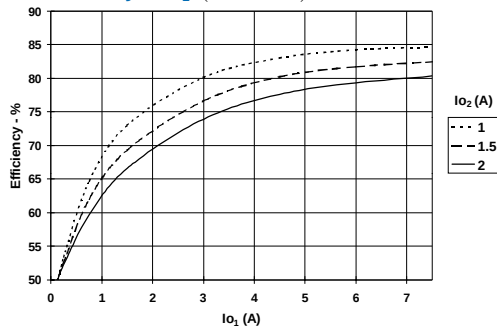
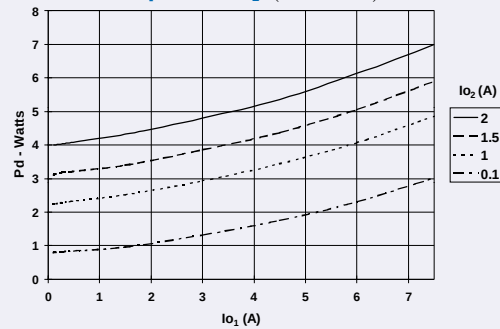
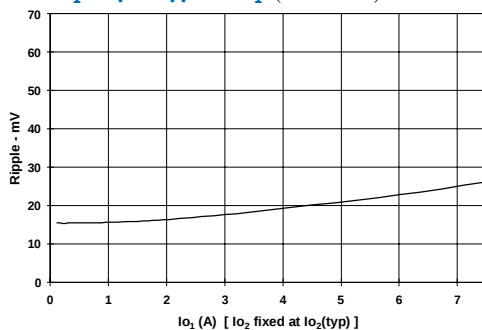
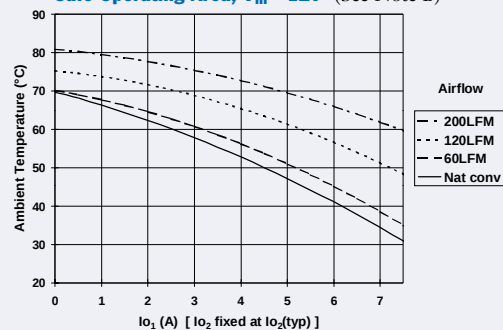
Note A: Characteristic data has been developed from actual products tested at 25°C . This data is considered typical data for the Converter.

Note B: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures.

PT6983 Performance Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 12\text{V}$, $C_1 = 560\mu\text{F}$, $C_2 = 330\mu\text{F}$, $I_{O1} = I_{O1typ}$, and $I_{O2} = I_{O2typ}$)

Characteristic	Symbol	Conditions		PT6983 (3.3V/1.8V)			Units
				Min	Typ	Max	
Output Current	I_{O1}	$T_a = 25^\circ\text{C}$, natural convection	V_{O1} (3.3V)	0.1 (i)	7.5 (ii)	9.5 (iii)	A
	I_{O2}		V_{O2} (1.8V)	0	2 (ii)	2 (iii)	
	I_{O1}	$T_a = 60^\circ\text{C}$, 200LFM airflow	V_{O1} (3.3V)	0.1 (i)	7.5 (ii)	9.5 (iii)	A
	I_{O2}		V_{O2} (1.8V)	0	2 (ii)	2 (iii)	
Input Voltage Range	V_{in}	Over I_O Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	V_O tol		V_{O1}	—	± 16	± 50	mV
			V_{O2}	—	± 9	± 27	
Temperature Variation	Reg_{temp}	$-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 1.0	—	% V_O
			V_{O2}	—	± 0.5	—	
Line Regulation	Reg_{line}	Over V_{in} range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Load Regulation	Reg_{load}	Over I_O range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Total Output Voltage Variation	ΔV_{Otot}	Includes set-point, line, load $-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 69	—	mV
			V_{O2}	—	± 28	—	
Efficiency	η			—	81	—	%
V_O Ripple (pk-pk)	V_r	20MHz bandwidth	V_{O1}	—	35	—	mV _{pp}
			V_{O2}	—	35	—	
Transient Response	t_{tr}	1A/ μs load step, 50% to 100% I_{Otyp}		—	60	—	μs
	ΔV_{tr}	V_O over/undershoot	V_{O1}	—	± 50	—	mV
			V_{O2}	—	± 20	—	

Notes: (i) $I_{O1(min)}$ current of 0.1A can be divided between both outputs, V_{O1} or V_{O2} . The module will operate at no load with reduced specifications.
(ii) The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.
(iii) The sum of I_{O1} and I_{O2} must be less than I_{O1max} , and I_{O2} must be less than I_{O2max} .

PT6983 Typical Characteristics**Efficiency vs I_{O1}** (See Note A)**Power Dissipation vs I_{O1}** (See Note A) **V_{O1} Output Ripple vs I_{O1}** (See Note A)**Safe Operating Area, $V_{in} = 12\text{V}$** (See Note B)

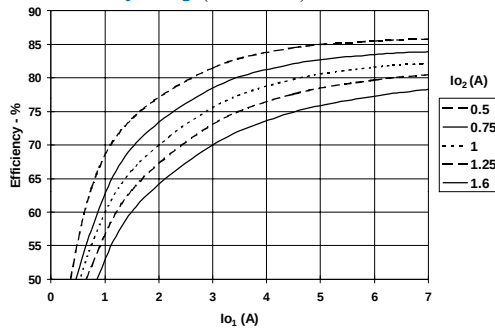
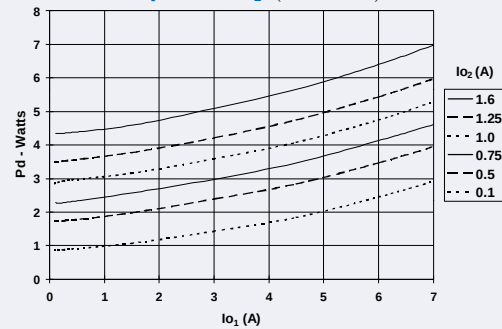
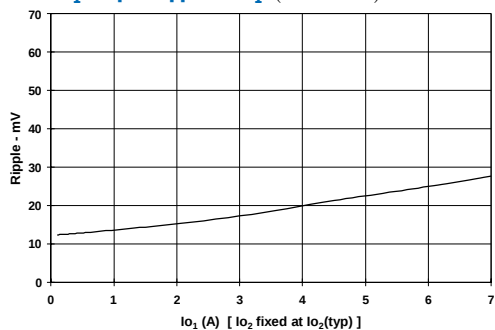
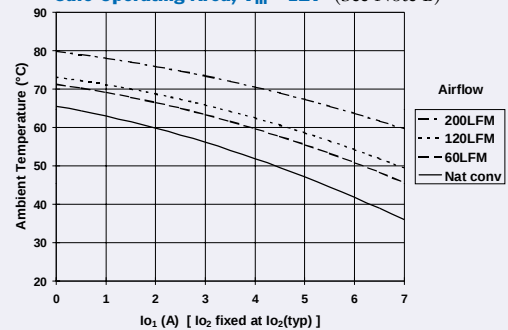
Note A: Characteristic data has been developed from actual products tested at 25°C . This data is considered typical data for the Converter.

Note B: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures

PT6984 Performance Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 12\text{V}$, $C_1 = 560\mu\text{F}$, $C_2 = 330\mu\text{F}$, $I_{O1} = I_{O1typ}$, and $I_{O2} = I_{O2typ}$)

Characteristic	Symbol	Conditions		PT6984 (3.3V/1.2V)			Units
				Min	Typ	Max	
Output Current	I_{O1}	$T_a = 25^\circ\text{C}$, natural convection	$V_{O1} (3.3\text{V})$	0.1 (i)	7 (ii)	8.6 (iii)	A
	I_{O2}		$V_{O2} (1.2\text{V})$	0	1.6 (ii)	1.6 (iii)	
	I_{O1}	$T_a = 60^\circ\text{C}$, 200LFM airflow	$V_{O1} (3.3\text{V})$	0.1 (i)	7 (ii)	8.6 (iii)	A
	I_{O2}		$V_{O2} (1.2\text{V})$	0	1.6 (ii)	1.6 (iii)	
Input Voltage Range	V_{in}	Over I_O Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	$V_O \text{ tol}$		V_{O1}	—	± 16	± 50	mV
			V_{O2}	—	± 6	± 18	
Temperature Variation	Reg_{temp}	$-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 1.0	—	% V_O
			V_{O2}	—	± 0.5	—	
Line Regulation	Reg_{line}	Over V_{in} range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Load Regulation	Reg_{load}	Over I_O range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Total Output Voltage Variation	ΔV_{otot}	Includes set-point, line, load $-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 69	—	mV
			V_{O2}	—	± 22	—	
Efficiency	η			—	78	—	%
V_O Ripple (pk-pk)	V_r	20MHz bandwidth	V_{O1}	—	35	—	mV _{pp}
			V_{O2}	—	35	—	
Transient Response	t_{tr}	1A/ μs load step, 50% to 100% I_{Otyp}		—	60	—	μs
	ΔV_{tr}	V_O over/undershoot	V_{O1}	—	± 50	—	
			V_{O2}	—	± 20	—	mV

Notes: (i) $I_{O1(min)}$ current of 0.1A can be divided between both outputs, V_{O1} or V_{O2} . The module will operate at no load with reduced specifications.
(ii) The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.
(iii) The sum of I_{O1} and I_{O2} must be less than I_{O1max} , and I_{O2} must be less than I_{O2max} .

PT6984 Typical Characteristics**Efficiency vs I_{O1}** (See Note A)**Power Dissipation vs I_{O1}** (See Note A) **V_{O1} Output Ripple vs I_{O1}** (See Note A)**Safe Operating Area, $V_{in} = 12\text{V}$** (See Note B)

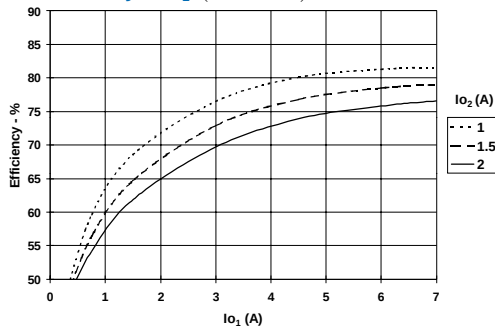
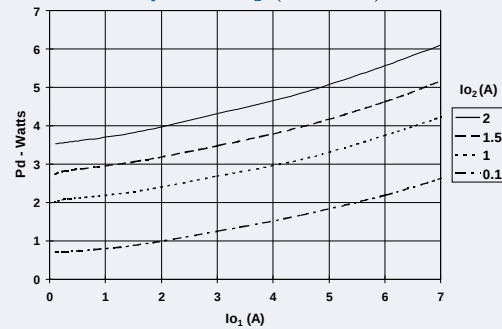
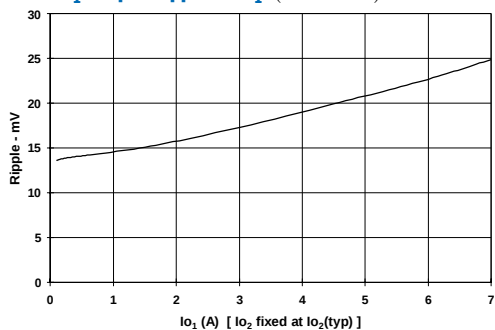
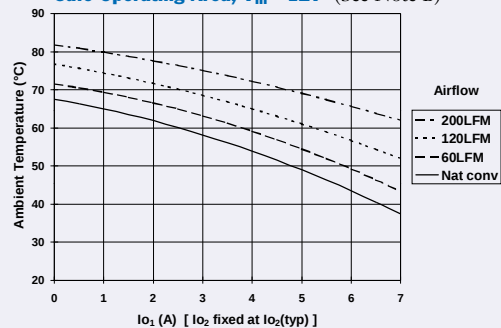
Note A: Characteristic data has been developed from actual products tested at 25°C . This data is considered typical data for the Converter.

Note B: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures.

PT6985 Performance Specifications (Unless otherwise stated, $T_a = 25^\circ\text{C}$, $V_{in} = 12\text{V}$, $C_1 = 560\mu\text{F}$, $C_2 = 330\mu\text{F}$, $I_{O1} = I_{O1typ}$, and $I_{O2} = I_{O2typ}$)

Characteristic	Symbol	Conditions		PT6985 (2.5V/1.2V)			Units
				Min	Typ	Max	
Output Current	I_{O1}	$T_a = 25^\circ\text{C}$, natural convection	$V_{O1} (2.5\text{V})$	0.1 (i)	7 (ii)	9 (iii)	A
	I_{O2}		$V_{O2} (1.2\text{V})$	0	2 (ii)	2.2 (iii)	
	I_{O1}	$T_a = 60^\circ\text{C}$, 200LFM airflow	$V_{O1} (2.5\text{V})$	0.1 (i)	7 (ii)	9 (iii)	A
	I_{O2}		$V_{O2} (1.2\text{V})$	0	2 (ii)	2.2 (iii)	
Input Voltage Range	V_{in}	Over I_O Range		10.8	—	13.2	VDC
Set Point Voltage Tolerance	$V_o \text{ tol}$		V_{O1}	—	± 12	± 38	mV
			V_{O2}	—	± 6	± 18	
Temperature Variation	Reg_{temp}	$-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 0.5	—	% V_o
			V_{O2}	—	± 0.5	—	
Line Regulation	Reg_{line}	Over V_{in} range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Load Regulation	Reg_{load}	Over I_O range	V_{O1}	—	± 10	± 15	mV
			V_{O2}	—	± 5	± 7	
Total Output Voltage Variation	ΔV_{otot}	Includes set-point, line, load $-40^\circ > T_a > +85^\circ\text{C}$	V_{O1}	—	± 44	—	mV
			V_{O2}	—	± 22	—	
Efficiency	η			—	77	—	%
V_o Ripple (pk-pk)	V_r	20MHz bandwidth	V_{O1}	—	35	—	mV _{pp}
			V_{O2}	—	35	—	
Transient Response	t_{tr}	1A/ μs load step, 50% to 100% I_{Otyp}		—	60	—	μs
	ΔV_{tr}	V_o over/undershoot	V_{O1}	—	± 50	—	
			V_{O2}	—	± 20	—	mV

Notes: (i) $I_{O1(min)}$ current of 0.1A can be divided between both outputs, V_{O1} or V_{O2} . The module will operate at no load with reduced specifications.
(ii) The typical current is that which can be drawn simultaneously from both outputs under the stated operating conditions.
(iii) The sum of I_{O1} and I_{O2} must be less than I_{O1max} , and I_{O2} must be less than I_{O2max} .

PT6985 Typical Characteristics**Efficiency vs I_{O1}** (See Note A)**Power Dissipation vs I_{O1}** (See Note A) **V_{O1} Output Ripple vs I_{O1}** (See Note A)**Safe Operating Area, $V_{in} = 12\text{V}$** (See Note B)

Note A: Characteristic data has been developed from actual products tested at 25°C . This data is considered typical data for the Converter.

Note B: SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures

Capacitor Recommendations for the Dual-Output PT6980 Regulator Series

Input Capacitors:

The recommended input capacitance is determined by 1.0 ampere minimum ripple current rating and 330µF minimum capacitance. Ripple current and <100mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of 2 × the maximum DC voltage + AC ripple. This is necessary to insure reliability for input voltage bus applications.

Output Capacitors: C₂(Required), C₃(Optional)

The ESR of the required capacitor (C₂) must not be greater than 50mΩ. Electrolytic capacitors have poor ripple performance at frequencies greater than 400kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions. Preferred low ESR type capacitor part numbers are identified in Table 1. The optional 100µF capacitor (C₃) for V₂out can have an ESR of up to 200mΩ for optimum performance and ripple reduction. (Note: Vendor part numbers for the optional capacitor, C₃, are not identified in the table. Use the same series selected for C₂)

Tantalum Capacitors

Tantalum type capacitors may be used at the output, but only the AVX TPS series, Sprague 593D/594/595 series, or Kemet T495/T510 series. The AVX TPS series, Kemet or Sprague series tantalums are recommended over many other types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation and lower ripple current capability. The TAJ Series is also less reliable than the AVX TPS series when determining power dissipation capability. Tantalum or Oscon® types are recommended for applications where ambient temperatures fall below 0°C.

Capacitor Table

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (Equivalent Series Resistance at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 1: Input/Output Capacitors

Capacitor Vendor/ Component Series	Capacitor Characteristics					Quantity		Vendor Number
	Working Voltage	Value(µF)	(ESR) Equivalent Series Resistance	85°C Maximum Ripple Current(Irms)	Physical Size(mm)	Input Bus	Output Bus	
Panasonic FC	35V	680µF	0.043Ω	1690mA	16x15	1	1	EEUFC1V681S
	35V	560µF	0.038Ω	1655mA	12.5x20	1	1	EEUFC1V561S
	50V	680µF	0.048Ω	1835mA	16x20	1	1	EEUFC1H681
United Chemi-con LXV/LXZ/FX/FS	35V	680µF	0.038Ω	1660mA	12.5x20	1	1	LXZ35VB681M112X20LL
	50V	680µF	0.048Ω	1840mA	16x20	1	1	LXZ50VB681M16X20LL
	10V	390µF	0.030Ω	3080mA	8x10.5	N/R	1	10FX390M
	20V	150µF	0.024Ω	3200mA	8x10.5	4	2	20FX150M
Nichicon PL/PM	35V	560µF	0.048Ω	1360mA	16x15	1	1	UPL1V561MHH6
	25V	820µF	0.049Ω	1340mA	16x15	1	1	UPL1E821MHH6
	35V	560µF	0.0048Ω	1360mA	16x15	1	1	UPM1V561MHH6
Panasonic FC Surface Mtg	35V	330µF	0.065±2Ω	>1205mA	12.5x16.5	2	2	EEVFC1V331LQ
	35V	1000µF	0.038Ω	2000mA	18x16.5	1	1	EEVFC1V1021N
	35V	470µF	0.043Ω	1690mA	16x16.5	1	1	EEVFC1V471N
Oscon SS/SV	10V	330µF	0.025Ω	>3500mA	10.0x10.5	N/R	1	10SS330M
	10V	330µF	0.025Ω	>3800mA	10.3x10.3	N/R	1	10SV330M Surface Mount(SV)
AVX Tantalum TPS	10V	330µF	0.060±2Ω	>2500mA	7.3Lx	N/R	2	TPSV337M010R0060
	10V	220µF	0.060±2Ω	>3000mA	4.3Wx	N/R	2	TPSV227M010R0060
Kemet T510 T495	10V	330µF	0.033Ω	1400mA	7.3Lx5.7W x 4.0H	N/R	1	T510X337M010AS
	10V	220µF	0.07Ω±2 =0.035Ω	>2000mA		N/R	2	T495X227M010AS
Sprague 594D	10V	330µF	0.045Ω	2350mA	7.3Lx 6.0Wx 4.1H	N/R	1	594D337X0010R2T

N/R –Not recommended. The voltage rating does not meet the minimim operating limits.

Adjusting the Output Voltage of the PT6980 Dual-Output Voltage Regulators

Each output voltage from the PT6980 series of integrated switching regulators (ISRs) can be independently adjusted higher or lower than the factory trimmed pre-set voltage. The voltages, V_{O1} and V_{O2} may be adjusted either up or down using a single external resistor ¹. Table 1 gives the adjustment range for both V_{O1} and V_{O2} for each model in the series as $V_a(\text{min})$ and $V_a(\text{max})$. Note that V_{O2} must always be lower than V_{O1} ².

V_{O1} Adjust Up: To increase the output, add a resistor R_4 between pin 16 (V_1 Adjust) and pins 7-11 (GND) ¹.

V_{O1} Adjust Down: Add a resistor (R_3), between pin 16 (V_{O1} Adjust) and pin 1 (V_{O1} Sense) ¹.

V_{O2} Adjust Up: Add a resistor R_2 between pin 23 (V_{O2} Adjust) and pins 7-11 (GND) ¹.

V_{O2} Adjust Down: Add a resistor (R_1) between pin 23 (V_{O2} Adjust) and pin 22 (V_{O2} Sense) ¹.

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor.

Notes:

1. Use only a single 1% resistor in either the (R_3) or R_4 location to adjust V_{O1} , and in the (R_1) or R_2 location to adjust V_{O2} . Place the resistor as close to the ISR as possible.
2. V_{O2} must always be at least 0.2V lower than V_{O1} .

3. Both the V_{O1} and V_{O2} may be adjusted down to an alternative bus voltage by making, (R_3) or (R_1) respectively, a zero ohm link. Refer to the Table 1 footnotes for guidance.
4. Never connect capacitors to either the V_{O1} Adjust or V_{O2} Adjust pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.
5. Adjusting either voltage (V_{O1} or V_{O2}) may increase the power dissipation in the regulator, and change the maximum current available at either output. Consult the note on p.2 of the data sheet regarding V_{O1}/V_{O2} loading.

The adjust up and adjust down resistor values can also be calculated using the following formulas. Be sure to select the correct formula parameter from Table 1 for the output and model being adjusted.

$$(\mathbf{R_1}) \text{ or } (\mathbf{R_3}) = \frac{10(V_a - V_r)}{V_o - V_a} - R_s \quad \text{k}\Omega$$

$$(\mathbf{R_2}) \text{ or } (\mathbf{R_4}) = \frac{10 \cdot V_r}{V_a - V_o} - R_s \quad \text{k}\Omega$$

Where: V_o = Original output voltage, (V_{O1} or V_{O2})
 V_a = Adjusted output voltage
 V_r = The reference voltage from Table 1
 R_s = The series resistance from Table 1

Figure 1

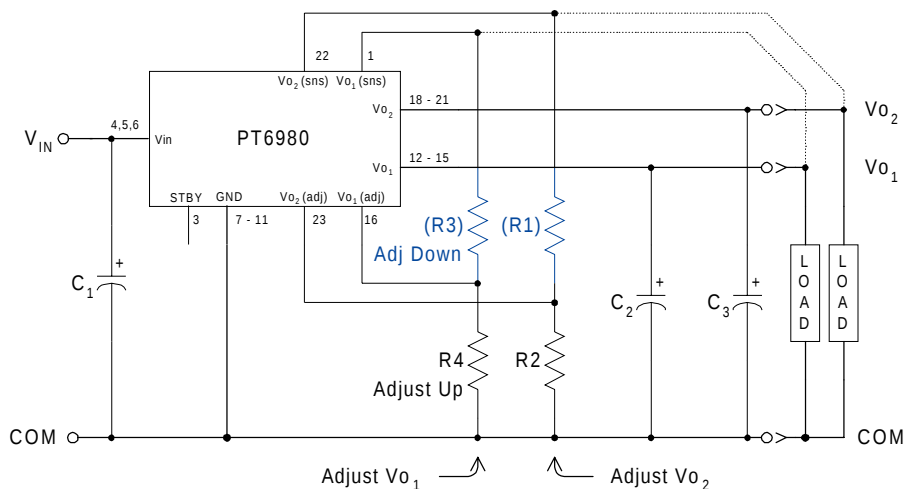


Table 1

ADJUSTMENT RANGE AND FORMULA PARAMETERS

Vo ₁ Bus			Vo ₂ Bus (2)		
Series Pt #	PT6981/85	PT6982/83/84	PT6984/85	PT6981/83	PT6936
Adj. Resistor	(R3)/R4	(R3)/R4	(R1)/R2	(R1)/R2	(R1)/R2
V _o (nom)	2.5V	3.3V	1.2V	1.8V	2.5V
V _a (min)	1.8V *	2.5V *	1.0V †	1.5V †	1.8V †
V _a (max)	3.6V	3.6V	1.5V #	2.4V	3.0
V _r	1.27V	1.27V	0.6125V	1.0V	1.0V
R _s (kΩ)	7.5	15.4	20.0	16.9	11.5

Ref. Note 3: * (R3) = Zero-ohm link
† (R1) = Zero-ohm link
(R2) = Zero-ohm link

Table 2

ADJUSTMENT RESISTOR VALUES

Vo ₁ Bus			Vo ₂ Bus			
Series Pt #	PT6981/85	PT6982/83/84	Series Pt #	PT6984/85	PT6981/83	PT6982
Adj. Resistor	(R3)/R4	(R3)/R4	Adj. Resistor	(R1)/R2	(R1)/R2	(R1)/R2
V _o (nom)	2.5V	3.3V	V _o (nom)	1.2V	1.8V	2.5V
V _a (req'd)			V _a (req'd)			
1.8	(0.0)		1.0	(0.0)kΩ		
1.85	(1.4)kΩ		1.05	(9.2)kΩ		
1.9	(3.0)kΩ		1.1	(28.8)kΩ		
1.95	(4.9)kΩ		1.15	(87.5)kΩ		
2.0	(7.1)kΩ		1.2			
2.05	(9.8)kΩ		1.25	101.5kΩ		
2.1	(13.3)kΩ		1.3	41.2kΩ		
2.2	(23.5)kΩ		1.35	20.8kΩ		
2.3	(44.0)kΩ		1.4	10.6kΩ		
2.4	(106.0)kΩ		1.45	4.5kΩ		
2.5		(0.0)kΩ	1.5	0.0kΩ	(0.0)kΩ	
2.6	120.0kΩ	(3.6)kΩ	1.55		(5.1)kΩ	
2.7	56.0kΩ	(8.4)kΩ	1.6		(13.1)kΩ	
2.8	34.8kΩ	(15.2)kΩ	1.65		(26.4)kΩ	
2.9	24.3kΩ	(25.4)kΩ	1.7		(53.1)kΩ	
3.0	17.9kΩ	(42.3)kΩ	1.75		(133.0)kΩ	
3.1	13.7kΩ	(76.1)kΩ	1.8			(0.0)kΩ
3.2	10.6kΩ	(178.0)kΩ	1.85		183.0kΩ	(1.6)kΩ
3.3	8.4kΩ		1.9		83.1kΩ	(3.5)kΩ
3.4	6.6kΩ	112.0k	1.95		49.8kΩ	(5.8)kΩ
3.5	5.2kΩ	48.1k	2.0		33.1kΩ	(8.5)kΩ
3.6	4.1kΩ	26.9k	2.05		23.1kΩ	(11.8)kΩ
			2.1		16.4kΩ	(16.0)kΩ
			2.2		8.1kΩ	(28.5)kΩ
			2.3		3.1kΩ	(53.5)kΩ
			2.4		0.0kΩ	(129.0)kΩ
			2.5			
			2.6			88.5kΩ
			2.7			38.5kΩ
			2.8			21.8kΩ
			2.9			13.5kΩ
			3.0			8.5kΩ

R₁/R₃ = (Blue), R₂/R₄ = Black

Using the Standby Function on the PT6980 Series of Dual-Output Voltage Regulators

Both output voltages of the 23-pin PT6980 dual-output converter may be disabled using the regulator's 'Standby' function. This function may be used in applications that require power-up/shutdown sequencing, or wherever there is a requirement to control the output voltage On/Off status with external circuitry.

The standby function is provided by the *STBY** control (pin 3). If pin 3 is left open-circuit the regulator operates normally, and provides a regulated output at both V_{O1} (pins 12–15) and V_{O2} (pins 18–21) whenever a valid supply voltage is applied to V_{in} (pins 4, 5, & 6) with respect to GND (pins 7–11). If a low voltage¹ is then applied to pin-3 both regulator outputs will be simultaneously disabled and the input current drawn by the ISR will drop to a typical value of 4mA. The standby control may also be used to hold-off both regulator outputs during the period that input power is applied.

The standby pin is ideally controlled using an open-collector (or open-drain) discrete transistor (See Figure 1). The open-circuit voltage is the input voltage $+V_{in}$. Table 1 gives the circuit parameters for this control input.

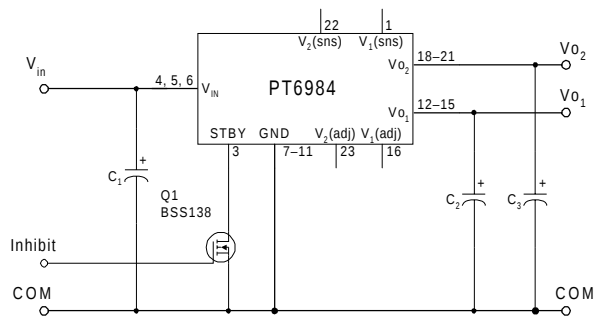
Table 1 Standby Control Parameters^{1, 2}

Parameter	Min	TYP	Max
Enable (V_{IH})	—	—	Open circuit
Disable (V_{IL})	-0.1V	—	0.4V ¹
V_{STBY} (open circuit)	—	$+V_{in}$ ²	—
I_{STBY} (I_{IL})	—	—	-0.5mA

Notes:

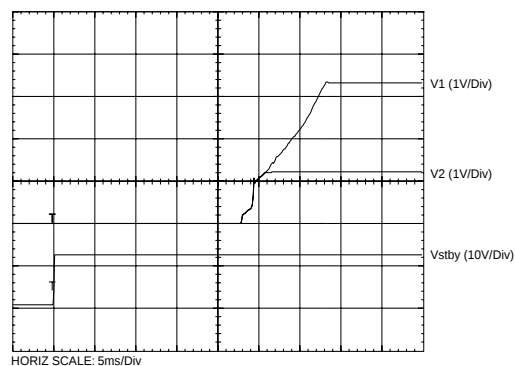
- The standby control input is Not compatible with TTL or other devices that incorporate a totem-pole output drive. Use only a true open-collector device, preferably a discrete bipolar transistor (or MOSFET). To ensure the regulator output is disabled, the control pin must be pulled to less than 0.4Vdc with a low-level 0.5mA sink to ground.
- The standby control input requires no external pull-up resistor. The open-circuit voltage of the *STBY** pin is the input voltage $+V_{in}$.
- When the regulator output is disabled the current drawn from the input source is typically reduced to 4mA.

Figure 1



Turn-On Time: Turning Q_1 in Figure 1 off removes the low-voltage signal at pin 3 and enables the PT6980 series regulator. Following a delay of about 25ms, V_{O1} and V_{O2} rise together until the lower voltage, V_{O2} , reaches its set output. V_{O1} continues to rise until both outputs reach full regulation voltage. The total power-up time is less than 40ms, and is relatively independent of load, temperature, and output capacitance. Figure 2 shows waveforms of the output voltages, V_{O1} and V_{O2} , for a PT6984 (3.3V/1.2V). The turn-off of Q_1 corresponds to the rise in V_{STBY} . The waveforms were measured with a 12V input voltage, and with resistive loads of 5A and 1.25A at the V_{O1} and V_{O2} outputs respectively.

Figure 2



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PT6983N	LIFEBUY	SIP MODULE	ELF	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type	
PT6984N	LIFEBUY	SIP MODULE	ELF	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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