PIC18F2455/2550/4455/4550 Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39632**C**), the following clarifications and corrections should be noted. Any silicon issues for the PIC18F2455/2550/4455/4550 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Timer1 Module

The Real-Time Clock application example, cited in **Section 12.6 "Using Timer1 as a Real-Time Clock,"** has changed.

"Example 12-1: Implementing a Real-Time Clock Using a Timer1 Interrupt Service" is corrected to the following example.

EXAMPLE 12-1: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

```
RTCinit
            MOVLW   80h             ; Preload TMR1 register pair
            MOVWF   TMR1H           ; for 1 second overflow
            CLRF    TMR1L
            MOVLW   b'00001111'     ; Configure for external clock,
            MOVWF   T1CON           ; Asynchronous operation, external oscillator
            CLRF    secs            ; Initialize timekeeping registers
            CLRF    mins            ;
            MOVLW   .12
            MOVWF   hours
            BSF     PIE1, TMR1IE    ; Enable Timer1 interrupt
            RETURN
RTCisr
                                    ; Insert the next 4 lines of code when TMR1
                                    ; can not be reliably updated before clock pulse goes low
            BTFSC   TMR1L,0         ; wait for TMR1L to become clear
            BRA     $-2             ; (may already be clear)
            BTFSS   TMR1L,0         ; wait for TMR1L to become set
            BRA     $-2             ; TMR1 has just incremented
                                    ; If TMR1 update can be completed before clock pulse goes low
                                    ; Start ISR here
            BSF     TMR1H, 7        ; Preload for 1 sec overflow
            BCF     PIR1, TMR1IF    ; Clear interrupt flag
            INCF    secs, F         ; Increment seconds
            MOVLW   .59             ; 60 seconds elapsed?
            CPFSGT  secs
            RETURN                  ; No, done
            CLRF    secs            ; Clear seconds
            INCF    mins, F         ; Increment minutes
            MOVLW   .59             ; 60 minutes elapsed?
            CPFSGT  mins
            RETURN                  ; No, done
            CLRF    mins            ; clear minutes
            INCF    hours, F        ; Increment hours
            MOVLW   .23             ; 24 hours elapsed?
            CPFSGT  hours
            RETURN                  ; No, done
            CLRF    hours           ; Reset hours
            RETURN                  ; Done
```

2. Module: Timer1 Module

The following text, **Section 12.7 "Considerations in Asynchronous Counter Mode"**, is new. It defines the proper method to update the TMR1 registers in Asynchronous mode.

Section 12.7 is located after **Section 12.6 "Using Timer1 as a Real-Time Clock"** in the data sheet.

12.7 Considerations in Asynchronous Counter Mode

Following a Timer1 interrupt and an update to the TMR1 registers, the Timer1 module uses a falling edge on its clock source to trigger the next register update on the rising edge. If the update is completed after the clock input has fallen, the next rising edge will not be counted.

If the application can reliably update TMR1 before the timer input goes low, no additional action is needed. Otherwise, an adjusted update can be performed following a later Timer1 increment. This can be done by monitoring TMR1L within the interrupt routine until it increments, and then updating the TMR1H:TMR1L register pair while the clock is low, or one-half of the period of the clock source. Assuming that Timer1 is being used as a Real-Time Clock, the clock source is a 32.768 kHz crystal oscillator; in this case, one-half period of the clock is 15.25 μs.

The Real-Time Clock application code in Example 12-1 shows a typical ISR for Timer1, as well as the optional code required if the update cannot be done reliably within the required interval.

(Example 12-1 appears on page 1 of this errata.)

3. Module: Universal Serial Bus (USB)

In **Subsection 17.2.2.8 "Internal Regulator,"** the following corrections should be noted (changes and added text appear in **bold** for the purposes of this errata):

- In the second paragraph, the first sentence is corrected to read, "The regulator is **dis**abled by default and can be **en**abled through the VREGEN Configuration bit."

  The sentence originally stated, "The regulator is enabled by default and can be disabled through the VREGEN Configuration bit."
- In the final note box of the section, Note 2 is corrected to read, "V_{DD} must be greater than **or equal to** V_{USB} at all times, even with the regulator disabled."

  The sentence originally stated, "V_{DD} must be greater than V_{USB} at all times, even with the regulator disabled."

4. Module: Master Synchronous Serial Port (MSSP) Module

In **Section 19.3.5 "Master Mode,"** the second paragraph of the second column is corrected to read, "This allows a maximum data rate (at 48 MHz) of **12.00** Mbps."

The sentence originally stated, "This allows a maximum data rate (at 48 MHz) of 2.00 Mbps."

5. Module: 10-Bit Analog-to-Digital (A/D) Converter Module

In **Register 21-1: "ADCON0: A/D Control Register 0,"** the display and the detailed bit description for bit 5 is corrected to **"VCFG1"**, rather than "VCFG0". All other bit 5 display and descriptions are correct in the device data sheet.

6. Module: Special Features of the CPU

In **Section 25.9.1 "Dedicated ICD/ICSP Port"**, the second sentence of the fourth paragraph is corrected to state, "When **V_{IHH}** is seen on the $\overline{MCLR}/V_{PP}$/RE3 pin, the state of the $\overline{ICRST}/ICV_{PP}$ pin is ignored". This refers to the high-voltage programming voltage level for ICSP™ (DC Specification D110).

The sentence originally stated, "When V_{IH} is seen on the $\overline{MCLR}/V_{PP}$/RE3 pin, the state of the $\overline{ICRST}/ICV_{PP}$ pin is ignored". That incorrectly referred to the maximum input voltage tolerated by the pin as an I/O (DC specification D040).

7. Module: Electrical Characteristics

In **Section 28.3 "DC Characteristics,"** pin-specific variations of parameters D031 (Input Low Voltage) and D041 (Input High Voltage) are corrected as characteristic for pins **RB0 and RB1**, not pins RC3 and RC4.

The following relevant portion of the table indicates the corrections. (For clarity, the corrected items appear in **bold** text – all other text appears in plain text for purposes of this errata.)

28.3 DC Characteristics: PIC18F2455/2550/4455/4550 (Industrial) PIC18LF2455/2550/4455/4550 (Industrial) (Partial Presentation)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D031	VIL	Input Low Voltage				
		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
		RB0 and RB1	VSS	0.3 VDD	V	
D041	VIH	Input High Voltage				
		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		RB0 and RB1	0.7 VDD	VDD	V	

8. Module: Electrical Characteristics

In **"Table 28-1: Memory Programming Requirements,"** the symbol for parameter D110 is corrected to **VIHH**, rather than VPP.

The following relevant portion of Table 28-1 indicates the correction. (For clarity, the corrected item appears in **bold** text – all other text appears in plain text for purposes of this errata.)

TABLE 28-1: MEMORY PROGRAMMING REQUIREMENTS (PARTIAL PRESENTATION)

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Internal Program Memory Programming Specifications(1)					
D110	**VIHH**	Voltage on $\overline{MCLR}$/VPP/RE3 pin	9.00	—	13.25	V	(Note 2)

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

2: Required only if Single-Supply Programming is disabled.

9. Module: Electrical Characteristics

In **"Table 28-5: USB Internal Voltage Regulator Specifications,"** parameter D323 (Regulator Voltage Output) is qualified with the condition of a minimum device **$V_{DD} \geq$ 4.0V** in the Comments column.

The following relevant portion of Table 28-1 indicates the correction. (For clarity, the corrected item appears in **bold** text – all other text has been changed to plain text for purposes of this errata.)

TABLE 28-5: USB INTERNAL VOLTAGE REGULATOR SPECIFICATIONS (PARTIAL PRESENTATION)

Operating Conditions: -40°C < T_A < +85°C (unless otherwise stated).							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D323	V_{USBANA}	Regulator Output Voltage	3.0	—	3.6	V	**$V_{DD} \geq$ 4.0V**

REVISION HISTORY

Rev A Document (7/2006)

Original version of this document. Includes issues 1-2 (Timer1), 3 (USB), 4 (MSSP), 5 (A/D Converter), 6 (Special Features of the CPU) and 7-9 (Electrical Characteristics).

NOTES:

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