

PLL Clock Driver for 2.5V SSTL_2 DDR SDRAM Memory

Features

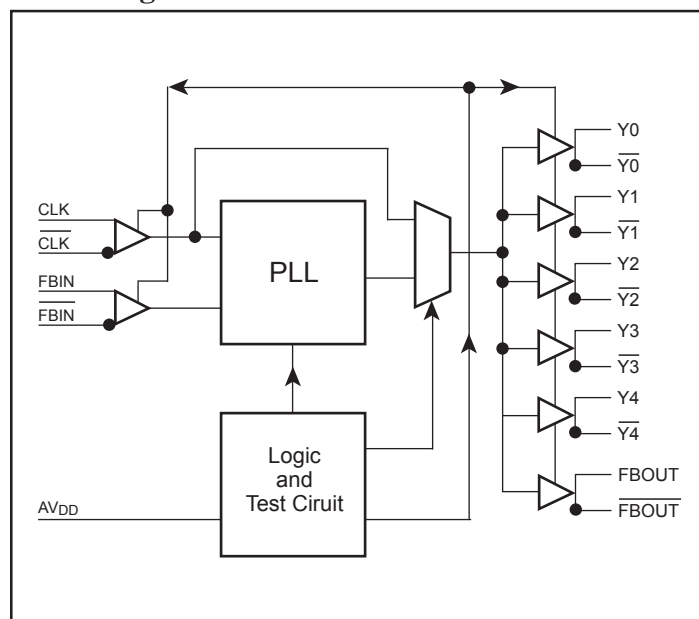
- PLL clock distribution optimized for SSTL_2 DDR SDRAM applications.
- Distributes one differential clock input pair to five differential clock output pairs.
- Inputs (CLK, $\overline{\text{CLK}}$) and (FBIN, $\overline{\text{FBIN}}$): SSTL_2
- Outputs (Y_x, $\overline{\text{Y}}_x$), (FBOUT, $\overline{\text{FBOUT}}$): SSTL_2
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the input clocks.
- Operates at AV_{DD} = 2.5V for core circuit and internal PLL, and V_{DDQ} = 2.5V for differential output drivers
- Packaging (Pb-free & Green available):
–28-pin TSSOP (L)

Description

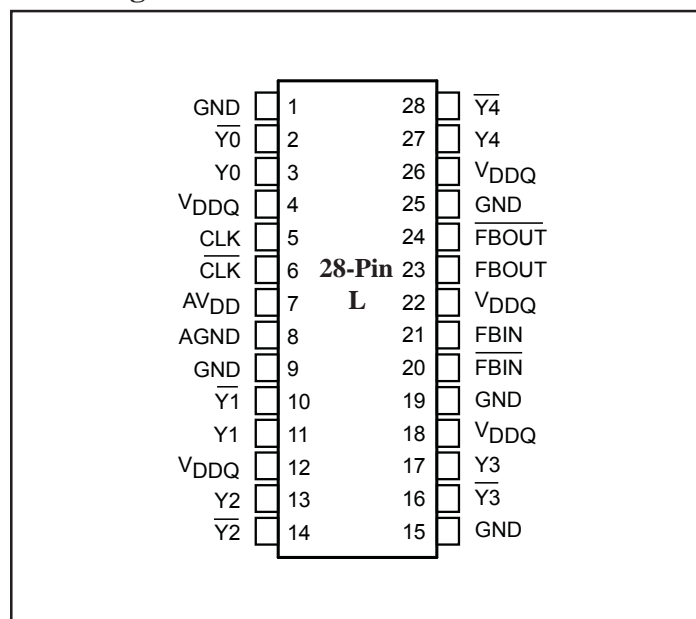
PI6CV855 PLL clock device is developed for SSTL_DDR SDRAM applications. This PLL Clock Buffer is designed for 2.5 V_{DDQ} and 2.5V AV_{DD} operation and differential data input and output levels. The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to five differential pairs of clock outputs (Y[0:4], $\overline{\text{Y}}[0:4]$) and one differential pair feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the Analog Power input (AV_{DD}). When the AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

The PI6CV855 is able to track Spread Spectrum Clocking to reduce EMI.

Block Diagram



Pin Configuration



Pinout Table

Pin Name	Pin No.	I/O Type	Description
CLK CLK	5 6	I	Reference Clock input
Y[0:4]	3,11,13,17,27	O	Clock outputs.
$\overline{Y[0:4]}$	2,10,14,16,28		Complement Clock outputs.
FBOUT FBOUT	23 24		Feedback output, and Complement Feedback Output
FBIN FBIN	21 20	I	Feedback input, and Complement Feedback input
V _{DDQ}	4,12,18,22,26	Power	Power Supply for I/O pins.
A _{VDD}	7		Analog/core power supply. A _{VDD} can be used to bypass the PLL for testing purposes. When A _{VDD} is strapped to ground, PLL is bypassed & CLK is buffered directly to the device outputs.
AGND	8	Ground	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	1,9,15,19,25		Ground for I/O pins.

Function Table

Inputs			Outputs				PLL State
A _{VDD}	CLK	\overline{CLK}	Y[0:4]	$\overline{Y[0:4]}$	FBOUT	\overline{FBOUT}	
GND	L	H	L	H	L	H	Bypassed/Off
GND	H	L	H	L	H	L	Bypassed/Off
2.5V(nom)	L	H	L	H	L	H	on
2.5V(nom)	H	L	H	L	H	L	on

Absolute Maximum Ratings (Over operating free-air temperature)

Symbol	Parameter	Min.	Max.	Units
V _{DDQ} , AV _{DD}	I/O supply voltage range and analog/core supply voltage range	- 0.5	3.6	V
V _I	Input voltage range	- 0.5	V _{DDQ} +0.5	
V _O	Output voltage range	- 0.5		
T _{stg}	Storage temperature	- 65	150	°C

Note: Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Timing Requirements (Over recommended operating free-air temperature)

Symbol	Description	AV _{DD} , V _{DDQ} = 2.5V ±0.2V		Units
		Min.	Max.	
f _{CK}	Operating clock frequency ^(1,2)	60	170	MHz
	Application clock frequency ⁽³⁾	95	170	
t _{DC}	Input clock duty cycle	40	60	%
t _{STAB}	PLL stabilization time after powerup		100	µs

Notes:

1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

DC Specifications

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
AV _{DD}	Analog/core supply voltage	2.3	2.5	2.7	V
V _{DDQ}	Output supply voltage	2.3	2.5	2.7	
V _{OH}	High-level output voltage	1.8		V _{DDQ}	
V _{OL}	Low-level output voltage	0		0.5	
V _{IX}	Input differential-pair crossing voltage	(V _{DDQ} /2) - 0.2		(V _{DDQ} /2) + 0.2	
V _{OX}	Output differential-pair crossing voltage at the SDRAM clock input	(V _{DDQ} /2) - 0.2		(V _{DDQ} /2) + 0.2	
V _{IN}	Input voltage level	-0.3		V _{DDQ} + 0.3	
V _{ID}	Input differential voltage between CLK and $\overline{\text{CLK}}$	0.36		V _{DDQ} + 0.6	
V _{OD}	Output differential voltage between Y[n] and $\overline{\text{Y[n]}}$ and FBOU _T and $\overline{\text{FBOU}}$	0.7		V _{DDQ} + 0.6	
T _A	Operating free air temperature	0		70	

Electrical Characteristics

Parameter		Test Conditions	AV _{DD} , V _{DDQ}	Min.	Typ.	Max.	Units
V _{IK}	All inputs	I _I = -18mA	2.3V			-1.2	V
I _I	CLK, FBIN	V _I = V _{DDQ} or GND	2.7V			±10	μA
I _{DDQ}	Dynamic supply current of V _{DDQ}	V _{DD} = 2.7V ⁽¹⁾				300	mA
I _{ADD}	Dynamic supply current of AV _{DD}	V _{DD} = 2.7V ⁽¹⁾				12	mA
C _I	CLK and $\overline{\text{CLK}}$	V _I = V _{DD} or GND	2.5V	2.0		3.0	pF
	FBIN and $\overline{\text{FBIN}}$						

Notes:

1. Driving 9 or 18 DDR SDRAM memory chips with 120-ohm termination resistor for each clock output pair at 134 MHz.

AC Specifications

Switching characteristics over recommended operating free-air temperature range, $f_{CLK} > 100$ MHz (unless otherwise noted).
 (See Figure 1 and 2)

Parameter	Description	Diagram	$V_{CC}, V_{DDQ} = 2.5V \pm 0.2V$			Units
			Min.	Nom.	Max	
$t(\theta)$	Static phase offset ⁽¹⁾	Figure 4	-50	0	50	ps
$t_{jit}(cc)$	Cycle-to-cycle jitter	Figure 3	-75		75	
$t_{jit}(per)$	Period jitter	Figure 6	-75		75	
$t_{jit}(hper)$	Half-period jitter	Figure 7	-100		100	
$tsl(i)$	Input clock slew rate ⁽²⁾	Figure 8	1.0		2.0	V/ns
$tsl(o)$	Output clock slew rate ⁽²⁾	Figure 8	1.0		2.0	
$tsk(o)$	Output clock skew	Figure 5			100	ps
The PLL on the PI6CV855 meets all the above parameters while supporting SSC synthesizers with the following parameters ⁽³⁾ .						
	SSC modulation frequency		30.0		50.0	kHz
	SSC clock input frequency deviation		0.00		-0.50	%
	PLL loop bandwidth			2		MHz
	Phase angle				-0.031	degrees

Notes:

1. Static Phase offset does not include jitter.
2. The slew rate is determined from the IBIS model with test load shown in Figure 1.
3. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

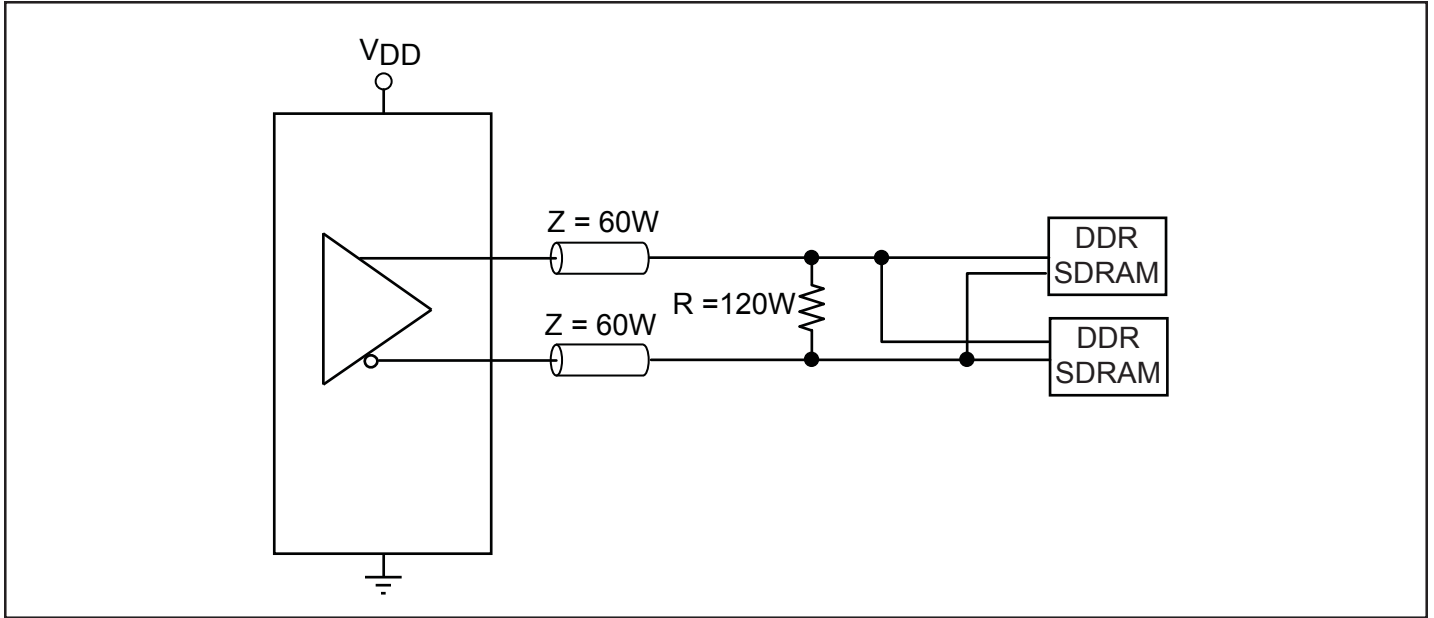


Figure 1. IBIS Model Output Load

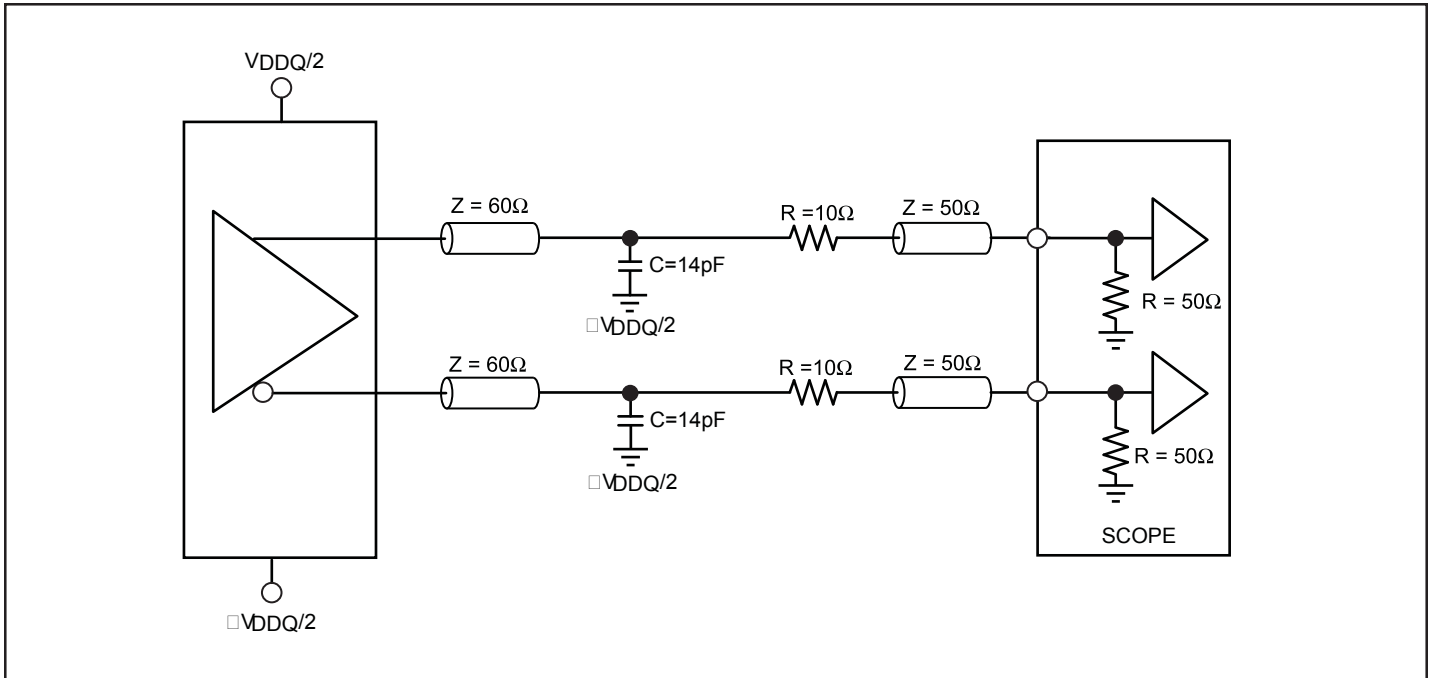


Figure 2. Output Load Test Circuit

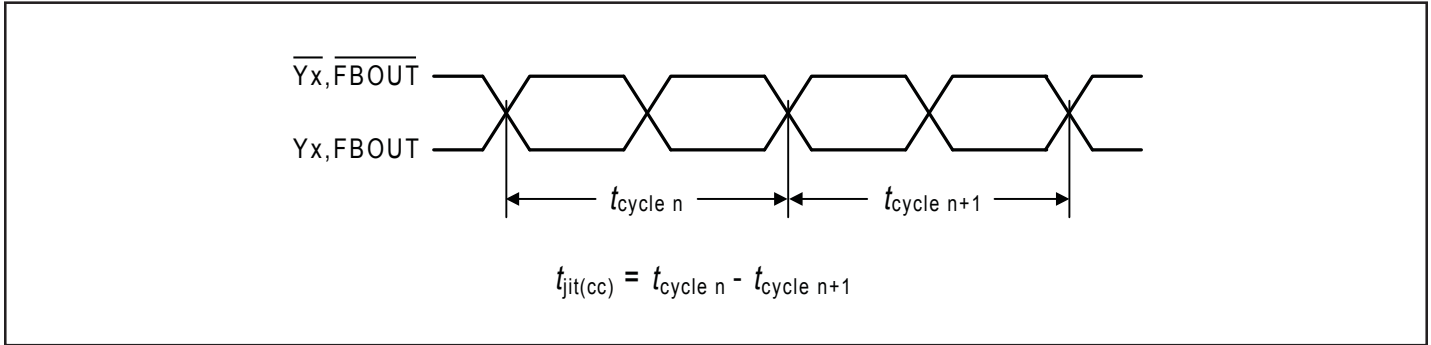


Figure 3. Cycle-to-Cycle Jitter

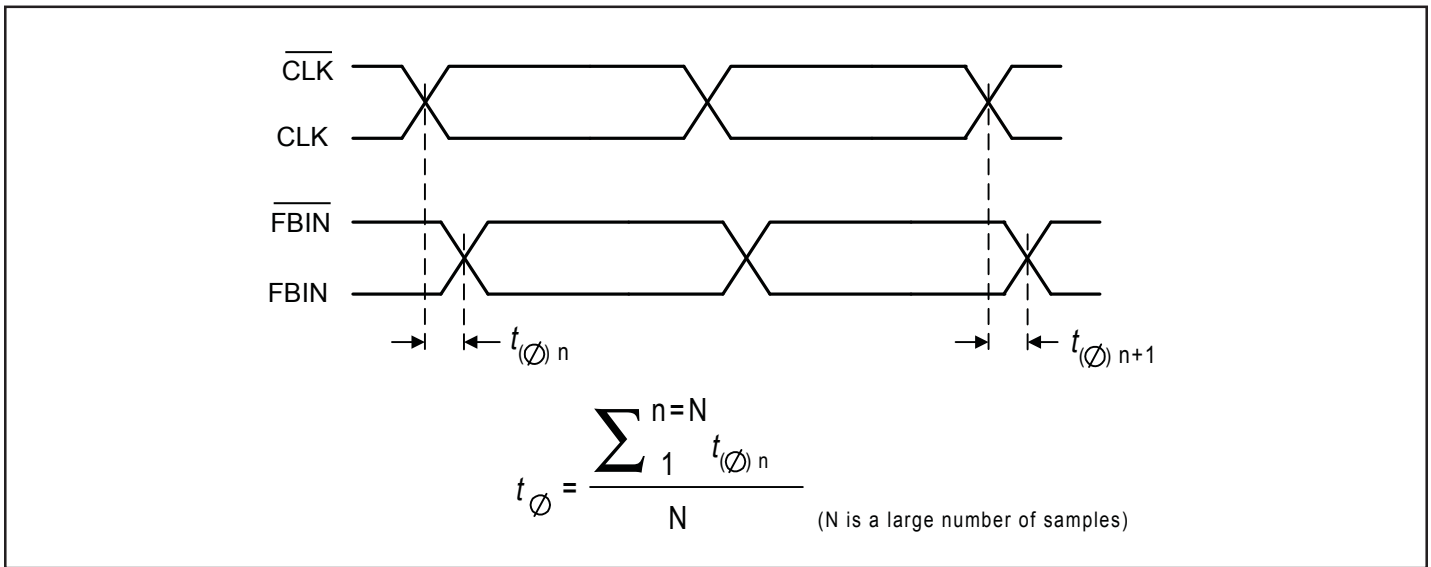


Figure 4. Static Phase Offset

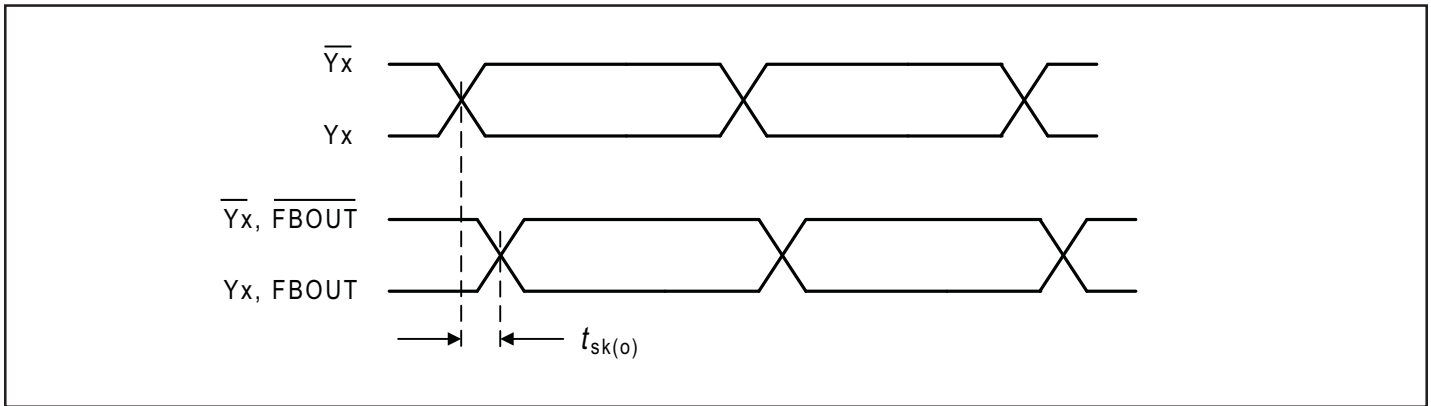


Figure 5. Output Skew

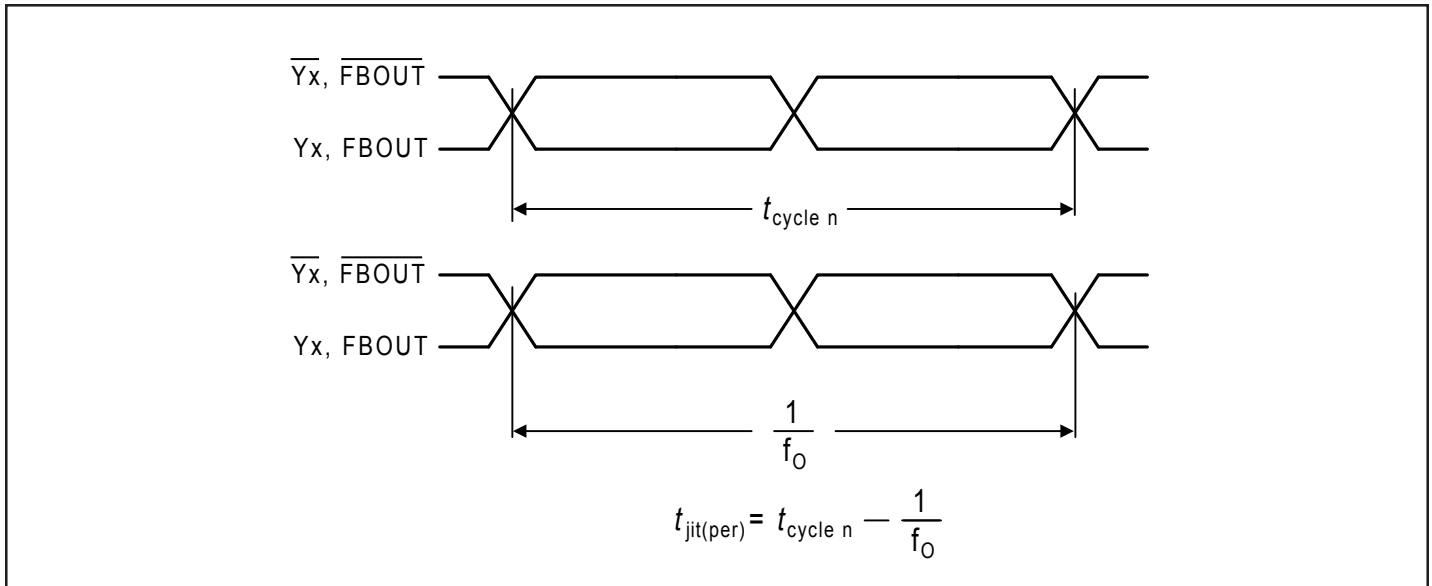


Figure 6. Period Jitter

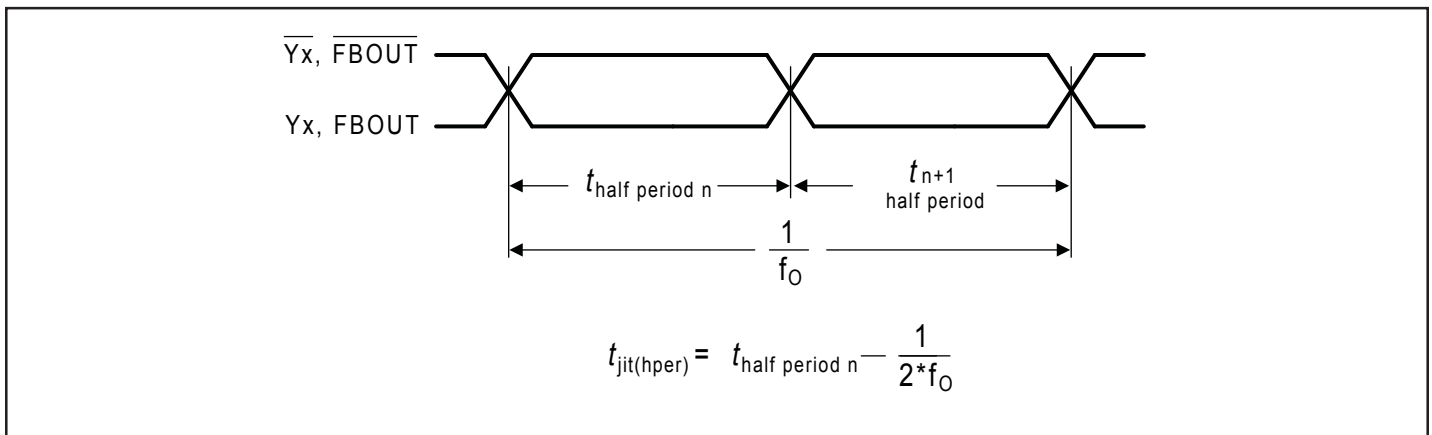


Figure 7. Half-Period Jitter

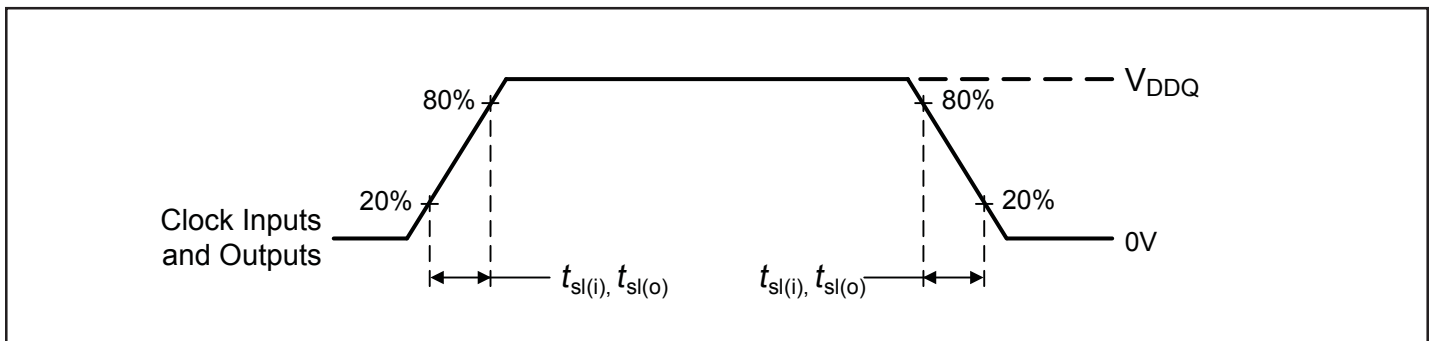


Figure 8. Input and Output Slew Rates

