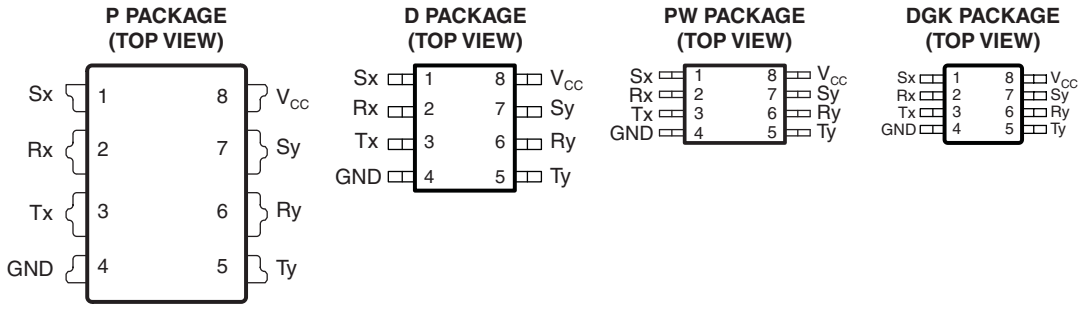
FEATURES

- **Operating Power-Supply Voltage Range of 2 V to 15 V**
- **Can Interface Between I^2C Buses Operating at Different Logic Levels (2 V to 15 V)**
- **Supports Bidirectional Data Transfer of I^2C Bus Signals**
- **Allows Bus Capacitance of 400 pF on the Main I^2C Bus (Sx/Sy Side) and 4000 pF on the Transmission Side (Tx/Ty)**
- **Outputs on the Transmission Side (Tx/Ty) Have High Sink Capability for Driving Low-Impedance or High-Capacitive Buses**
- **I^2C Bus Signals Can Be Split Into Pairs of Forward (Tx/Ty) and Reverse (Rx/Ry) Signals for Interface With Optoelectrical Isolators and Similar Devices That Need Unidirectional Input and Output Signal Paths**
- **400-kHz Fast I^2C Bus Operation Over at Least 20 Meters of Wire**
- **Low Standby Current Consumption**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **3500-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**



DESCRIPTION/ORDERING INFORMATION

The P82B96 is a bipolar device that supports bidirectional data transfer between the normal I^2C bus and a range of other bus configurations with different voltage and current levels. It can function as the interface without any limitations on the normal I^2C operation and clock speed.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – P	Tube of 50	P82B96P	P82B96P
	SOIC – D	Reel of 2000	P82B96DR	PG96
		Tube of 75	P82B96D	
	TSSOP – PW	Reel of 2000	P82B96PWR	PG96
		Tube of 150	P82B96PW	
	VSSOP – DGK	Reel of 2500	P82B96DGKR	7DS

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

One of the advantages of the P82B96 is that it can isolate bus capacitance such that the total loading (devices and trace lengths) of the new bus or remote I^2C nodes are not apparent to other I^2C buses (or nodes). This device also adds minimal loading to I^2C node where it is positioned. Any restrictions on the number of I^2C devices in a system, or the physical separation between them, are virtually eliminated.

The P82B96 easily can transmit SDA/SCL signals via balanced transmission lines (twisted pairs) or with galvanic isolation (optocoupling), because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be connected directly (without causing bus latching), to provide an alternative bidirectional signal line with I^2C properties.

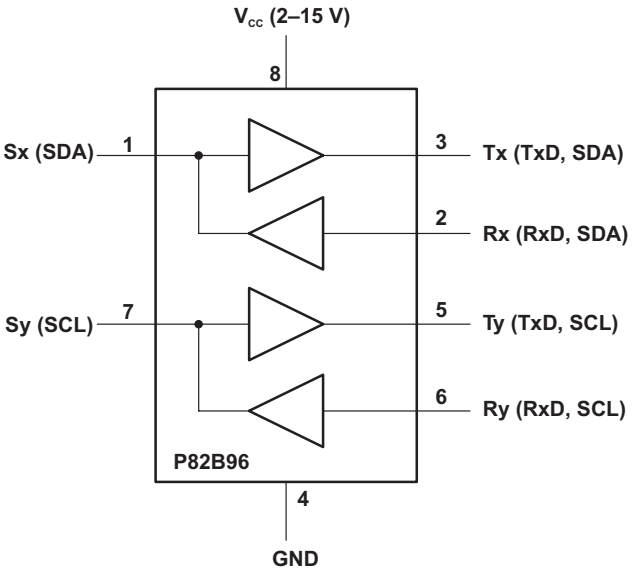
Two or more Sx or Sy I/Os must not be interconnected. The P82B96 design does not support this configuration. Bidirectional I^2C signals do not allow any direction control pin so, instead, slightly different logic low-voltage levels are used at Sx/Sy to avoid latching of this buffer. A regular I^2C low applied at the Rx/Ry of a P82B96 is propagated to Sx/Sy as a buffered low with a slightly higher voltage level. If this special buffered low is applied to the Sx/Sy of another P82B96, the second P82B96 does not recognize it as a regular I^2C bus low and does not propagate it to its Tx/Ty output. The Sx/Sy side of P82B96 may not be connected to similar buffers that rely on special logic thresholds for their operation, such as the PCA9515A.

The Sx/Sy side is intended only for, and compatible with, the normal I^2C logic voltage levels of I^2C master and slave devices or Tx/Rx signals of a second P82B96, if required. The Tx/Rx and Ty/Ry I/O pins use the standard I^2C logic voltage levels of all I^2C parts. If Rx and Tx are connected, Sx can function as either the SDA or SCL line. Similarly, if Ry and Ty are connected, Sy can function as either the SDA or SCL line. There are no restrictions on the interconnection of the Tx/Rx and Ty/Ry I/O pins to other P82B96s, for example in a star or multi-point configuration with the Tx/Rx and Ty/Ry I/O pins on the common bus, and the Sx/Sy side connected to the line-card slave devices.

TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	Sx	Serial data bus or SDA. Connect to V_{CC} of I^2C master through a pullup resistor.
2	Rx	Receive signal. Connect to V_{CC} of P82B96 through a pullup resistor.
3	Tx	Transmit signal. Connect to V_{CC} of P82B96 through a pullup resistor.
4	GND	Ground
5	Ty	Transmit signal. Connect to V_{CC} of P82B96 through a pullup resistor.
6	Ry	Receive signal. Connect to V_{CC} of P82B96 through a pullup resistor.
7	Sy	Serial clock bus or SCL. Connect to V_{CC} of I^2C master through a pullup resistor.
8	V_{CC}	Supply voltage

FUNCTIONAL BLOCK DIAGRAM



Functional Description

Sx and Sy

The I^2C pins, Sx and Sy, are designed to interface with a normal I^2C bus. The logic threshold-voltage levels on the I^2C bus are independent of the supply V_{CC}. The maximum I^2C bus supply voltage is 15 V, and the specified static sink current is 3 mA.

Sx and Sy have two identical buffers. Each buffer is made up of two logic signal paths. The first one, named Tx or Ty, is a forward path from the I^2C interface pin, which drives the buffered bus. The second one, named Rx or Ry, is a reverse signal path from the buffered bus input to drive the I^2C bus interface.

There are two purposes for these paths: to sense the voltage state of the I^2C pin (Sx or Sy) and transmit this state to Tx or Ty, respectively, and to detect the state of the Rx or Ry and pull the I^2C pin low when Rx or Ry is low.

Tx and Ty

Tx and Ty are open-collector outputs without ESD protection diodes to V_{CC}. Each pin may be connected via a pullup resistor to a supply voltage in excess of V_{CC}, as long as the 15-V rating is not exceeded. Tx and Ty have a larger current-sinking capability than a normal I^2C device and can sink a static current of greater than 30 mA. They also have dynamic pulldown capability of 100-mA, typically.

A logic low is transmitted to Tx or Ty only when the voltage at the I^2C pin (Sx or Sy) is below 0.6 V. A logic low at Rx or Ry causes the I^2C bus (Sx or Sy) to be pulled to a logic low level in accordance with I^2C requirements (maximum 1.5 V in 5-V applications), but not low enough to be looped back to the Tx or Ty output and cause the buffer to latch low.

The minimum low level that the P82B96 can achieve on the I^2C bus by a low at Rx or Ry typically is 0.8 V.

If V_{CC} fails, neither the I^2C pins nor the Tx or Ty outputs are held low. Their open-collector configuration allows them to be pulled up to the rated maximum of 15 V without V_{CC} present. The input configuration on Sx, Sy, Rx, and Ry also presents no loading of external signals when V_{CC} is not present.

The effective input capacitance of any signal pin, measured by its effect on bus rise times, is less than 4 pF for all bus voltages and supply voltages, including V_{CC} = 0 V.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	18	V
V_I	Voltage range on buffered input	Sx or Sy (SDA or SCL)	–0.3	18	V
		Rx or Ry	–0.3	18	
V_O	Voltage range on buffered output	Sx or Sy (SDA or SCL)	–0.3	18	V
		Tx or Ty	–0.3	18	
I_O	Continuous output current	Sx or Sy		250	mA
		Tx or Ty		250	
I_{CC}	Continuous current through V_{CC} or GND			250	mA
θ_{JA}	Package thermal impedance(2)	D package		97	°C/W
		P package		85	
		PW package		149	
		DGK package		172	
T_{stg}	Storage temperature range		–55	125	°C
T_A	Operating free-air temperature range		–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2	15	V
I_{OL}	Low-level output current	Sx, Sy	V_{Sx}, V_{Sy} = 1 V, V_{Rx}, V_{Ry} ≤ 0.42 V		3	mA
		Tx, Ty	V_{Sx}, V_{Sy} = 0.4 V, V_{Tx}, V_{Ty} = 0.4 V		30	
V_{IOmax}	Maximum input/output voltage level	Sx, Sy	V_{Tx}, V_{Ty} = 0.4 V		15	V
		Tx, Ty	V_{Sx}, V_{Sy} = 0.4 V		15	
V_{ILdiff}	Low-level input voltage difference	Sx, Sy			0.4	V
T_A	Operating free-air temperature			–40	85	°C

Electrical Characteristics

V_{CC} = 2.3 V to 2.7 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
$\Delta V/\Delta T_{IN}$	Temperature coefficient of input thresholds	Sx, Sy			–2				mV/°C
V_{OL}	Low-level output voltage	Sx, Sy	I_{Sx}, I_{Sy} = 3 mA	0.8	0.88	1			(2)V
			I_{Sx}, I_{Sy} = 0.2 mA	0.67	0.73	0.79		(2)	
$\Delta V/\Delta T_{OUT}$	Temperature coefficient of output low levels(3)	Sx, Sy	I_{Sx}, I_{Sy} = 0.2 mA		–1.8				mV/°C
I_{CC}	Quiescent supply current		Sx = Sy = V_{CC}		0.9	1.8		2	mA
ΔI_{CC}	Additional supply current per pin low	Tx, Ty			1.7	2.75		3	mA
I_{IOS}	Dynamic output sink capability on I^2C bus	Sx, Sy	V_{Sx}, V_{Sy} > 2 V, V_{Rx}, V_{Ry} = low	7	18		5.5		mA
	Leakage current on I^2C bus		V_{Sx}, V_{Sy} = 2.5 V, V_{Rx}, V_{Ry} = high		0.1	1		1	µA
I_{IOT}	Dynamic output sink capability on buffered bus	Tx, Ty	V_{Tx}, V_{Ty} > 1 V, V_{Sx}, V_{Sy} = low on I^2C bus = 0.4 V	60	100		60		mA
	Leakage current on buffered bus		V_{Tx}, V_{Ty} = V_{CC} = 2.5 V, V_{Sx}, V_{Sy} = high		0.1	1		1	µA
I_I	Input current from I^2C bus	Sx, Sy	Bus low, V_{Rx}, V_{Ry} = high		–1			1	µA
	Input current from buffered bus	Rx, Ry	Bus low, V_{Rx}, V_{Ry} = 0.4 V		–1			1	
	Leakage current on buffered bus input		V_{Rx}, V_{Ry} = V_{CC}		1			1.5	
V_{IT}	Input threshold	Sx, Sy	Input logic level high threshold(4) on normal I^2C bus		0.65	0.7		(2)	V
			Input logic level low threshold(4) on normal I^2C bus	0.6	0.65			(2)	
		Rx, Ry	Input logic level high	0.58 V_{CC}			0.58 V_{CC}		
			Input threshold		0.5 V_{CC}				
			Input logic level low			0.42 V_{CC}		0.42 V_{CC}	
V_{IOdiff}	Input/output logic level difference(5)	Sx, Sy	(V_{Sx} output low at 3 mA) – (V_{Sx} input high max) for I^2C applications	100	150		100		mV
V_{IOrel}	V_{CC} voltage at which all buses are released	Sx, Sy Tx, Ty	Sx, Sy are low, V_{CC} ramping, voltage on Tx, Ty lowered until released	1			1		V
$\Delta V/\Delta T_{REL}$	Temperature coefficient of release voltage				–4				mV/°C
C_{in}	Input capacitance	Rx, Ry			2.5	4		4	pF

(1) Typical value is at V_{CC} = 2.5 V, T_A = 25°C
(2) See the Typical Characteristics section of this data sheet.
(3) The output logic low depends on the sink current.
(4) The input logic threshold is independent of the supply voltage.
(5) The minimum value requirement for pullup current, 200 µA, ensures that the minimum value for V_{SX} output low always exceeds the minimum V_{Sx} input high level to eliminate any possibility of latching. The specified difference is specified by design within any device. While the tolerances on absolute levels allow a small probability that the low from one Sx output is recognized by an Sx input of another P82B96, this has no consequences for normal applications. In any design, the Sx pins of different devices should never be linked, because the resulting system would be very susceptible to induced noise and would not support all I^2C operating modes.

Electrical Characteristics

V_{CC} = 3 V to 3.6 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
$\Delta V/\Delta T_{IN}$	Temperature coefficient of input thresholds	Sx, Sy			–2				mV/°C
V_{OL}	Low-level output voltage	Sx, Sy	I_{Sx}, I_{Sy} = 3 mA	0.8	0.88	1			(2)V
			I_{Sx}, I_{Sy} = 0.2 mA	0.67	0.73	0.79		(2)	
$\Delta V/\Delta T_{OUT}$	Temperature coefficient of output low levels(3)	Sx, Sy	I_{Sx}, I_{Sy} = 0.2 mA		–1.8				mV/°C
I_{CC}	Quiescent supply current		Sx = Sy = V_{CC}		0.9	1.8		2	mA
ΔI_{CC}	Additional supply current per pin low	Tx, Ty			1.7	2.75		3	mA
I_{IOS}	Dynamic output sink capability on I^2C bus	Sx, Sy	V_{Sx}, V_{Sy} > 2 V, V_{Rx}, V_{Ry} = low	7	18		5.7		mA
	Leakage current on I^2C bus		V_{Sx}, V_{Sy} = 5 V, V_{Rx}, V_{Ry} = high		0.1	1		1	µA
I_{IOT}	Dynamic output sink capability on buffered bus	Tx, Ty	V_{Tx}, V_{Ty} > 1 V, V_{Sx}, V_{Sy} = low on I^2C bus = 0.4 V	60	100		60		mA
	Leakage current on buffered bus		V_{Tx}, V_{Ty} = V_{CC} = 3.3 V, V_{Sx}, V_{Sy} = high		0.1	1		1	µA
I_I	Input current from I^2C bus	Sx, Sy	Bus low, V_{Rx}, V_{Ry} = high		–1			1	µA
	Input current from buffered bus	Rx, Ry	Bus low, V_{Rx}, V_{Ry} = 0.4 V		–1			1	
	Leakage current on buffered bus input		V_{Rx}, V_{Ry} = V_{CC}		1			1.5	
V_{IT}	Input threshold	Sx, Sy	Input logic-level high threshold(4) on normal I^2C bus		0.65	0.7		(2)	V
			Input logic-level low threshold(4) on normal I^2C bus	0.6	0.65			(2)	
		Rx, Ry	Input logic level high	0.58 V_{CC}			0.58 V_{CC}		
			Input threshold		0.5 V_{CC}				
			Input logic level low			0.42 V_{CC}		0.42 V_{CC}	
V_{IOdiff}	Input/output logic level difference(5)	Sx, Sy	(V_{Sx} output low at 3 mA) – (V_{Sx} input high max) for I^2C applications	100	150		100		mV
V_{IOrel}	V_{CC} voltage at which all buses are released	Sx, Sy Tx, Ty	Sx, Sy are low, V_{CC} ramping, voltage on Tx, Ty lowered until released	1			1		V

(1) Typical value is at V_{CC} = 3.3 V, T_A = 25°C
(2) See the Typical Characteristics section of this data sheet.
(3) The output logic low depends on the sink current.
(4) The input logic threshold is independent of the supply voltage.
(5) The minimum value requirement for pullup current, 200 µA, ensures that the minimum value for V_{SX} output low always exceeds the minimum V_{Sx} input high level to eliminate any possibility of latching. The specified difference is specified by design within any device. While the tolerances on absolute levels allow a small probability that the low from one Sx output is recognized by an Sx input of another P82B96, this has no consequences for normal applications. In any design, the Sx pins of different devices never should be linked, because the resulting system would be very susceptible to induced noise and would not support all I^2C operating modes.

Electrical Characteristics (continued)

V_{CC} = 3 V to 3.6 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
$\Delta V/\Delta T_{REL}$	Temperature coefficient of release voltage				–4				mV/°C
C_{in}	Input capacitance	Rx, Ry			2.5	4		4	pF

Electrical Characteristics

V_{CC} = 4.5 V to 5.5 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
$\Delta V/\Delta T_{IN}$	Temperature coefficient of input thresholds	Sx, Sy			–2				mV/°C
V_{OL}	Low-level output voltage	Sx, Sy	I_{Sx}, I_{Sy} = 3 mA	0.8	0.88	1			(2)V
			I_{Sx}, I_{Sy} = 0.2 mA	0.67	0.73	0.79		(2)	
$\Delta V/\Delta T_{OUT}$	Temperature coefficient of output low levels(3)	Sx, Sy	I_{Sx}, I_{Sy} = 0.2 mA		–1.8				mV/°C
I_{CC}	Quiescent supply current		Sx = Sy = V_{CC}		0.9	1.8		2	mA
ΔI_{CC}	Additional supply current per pin low	Tx, Ty			1.7	2.75		3	mA
I_{IOS}	Dynamic output sink capability on I^2C bus	Sx, Sy	V_{Sx}, V_{Sy} > 2 V, V_{Rx}, V_{Ry} = low	7	18		6		mA
	Leakage current on I^2C bus		V_{Sx}, V_{Sy} = 5 V, V_{Rx}, V_{Ry} = high		0.1	1		1	µA
I_{IOT}	Dynamic output sink capability on buffered bus	Tx, Ty	V_{Tx}, V_{Ty} > 1 V, V_{Sx}, V_{Sy} = low on I^2C bus = 0.4 V	60	100		60		mA
	Leakage current on buffered bus		V_{Tx}, V_{Ty} = V_{CC} = 5 V, V_{Sx}, V_{Sy} = high		0.1	1		1	µA
I_I	Input current from I^2C bus	Sx, Sy	Bus low, V_{Rx}, V_{Ry} = high		–1			1	µA
	Input current from buffered bus	Rx, Ry	Bus low, V_{Rx}, V_{Ry} = 0.4 V		–1			1	
	Leakage current on buffered bus input		V_{Rx}, V_{Ry} = V_{CC}		1			1.5	
V_{IT}	Input threshold	Sx, Sy	Input logic-level high threshold(4) on normal I^2C bus		0.65	0.7		(2)	V
			Input logic-level low threshold(4) on normal I^2C bus	0.6	0.65			(2)	
		Rx, Ry	Input logic level high	0.58 V_{CC}			0.58 V_{CC}		
			Input threshold		0.5 V_{CC}				
			Input logic level low			0.42 V_{CC}		0.42 V_{CC}	
V_{IOdiff}	Input/output logic level difference(5)	Sx, Sy	(V_{Sx} output low at 3 mA) – (V_{Sx} input high max) for I^2C applications	100	150		100		mV
V_{IOrel}	V_{CC} voltage at which all buses are released	Sx, Sy Tx, Ty	Sx, Sy are low, V_{CC} ramping, voltage on Tx, Ty lowered until released	1			1		V

(1) Typical value is at V_{CC} = 5 V, T_A = 25°C
(2) See the Typical Characteristics section of this data sheet.
(3) The output logic low depends on the sink current.
(4) The input logic threshold is independent of the supply voltage.
(5) The minimum value requirement for pullup current, 200 µA, ensures that the minimum value for V_{SX} output low always exceeds the minimum V_{Sx} input high level to eliminate any possibility of latching. The specified difference is specified by design within any device. While the tolerances on absolute levels allow a small probability that the low from one Sx output is recognized by an Sx input of another P82B96, this has no consequences for normal applications. In any design, the Sx pins of different devices never should be linked, because the resulting system would be very susceptible to induced noise and would not support all I^2C operating modes.

Electrical Characteristics (continued)

V_{CC} = 4.5 V to 5.5 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
$\Delta V/\Delta T_{REL}$	Temperature coefficient of release voltage				–4				mV/°C
C_{in}	Input capacitance	Rx, Ry			2.5	4		4	pF

Electrical Characteristics

V_{CC} = 15 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
$\Delta V/\Delta T_{IN}$	Temperature coefficient of input thresholds	Sx, Sy			–2				mV/°C
V_{OL}	Low-level output voltage	Sx, Sy	I_{Sx}, I_{Sy} = 3 mA	0.8	0.88	1			(2)V
			I_{Sx}, I_{Sy} = 0.2 mA	0.67	0.73	0.79		(2)	
$\Delta V/\Delta T_{OUT}$	Temperature coefficient of output low levels(3)	Sx, Sy	I_{Sx}, I_{Sy} = 0.2 mA		–1.8				mV/°C
I_{CC}	Quiescent supply current		Sx = Sy = V_{CC}		0.9	1.8		2	mA
ΔI_{CC}	Additional supply current per pin low	Tx, Ty			1.7	2.75		3	mA
I_{IOS}	Dynamic output sink capability on I^2C bus	Sx, Sy	V_{Sx}, V_{Sy} > 2 V, V_{Rx}, V_{Ry} = low	7	18		6.5		mA
	Leakage current on I^2C bus		V_{Sx}, V_{Sy} = 15 V, V_{Rx}, V_{Ry} = high		0.1	1		1	µA
I_{IOT}	Dynamic output sink capability on buffered bus	Tx, Ty	V_{Tx}, V_{Ty} > 1 V, V_{Sx}, V_{Sy} = low on I^2C bus = 0.4 V	60	100		60		mA
	Leakage current on buffered bus		V_{Tx}, V_{Ty} = V_{CC} = 15 V, V_{Sx}, V_{Sy} = high		0.1	1		1	µA
I_I	Input current from I^2C bus	Sx, Sy	Bus low, V_{Rx}, V_{Ry} = high		–1			1	µA
	Input current from buffered bus	Rx, Ry	Bus low, V_{Rx}, V_{Ry} = 0.4 V		–1			1	
	Leakage current on buffered bus input		V_{Rx}, V_{Ry} = V_{CC}		1			1.5	
V_{IT}	Input threshold	Sx, Sy	Input logic-level high threshold(4) on normal I^2C bus		0.65	0.7		(2)	V
			Input logic-level high threshold(4) on normal I^2C bus	0.6	0.65			(2)	
		Rx, Ry	Input logic level high	0.58 V_{CC}			0.58 V_{CC}		
			Input threshold		0.5 V_{CC}				
			Input logic level low			0.42 V_{CC}		0.42 V_{CC}	
V_{IOdiff}	Input/output logic level difference(5)	Sx, Sy	(V_{Sx} output low at 3 mA) – (V_{Sx} input high max) for I^2C applications	100	150		100		mV

(1) Typical value is at V_{CC} = 15 V, T_A = 25°C
(2) See the Typical Characteristics section of this data sheet.
(3) The output logic low depends on the sink current.
(4) The input logic threshold is independent of the supply voltage.
(5) The minimum value requirement for pullup current, 200 µA, ensures that the minimum value for V_{SX} output low always exceeds the minimum V_{Sx} input high level to eliminate any possibility of latching. The specified difference is specified by design within any device. While the tolerances on absolute levels allow a small probability that the low from one Sx output is recognized by an Sx input of another P82B96, this has no consequences for normal applications. In any design, the Sx pins of different devices never should be linked, because the resulting system would be very susceptible to induced noise and would not support all I^2C operating modes.

Electrical Characteristics (continued)

V_{CC} = 15 V, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	
V_{IOrel}	V_{CC} voltage at which all buses are released	Sx, Sy Tx, Ty	Sx, Sy are low, V_{CC} ramping, voltage on Tx, Ty lowered until released	1			1		V
$\Delta V/\Delta T_{REL}$	Temperature coefficient of release voltage				–4				mV/°C
C_{in}	Input capacitance	Rx, Ry			2.5	4		4	pF

Switching Characteristics

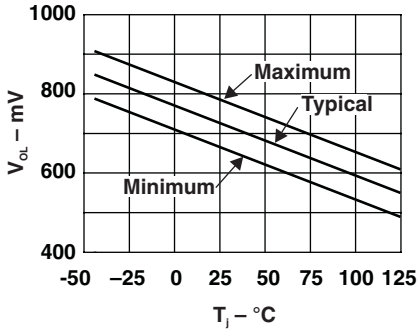
V_{CC} = 5 V, T_A = 25°C, no capacitive loads, voltages are specified with respect to GND (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TYP	UNIT
t_{pzl}	Buffer delay time on falling input(1)	V_{Sx} (or V_{Sy}) = input switching threshold	V_{Tx} (or V_{Ty}) output falling 50% of V_{LOAD}	R_{Tx} pullup = 160 Ω, C_{Tx} = 7 pF + board trace capacitance	70	ns
t_{plz}	Buffer delay time on rising input(2)	V_{Sx} (or V_{Sy}) = input switching threshold	V_{Tx} (or V_{Ty}) output reaching 50% of V_{LOAD}	R_{Tx} pullup = 160 Ω, C_{Tx} = 7 pF + board trace capacitance	90	ns
t_{pzl}	Buffer delay time on falling input(3)	V_{Rx} (or V_{Ry}) = input switching threshold	V_{Sx} (or V_{Sy}) output falling 50% of V_{LOAD}	R_{Sx} pullup = 1500 Ω, C_{Tx} = 7 pF + board trace capacitance	250	ns
t_{plz}	Buffer delay time on rising input(4)	V_{Rx} (or V_{Ry}) = input switching threshold	V_{Sx} (or V_{Sy}) output reaching 50% of V_{LOAD}	R_{Sx} pullup = 1500 Ω, C_{Tx} = 7 pF + board trace capacitance	270	ns

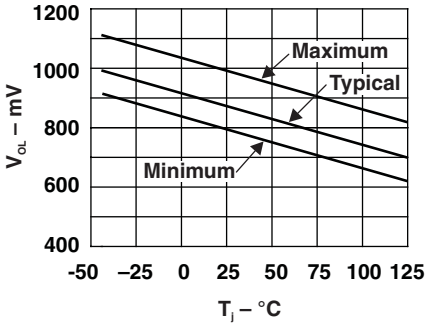
(1) The fall time of V_{Tx} from 5 V to 2.5 V in the test is approximately 15 ns.
(2) The fall time of V_{Sx} from 5 V to 2.5 V in the test is approximately 50 ns.
(3) The rise time of V_{Tx} from 0 V to 2.5 V in the test is approximately 20 ns.
(4) The rise time of V_{Sx} from 0.9 V to 2.5 V in the test is approximately 70 ns.

TYPICAL CHARACTERISTICS

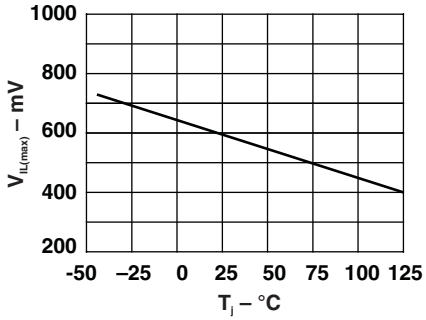
V_{OL} AT Sx
vs
JUNCTION TEMPERATURE
I_{OL} = 0.2 mA



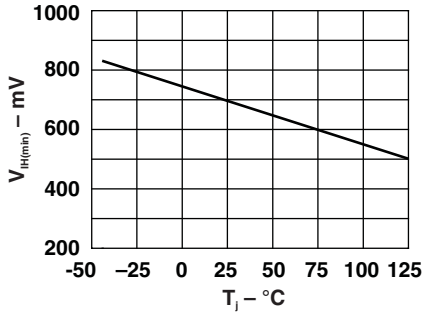
V_{OL} AT Sx
vs
JUNCTION TEMPERATURE
I_{OL} = 3 mA



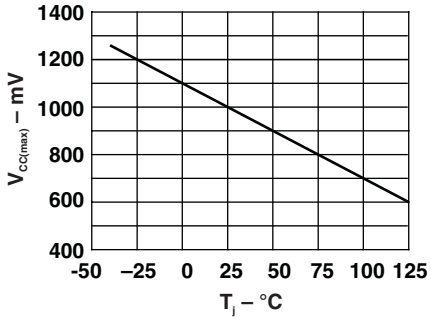
$V_{IL(max)}$ AT Sx
vs
JUNCTION TEMPERATURE



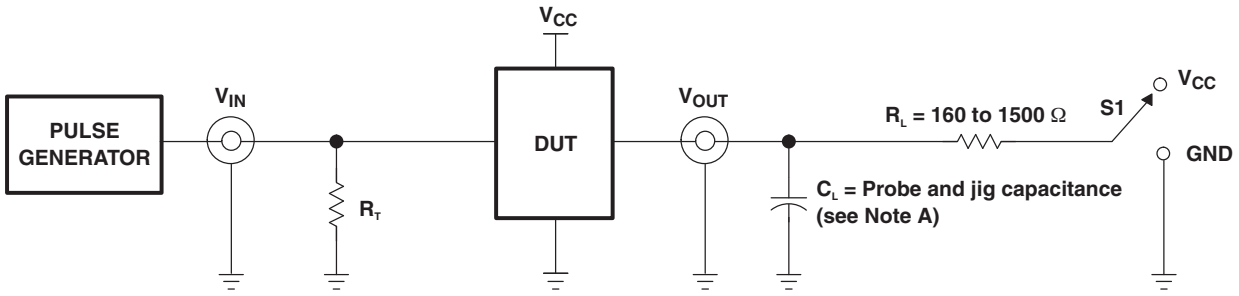
$V_{IH(min)}$ AT Sx
vs
JUNCTION TEMPERATURE



$V_{CC(max)}$
vs
JUNCTION TEMPERATURE

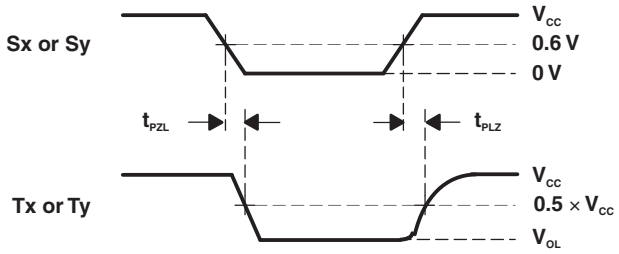


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

Typical Applications

Figure 2 through Figure 4 show typical applications for the P82B96.

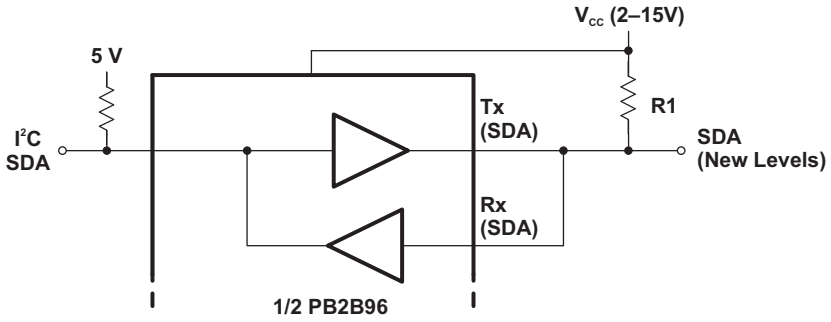


Figure 2. Interfacing I²C Bus With Different Logic Levels

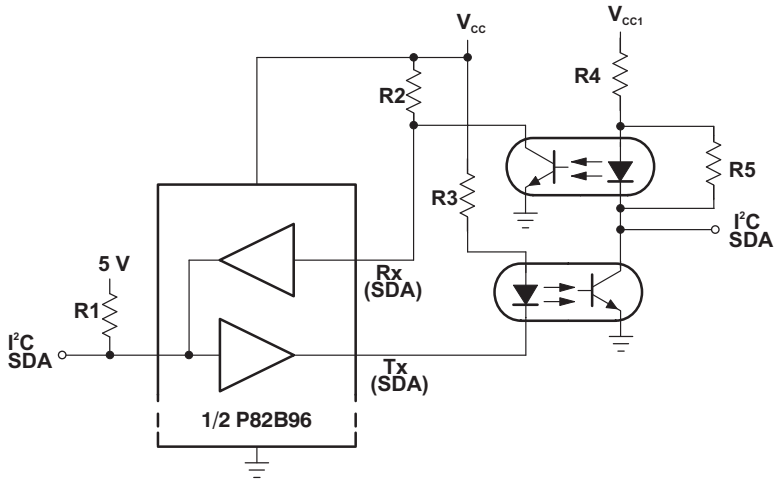


Figure 3. Galvanic Isolation of I²C Nodes

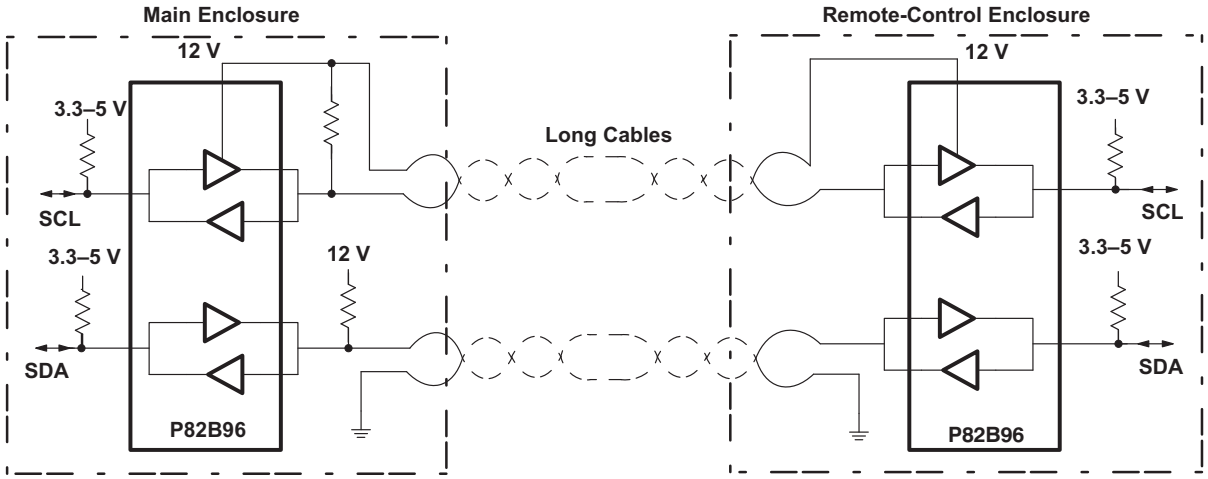


Figure 4. Long-Distance I²C Communications

APPLICATION INFORMATION (continued)

Figure 5 shows how a master I²C bus can be protected against short circuits or failures in applications that involve plug/socket connections and long cables that may become damaged. A simple circuit is added to monitor the SDA bus and, if its low time exceeds the design value, disconnect the master bus. P82B96 frees all of its I/Os if its supply is removed, so one option is to connect its V_{CC} to the output of a logic gate from, for example, the LVC family. The SDA and SCL lines could be timed, and V_{CC} disabled via the gate, if a line exceeds a design value of the low period. If the supply voltage of logic gates restricts the choice of V_{CC} supply, the low-cost discrete circuit in Figure 5 can be used. If the SDA line is held low, the 100-nF capacitor charges, and Ry is pulled toward V_{CC}. When it exceeds $V_{CC}/2$, Ry sets Sy high, which effectively releases it.

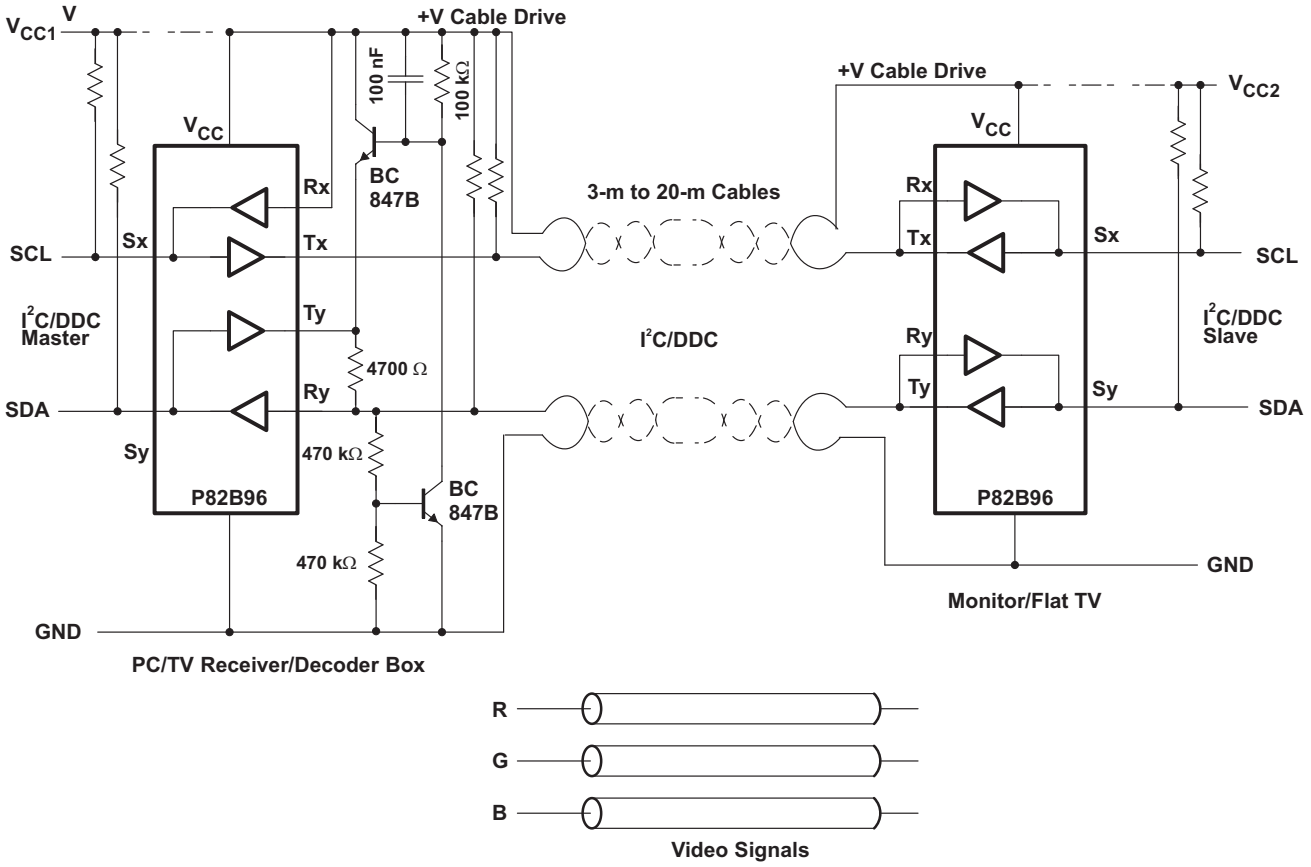


Figure 5. Extending DCC Bus

In this example, the SCL line is made unidirectional by tying Rx to V_{CC}. The state of the buffered SCL line cannot affect the master clock line, which is allowed when clock stretching is not required. It is simple to add an additional transistor or diode to control the Rx input in the same way as Ry, when necessary. The +V cable drive can be any voltage up to 15 V, and the bus may be run at a lower impedance by selecting pullup resistors for a static sink current up to 30 mA. V_{CC1} and V_{CC2} may be chosen to suit the connected devices. Because DDC uses relatively low speeds (<100 kHz), the cable length is not restricted to 20 m by the I²C signaling, but it may be limited by the video signaling.

Figure 6 and Table 1 show that P82B96 can achieve high clock rates over long cables. While calculating with lumped wiring capacitance yields reasonable approximations to actual timing; even 25 m of cable is better treated using transmission line theory. Flat ribbon cables connected as shown, with the bus signals on the outer edge, have a characteristic impedance in the range 100–200 Ω. For simplicity, they cannot be terminated in their characteristic impedance, but a practical compromise is to use the minimum pullup allowed for P82B96 and place half this termination at each end of the cable. When each pullup is below 330 Ω, the rising-edge waveforms have their first voltage step level above the logic threshold at Rx, and cable timing calculations can be based on the fast rise/fall times of resistive loading, plus simple one-way propagation delays. When the pullup is larger, but below 750 Ω, the threshold at Rx is crossed after one signal reflection. So, at the sending

APPLICATION INFORMATION (continued)

end, it is crossed after two times the one-way propagation delay and, at the receiving end, after three times that propagation delay. For flat cables with partial plastic dielectric insulation (by using outer cores) the one-way propagation delays are about 5 ns/m. The 10% to 90% rise and fall times on the cable are between 20 ns and 50 ns, so their delay contributions are small. There is ringing on falling edges that can be damped, if required, using Schottky diodes, as shown.

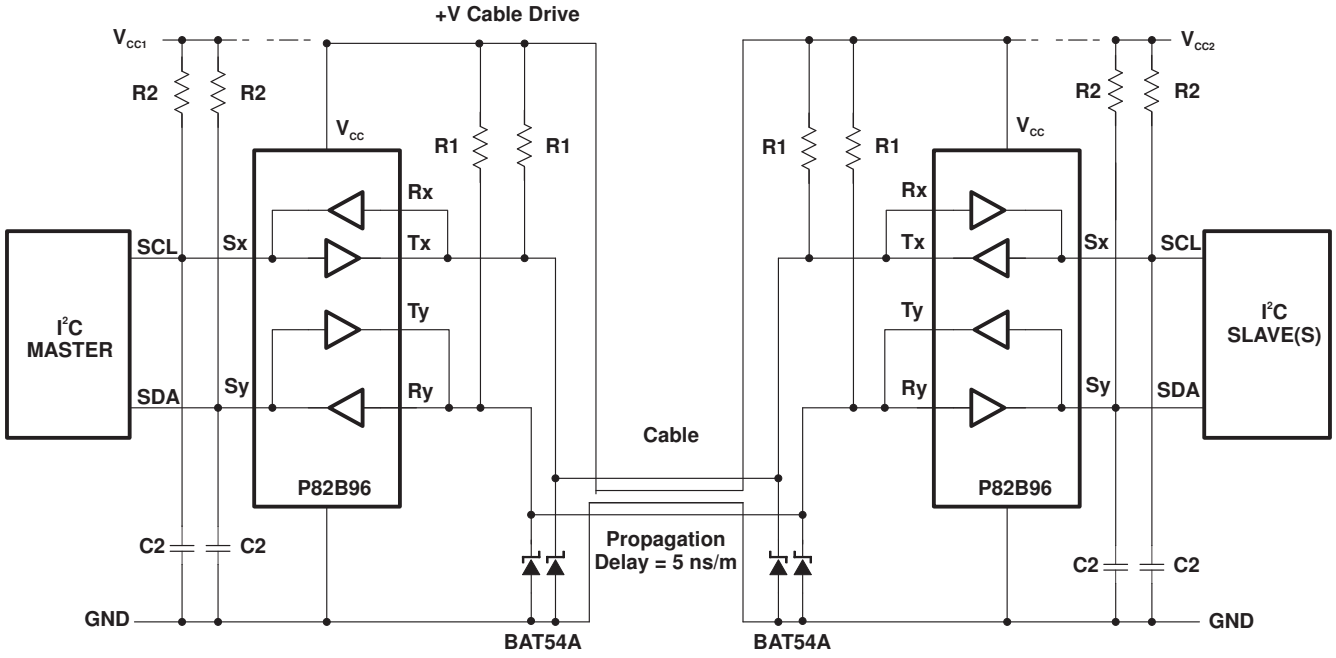


Figure 6. Driving Ribbon or Flat Telephone Cables

Table 1. Bus Capabilities

V_{CC1} (V)	+V CABLE (V)	V_{CC2} (V)	R1 (Ω)	R2 (kΩ)	C2 (pF)	CABLE LENGTH (m)	CABLE CAPACITANCE	CABLE DELAY (ns)	MASTER SCL PULSE DURATION (ns)		BUS CLOCK SPEED (kHz)	MAXIMUM SLAVE RESPONSE DELAY
									HIGH	LOW		
5	12	5	750	2.2	400	250	(1)	1250	600	4000	120	(2)
5	12	5	750	2.2	220	100	(1)	500	600	2600	185	(2)
3.3	5	3.3	330	1	220	25	1 nF	125	600	1500	390	(2)
3.3	5	3.3	330	1	100	3	120 pF	15	600	1000	500	600 ns

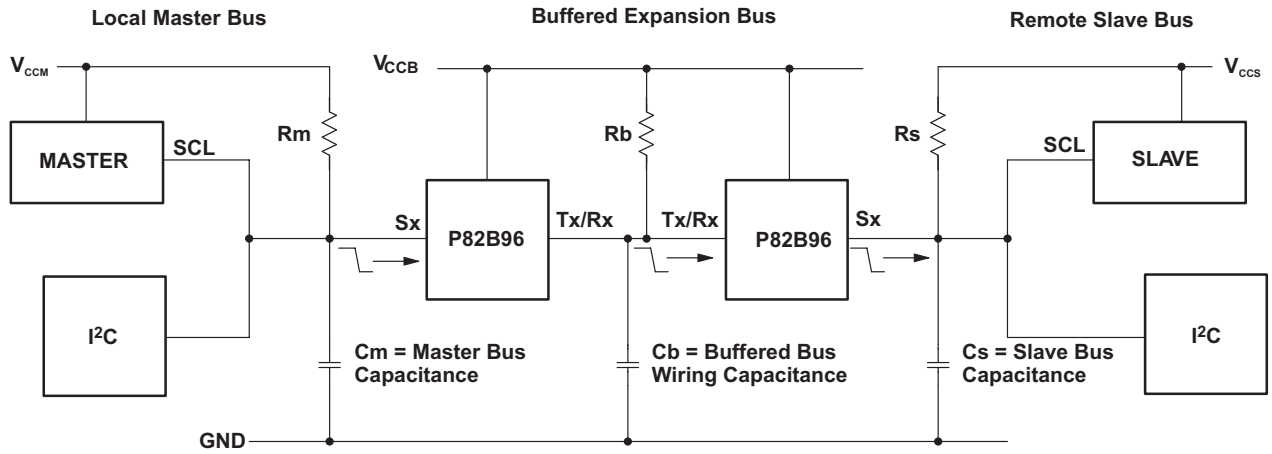
(1) Not applicable; calculations are delay based.
(2) Normal 400-kHz bus specification

When the master SCL high and low periods can be programmed separately, the timings can allow for bus delays. The low period should be programmed to achieve the minimum 1300 ns plus the net delay in the slave response data signal caused by bus and buffer delays. The longest data delay is the sum of the delay of the falling edge of SCL from master to slave and the delay of the rising edge of SDA from slave data to master. Because the buffer stretches the programmed SCL low period, the actual SCL frequency is lower than calculated from the programmed clock periods. In the example for the 25-m cable in Table 1, the clock is stretched 400 ns, the falling edge of SCL is delayed 490 ns, and the SDA rising edge is delayed 570 ns. The required additional low period is (490 + 570) = 1060 ns and the I^2C bus specifications already include an allowance for a worst-case bus rise time (0% to 70%) of 425 ns. The bus rise time can be 300 ns (30% to 70%), which means it can be 425 ns (0% to 70%). The 25-m cable delay times include all rise and fall times. Therefore, the device only needs to be programmed with an additional (1060 – 400 – 425) = 235 ns, making a total programmed low period 1535 ns. The programmed low is stretched by 400 ns to yield an actual bus low time of 1935 ns, which, allowing the minimum high period of 600 ns, yields a cycle period of 2535 ns or 394 kHz.

Note that, in both the 100-m and 250-m examples, the capacitive loading on the I^2C buses at each end is within the maximum allowed Standard mode loading of 400 pF, but exceeds the Fast mode limit. This is an example of a hybrid mode, because it relies on the response delays of Fast mode parts, but uses (allowable) Standard mode bus loadings with rise times that contribute significantly to the system delays. The cables cause large propagation delays. Therefore, these systems must operate well below the 400-kHz limit, but illustrate how they still can exceed the 100-kHz limit, provided all parts are capable of Fast mode operation. The fastest example illustrates how the 400-kHz limit can be exceeded, provided master and slave parts have delay specifications smaller than the maximum allowed. Many TI slaves have delays shorter than 600 ns, but none have that specified.

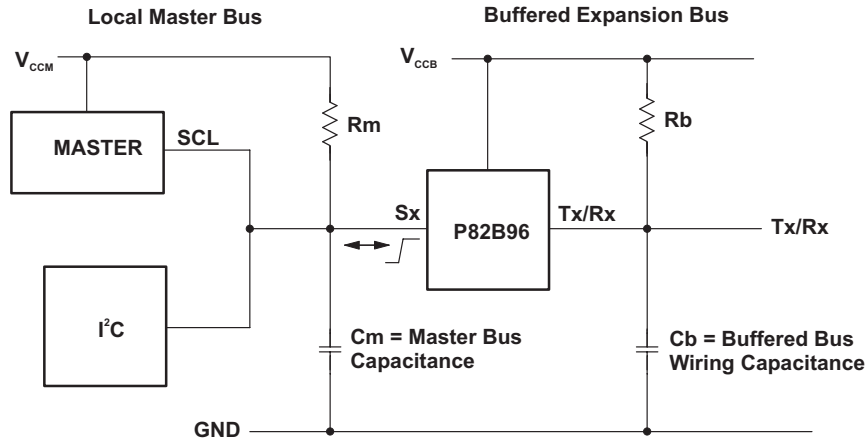
Calculating System Delays and Bus-Clock Frequency for Fast Mode System

Figure 7 through Figure 9 show the P82B96 used to drive extended bus wiring, with relatively large capacitance, linking two Fast mode I^2C bus nodes. It includes simplified expressions for making the relevant timing calculations for 3.3-/5-V operation. Because the buffers and the wiring introduce timing delays, it may be necessary to decrease the nominal SCL frequency below 400 kHz. In most cases, the actual bus frequency is lower than the nominal master timing, due to bit-wise stretching of the clock periods.



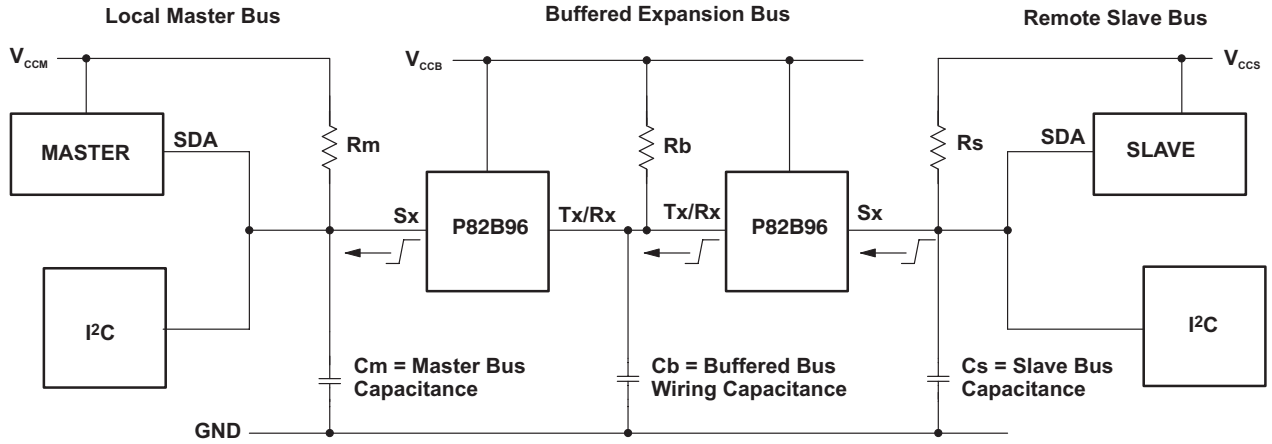
Falling edge of SCL at master is delayed by the buffers and bus fall times.
Effective Delay of SCL at Slave = 255 + 17 V_{CCM} + (2.5 + 4 × 10^9 Cb) V_{CCB} (ns)
C = F, V = Volts

Figure 7.



Rising edge of SCL at master is delayed (clock stretch) by buffer and bus rise times.
Effective delay of SCL at master = 270 + RmCm + 0.7RbCb (ns)
C = F, R = Ω

Figure 8.



Rising edge of SDA at slave is delayed by the buffers and bus rise times.
Effective delay of SDA at master = 270 + 0.2RsCs + 0.7(RbCb + RmCm) (ns)
C = F, R = Ω

Figure 9.

The delay factors involved in calculation of the allowed bus speed are:

1. The propagation delay of the master signal through the buffers and wiring to the slave. The important delay is that of the falling edge of SCL, because this edge requests the data or ACK from a slave.
2. The effective stretching of the nominal low period of SCL at the master, caused by the buffer and bus rise times.
3. The propagation delay of the slave response signal through the buffers and wiring back to the master. The important delay is that of a rising edge in the SDA signal. Rising edges always are slower and, therefore, are delayed by a longer time than falling edges. (The rising edges are limited by the passive pullup, while falling edges actively are driven.)

The timing requirement in any I^2C system is that a slave's data response (which is provided in response to a falling edge of SCL) must be received at the master before the end of the corresponding low period of SCL as it appears on the bus wiring at the master. Because all slaves, as a minimum, satisfy the worst-case timing requirements of a 400-kHz part, they must provide their response within the minimum allowed clock low period of 1300 ns. Therefore, in systems that introduce additional delays, it is necessary only to extend that minimum clock low period by any effective delay of the slave response. The effective delay of the slave's response equals the total delays in SCL falling edge from the master reaching the slave (A) minus the effective delay (stretch) of the SCL rising edge (B) plus total delays in the slave response data, carried on SDA, and reaching the master (C).

The master microcontroller should be programmed to produce a nominal SCL low period of (1300 + A – B + C) ns and should be programmed to produce the nominal minimum SCL high period of 600 ns. Then, a check should be made to ensure the cycle time is not shorter than the minimum 2500 ns. If found to be necessary, increase either clock period.

Due to clock stretching, the SCL cycle time always is longer than (600 + 1300 + A + C) ns.

Sample Calculations

The master bus has an RmCm product of 100 ns and V_{CCM} = 5 V.

The buffered bus has a capacitance of 1 nF and a pullup resistor of 160 Ω to 5 V, giving an RbCb product of 160 ns. The slave bus also has an RsCs product of 100 ns.

The master low period should be programmed to be ≥(1300 + 372.5 – 482 + 472) ns, which calculates to ≥1662.5 ns.

The master high period may be programmed to the minimum 600 ns. The nominal master clock period is ≥(1662.5 + 600) ns = 2262.5 ns, equivalent to a frequency of 442 kHz.

The actual bus-clock period, including the 482-ns clock stretch effect, is below (nominal + stretch) = (2262.5 + 482) ns or ≥2745 ns, equivalent to an allowable frequency of 364 kHz.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
P82B96D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7DS	Samples
P82B96DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7DS	Samples
P82B96DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	P82B96P	Samples
P82B96PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples
P82B96PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PG96	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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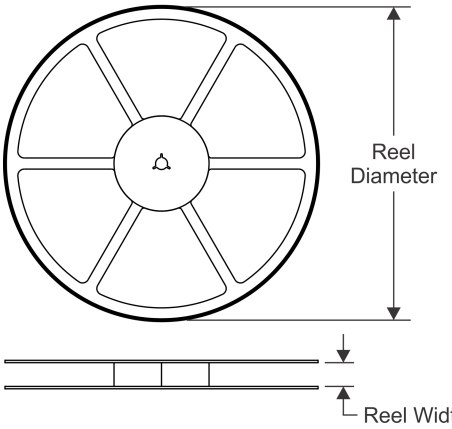
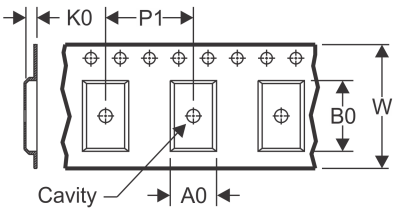
TAPE AND REEL INFORMATION

REEL DIMENSIONS

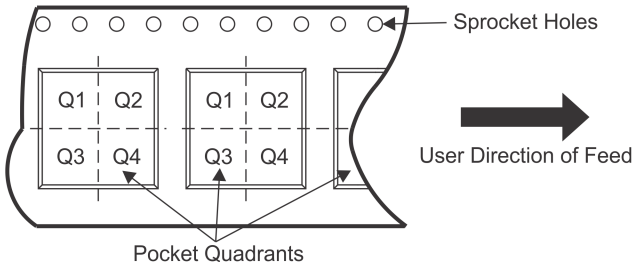


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

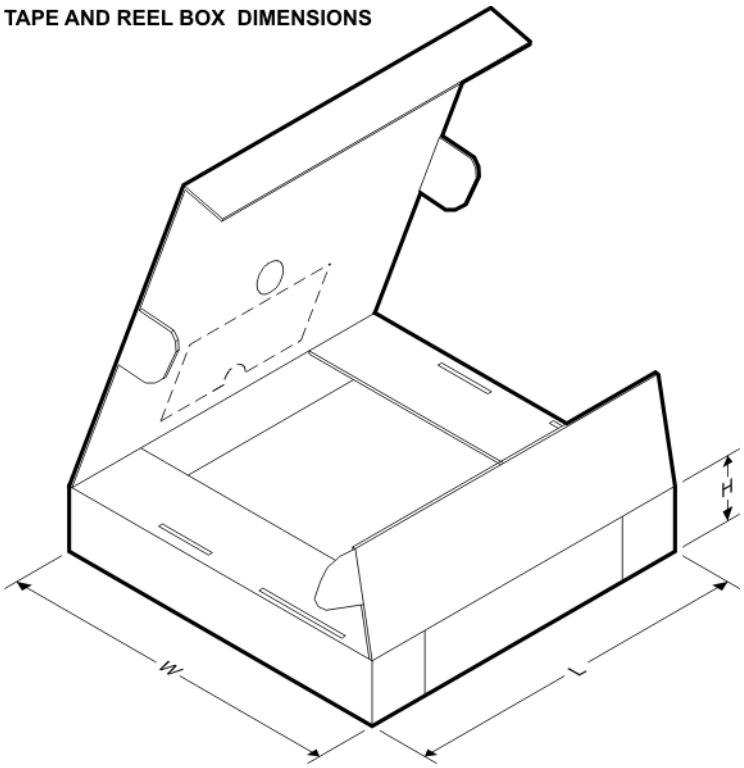
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
P82B96DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
P82B96DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
P82B96PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

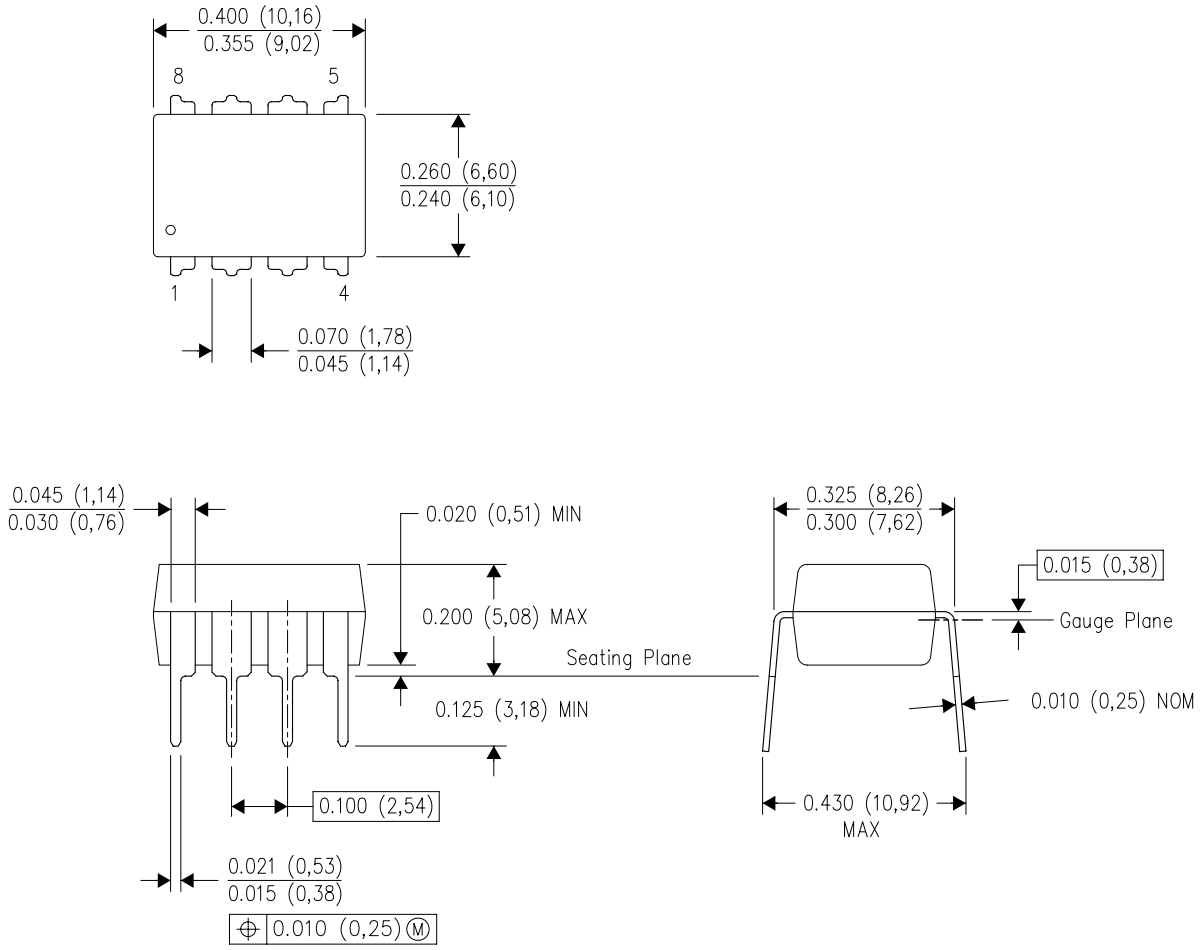
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

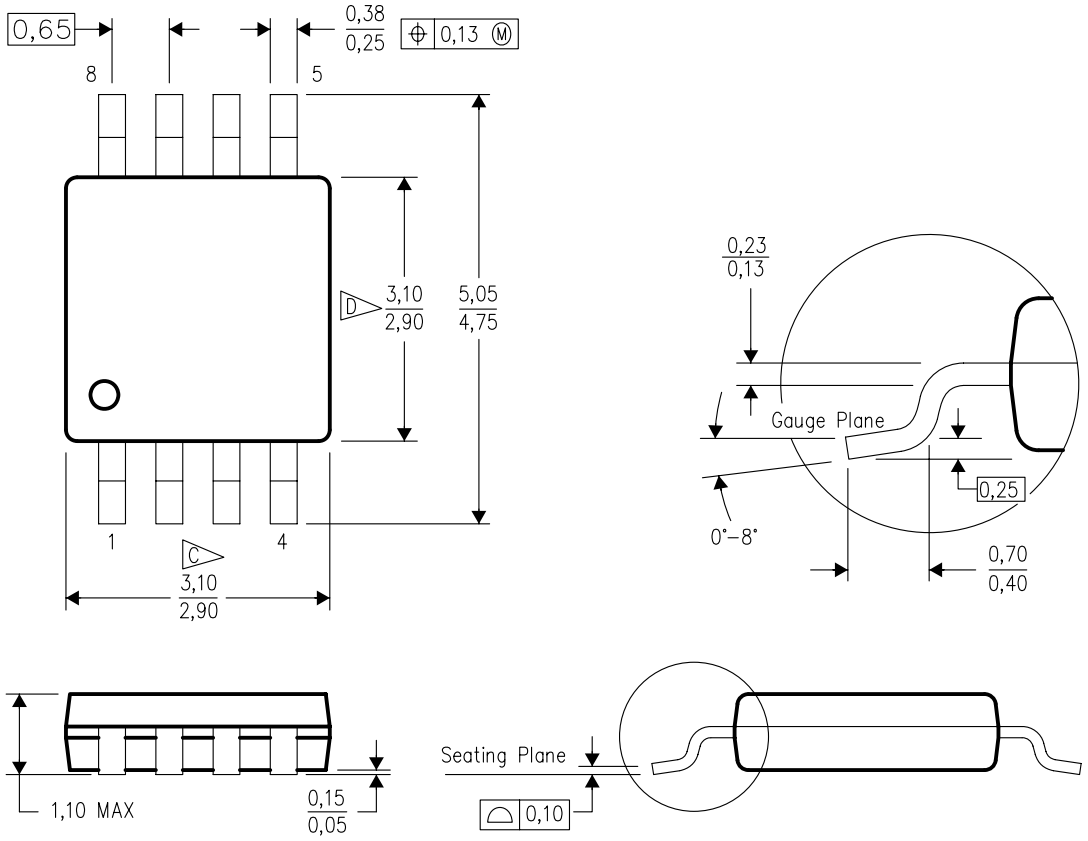
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
P82B96DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
P82B96DR	SOIC	D	8	2500	367.0	367.0	35.0
P82B96PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

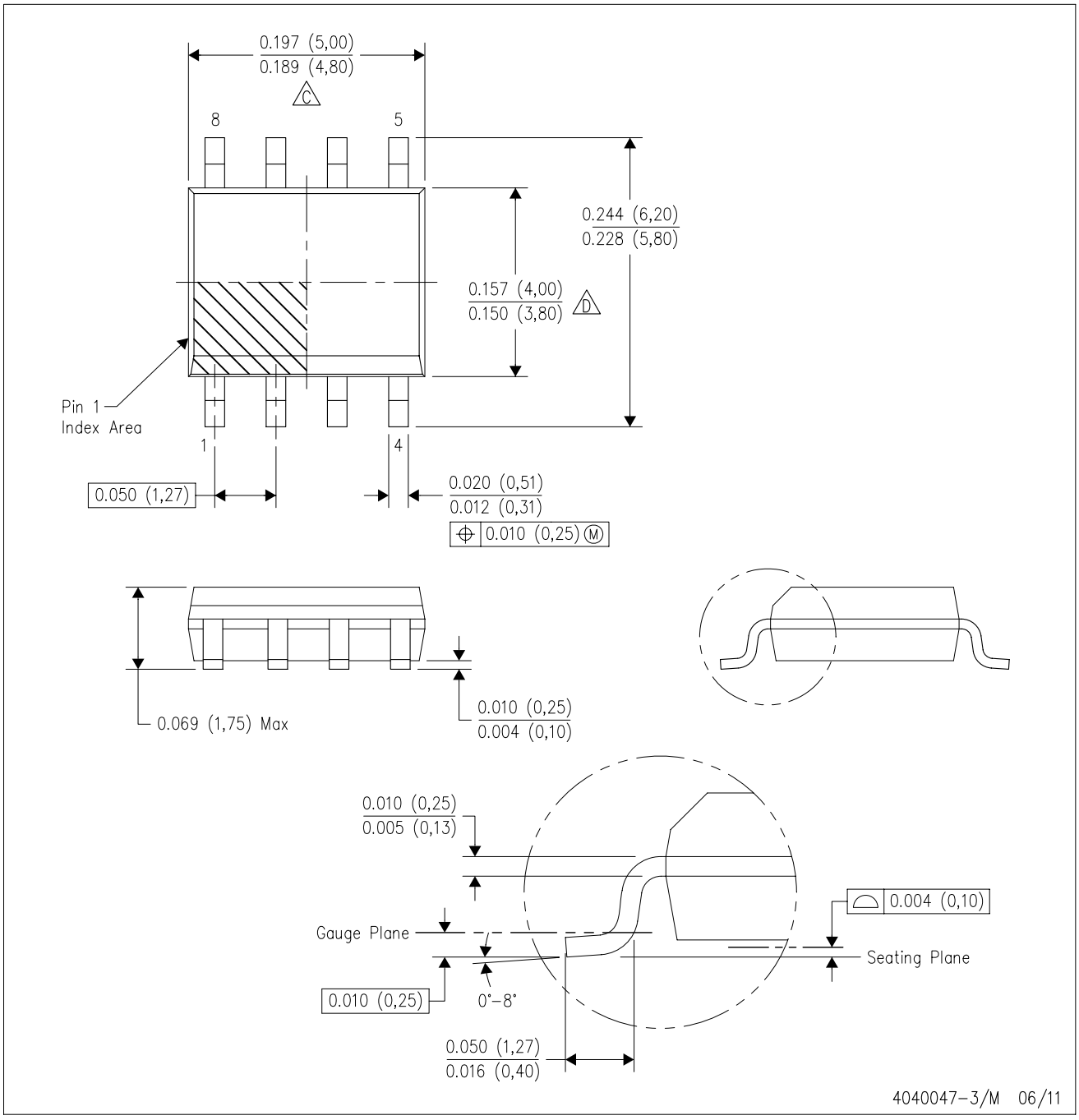
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

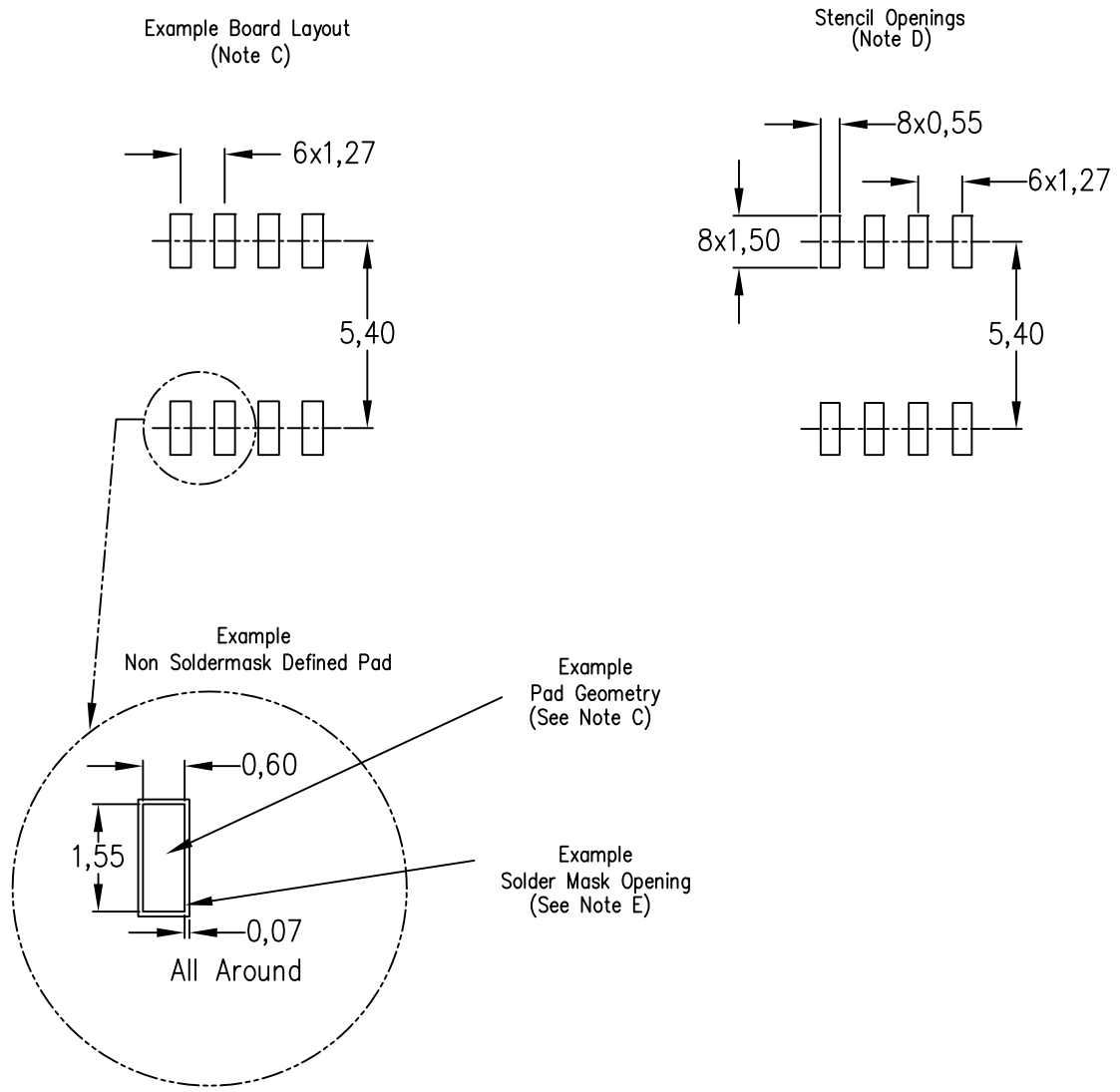
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



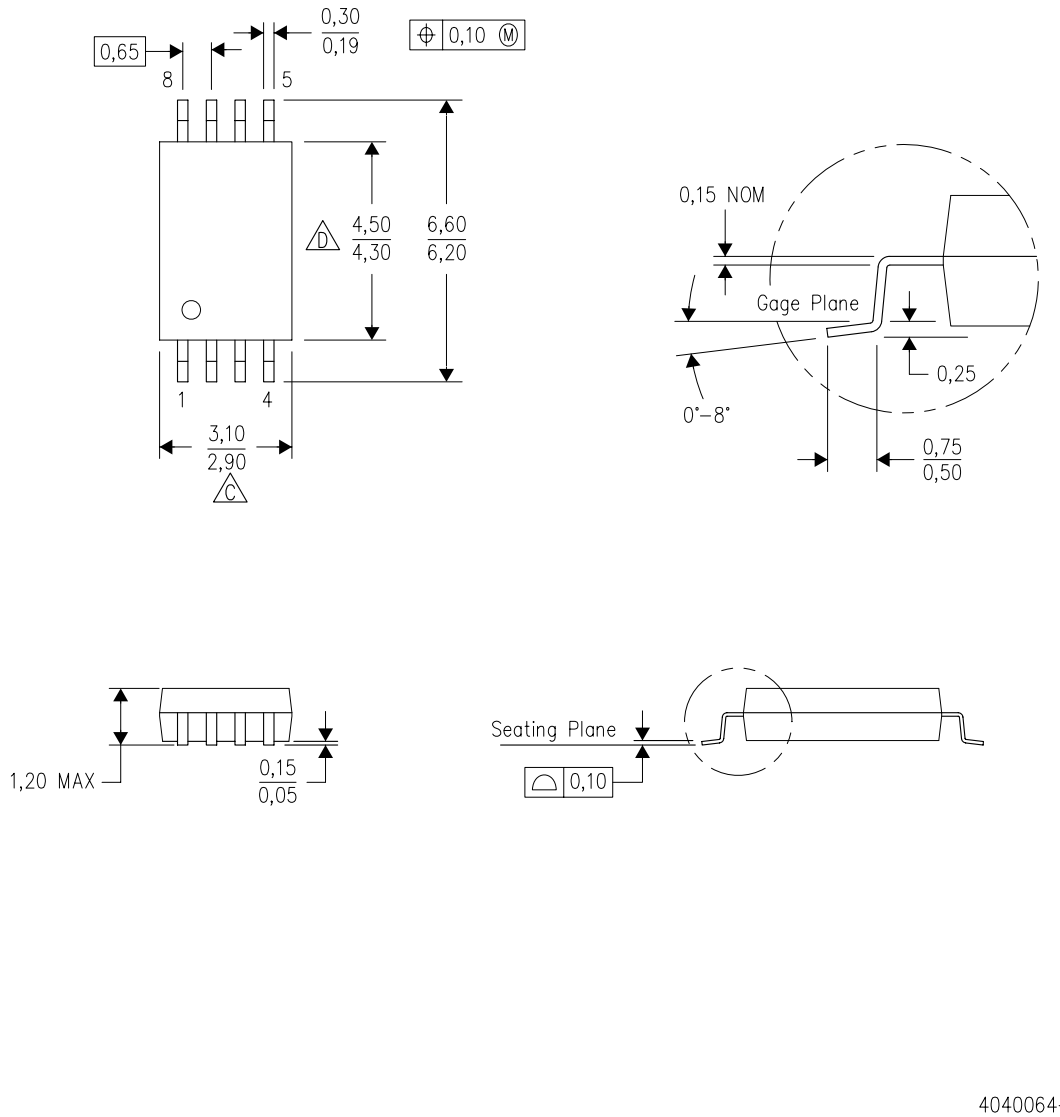
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040064–2/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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