Unity-Gain Stable, Wideband Voltage Limiting Amplifier

FEATURES

- HIGH LINEARITY NEAR LIMITING
- FAST RECOVERY FROM OVERDRIVE: 1ns
- LIMITING VOLTAGE ACCURACY: ±10mV
- –3dB BANDWIDTH (G = +1): 450MHz
- GAIN BANDWIDTH PRODUCT: 250MHz
- SLEW RATE: 1100V/µs
- ±5V AND +5V SUPPLY OPERATION
- HIGH-GAIN VERSION AVAILABLE: OPA699

APPLICATIONS

- FAST LIMITING ANALOG-TO-DIGITAL CONVERTER (ADC) INPUT BUFFERS
- CCD PIXEL CLOCK STRIPPING
- VIDEO SYNC STRIPPING
- HF MIXERS
- IF LIMITING AMPLIFIERS
- AM SIGNAL GENERATION
- NONLINEAR ANALOG SIGNAL PROCESSING
- OPA688 UPGRADE

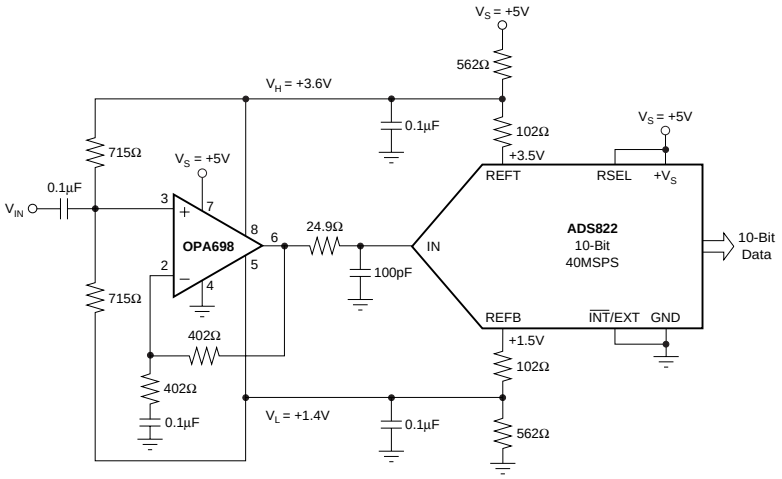
DESCRIPTION

The OPA698 is a wideband, unity-gain stable voltage-feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±10mV. The op amp operates linearly to within 20mV of the output limit voltages.

The combination of a narrow nonlinear range and the low limiting offset allows the limiting voltages to be set within 100mV of the desired linear output range. A fast 1ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA698 to be used in all standard op amp applications.

Nonlinear analog signal processing will benefit from the ability of the OPA698 to sharply transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

The OPA698 is available in an industry standard pinout SO-8 package. For higher gain, or transimpedance applications requiring output limiting with fast recovery, consider the OPA699.



Single-Supply Limiting ADC Input Driver

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Characteristics
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Limiter Voltage Range	$\pm(V_S - 0.7V)$
Storage Temperature Range: ID	–65°C to +125°C
Lead Temperature (SO-8, soldering, 3s)	+260°C
ESD Resistance: HBM	2000V
MM	200V
CDM	1000V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RELATED PRODUCTS

	SINGLES	DUALS	DESCRIPTION
Output Limiting	OPA699		High Gain BW, Non-unity Gain Stable
Voltage Feedback	OPA690	OPA2690	High Slew, Unity Gain Stable

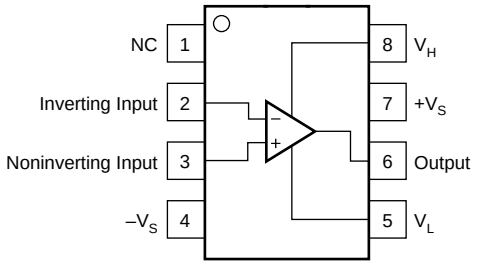
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA698	SO-8 Surface Mount	D	–40°C to +85°C	OPA698ID	OPA698ID	Rails, 100
"	"	"	"	"	OPA698IDR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

Top View **SO**



NC = Not Connected

ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C.**

G = +2, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA698ID TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	V_O < 0.2V_{PP}							
	G = +1, R_F = 25Ω	450				MHz	typ	C
	G = +2	215	150	145	140	MHz	min	B
	G = –1	215				MHz	typ	C
Gain-Bandwidth Product (G ≥ +5)	V_O < 0.2V_{PP}	250	180	175	170	MHz	min	B
Gain Peaking	G = +1, R_F = 25Ω, V_O < 0.2V_{PP}	5				dB	typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.2V_{PP}	30				MHz	typ	C
Large-Signal Bandwidth	V_O = 4V_{PP}, V_H = –V_L = 2.5V	160	110	105	100	MHz	min	B
Step Response:								
Slew Rate	4V Step, V_H = –V_L = 2.5V	1100	750	700	650	V/µs	min	B
Rise-and-Fall Time	0.2V Step	1.6	2.3	2.4	2.5	ns	max	B
Settling Time: 0.05%	2V Step	8				ns	typ	C
Harmonic Distortion: 2nd	f = 5MHz, V_O = 2V_{PP}	–74	–65	–64	–63	dB	min	B
3rd	f = 5MHz, V_O = 2V_{PP}	–87	–83	–83	–82	dB	min	B
Differential Gain	NTSC, PAL, R_L = 500Ω	0.012				%	typ	C
Differential Phase	NTSC, PAL, R_L = 500Ω	0.008				degrees	typ	C
Input Noise:								
Voltage Noise Density	f ≥ 1MHz	5.6	6.1	6.7	7.2	nV/√Hz	max	B
Current Noise Density	f ≥ 1MHz	2.2	2.7	2.8	3	pA/√Hz	max	B
DC PERFORMANCE (V_{CM} = 0)								
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.5V	63	**56**	53	52	dB	min	A
Input Offset Voltage		±2	**±5**	±6	±8	mV	max	A
Average Drift		—		±15	±20	µV/°C	max	B
Input Bias Current(4)		+3	**±10**	±11	±12	µA	max	A
Average Drift		—		±15	±20	nA/°C	max	B
Input Offset Current		±0.3	**±2**	±2.5	±3	µA	max	A
Average Drift		—		±10	±10	nA/°C	max	B
INPUT								
Common-Mode Rejection	Input Referred, V_{CM} = ±0.5V	61	**55**	54	52	dB	min	A
Common-Mode Input Range(5)		±3.3	**±3.2**	±3.2	±3.1	V	min	A
Input Impedance								
Differential-Mode		0.32 || 1				MΩ || pF	typ	C
Common-Mode		3.5 || 1				MΩ || pF	typ	C
OUTPUT	V_H = –V_L = 4.3V							
Output Voltage Range	R_L ≥ 500Ω	±4.0	**±3.9**	±3.9	±3.8	V	min	A
Current Output, Sourcing	V_O = 0	+120	**+90**	+85	+80	mA	min	A
Sinking	V_O = 0	–120	**–90**	–85	–80	mA	min	A
Closed-Loop Output Impedance	G = +1, R_F = 25Ω, f < 100kHz	0.01				Ω	typ	C
POWER SUPPLY								
Operating Voltage, Specified		±5				V	typ	C
Maximum		**—**	**±6**	±6	±6	V	max	A
Quiescent Current, Maximum	V_S = ±5V	15.5	**15.9**	16.3	16.6	mA	max	A
Minimum	V_S = ±5V	15.5	**15.2**	14.9	14.6	mA	min	A
Power-Supply Rejection Ratio	+V_S = 4.5V to 5.5V							
–PSRR (Input Referred)		75	**68**	67	66	dB	min	A
OUTPUT VOLTAGE LIMITERS								
Output Voltage Limited Range	Pins 5 and 8	±3.8				V	max	C
Default Limit Voltage, Upper	Limiter Pins Open	+3.5	**+3.3**	+3.2	+3.1	V	min	A
Lower	Limiter Pins Open	–3.5	**–3.3**	–3.2	–3.1	V	max	A
Minimum Limiter Separation (V_H – V_L)		400	400	400	400	mV	min	B
Maximum Limit Voltage		—	±4.3	±4.3	±4.3	V	max	B
Limiter Input Bias Current Magnitude (6)	V_O = 0							
Maximum		50	**60**	62	64	µA	max	A
Minimum		50	**40**	38	36	µA	min	A
Average Drift		—		30	35	nA/°C	max	B
Limiter Input Impedance		3.4 || 1				MΩ || pF	typ	C
Limiter Feedthrough(7)	f = 5MHz	–68				dB	typ	C
DC Performance in Limit Mode	V_{IN} = ±2V							
Limiter Offset	(V_O – V_H) or (V_O – V_L)	±10	**±30**	±35	±40	mV	max	A
Op Amp Input Bias Current Shift(4)	Linear to Limited Output	3				µA	typ	C
AC Performance in Limit Mode								
Limiter Small-Signal Bandwidth	2V_{DC} + 20mV_{PP}	600				MHz	typ	C
Limiter Slew Rate(8)	2x Overdrive, V_H or V_L	125				V/µs	typ	C

ELECTRICAL CHARACTERISTICS: V_S = ±5V (Cont.)

Boldface limits are tested at **+25°C.**

G = +2, R_F = 402Ω, R_L = 500Ω, and V_H = –V_L = 2V (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA698ID TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
OUTPUT VOLTAGE LIMITERS (Cont.)								
Limited Step Response	2x Overdrive							
Overshoot	V_{IN} = 0 to ±2V Step	250				mV	typ	C
Recovery Time	V_{IN} = ±2V to 0V Step	1	1.9	2	2.1	ns	max	B
Linearity Guardband(9)	f = 5MHz, V_O = $2V_{PP}$	30				mV	typ	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification: I	–40 to +85				°C	typ	C
Thermal Resistance	Junction-to-Ambient							
D SO-8		125	—	—	—	°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive out of node.

(5) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.

(6) I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3, Figure 1, and Figure 8.

(7) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.

(8) V_H slew rate conditions are: V_{IN} = +2V, G = +2, V_L = –2V, V_H = step between 2V and 0V. V_L slew rate conditions are similar.

(9) Linearity Guardband is defined for an output sinusoid (f = 5MHz, V_O = $0V_{DC}$ ± $1V_{PP}$) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 9).

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

G = +2, R_L = 500Ω tied to V_{CM} = 2.5V, R_F = 402Ω, V_L = V_{CM} –1.2V, and V_H = V_{CM} +1.2V (see Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA698ID TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth	V_O < 0.2V_{PP}							
	G = +1, R_F = 25Ω	375				MHz	typ	C
	G = +2	200	150	145	140	MHz	min	B
	G = –1	200				MHz	typ	C
Gain-Bandwidth Product (G ≥ +5)	V_O < 0.2V_{PP}	230	170	165	155	MHz	min	B
Gain Peaking	G = +1, R_F = 25Ω, V_O < 0.2V_{PP}	7				dB	typ	C
0.1dB Gain Flatness Bandwidth	V_O < 0.2V_{PP}	30				MHz	typ	C
Large-Signal Bandwidth	V_O = 2V_{PP}	200	120	110	100	MHz	min	B
Step Response:								
Slew Rate	2V Step	820	560	550	500	V/µs	min	B
Rise-and-Fall Time	0.2V Step	1.9	2.3	2.4	2.5	ns	max	B
Settling Time: 0.05%	1V Step	12				ns	typ	C
Harmonic Distortion: 2nd	f = 5MHz, V_O = 2V_{PP}	69	63	62	61	dB	min	B
3rd	f = 5MHz, V_O = 2V_{PP}	73	69	68	67	dB	min	B
Input Noise:								
Voltage Noise Density	f ≥ 1MHz	5.7				nV/√Hz	typ	C
Current Noise Density	f ≥ 1MHz	2.3				pA/√Hz	typ	C
DC PERFORMANCE	V_{CM} = 2.5V							
Open-Loop Voltage Gain (A_{OL})	V_O = ±0.5V	60	**54**	52	51	dB	min	A
Input Offset Voltage		±1	**±6**	±7	±8	mV	max	A
Average Drift		—		±15	±15	µV/°C	max	B
Input Bias Current(4)		+3	**±10**	±11	±12	µA	max	A
Average Drift		—		±25	±25	nA/°C	max	B
Input Offset Current		±0.4	**±2**	±2.5	±3	µA	max	A
Average Drift		—		±15	±15	nA/°C	max	B
INPUT								
Common-Mode Rejection	Input Referred, V_{CM} = ±0.5V	58	**54**	53	52	dB	min	A
Common-Mode Input Range(5)		V_{CM} ± 0.8	**V_{CM} ± 0.7**	V_{CM} ± 0.7	V_{CM} ± 0.6	V	min	A
Input Impedance								
Differential-Mode		0.32 || 1				MΩ || pF	typ	C
Common-Mode		3.5 || 1				MΩ || pF	typ	C
OUTPUT	V_H = V_{CM} +1.8V, V_L = V_{CM} – 1.8V							
Output Voltage Range	R_L ≥ 500Ω	V_{CM} ± 1.6	**V_{CM} ± 1.4**	V_{CM} ± 1.4	V_{CM} ± 1.3	V	min	A
Current Output, Sourcing	V_O = 2.5V	+70	**+60**	+55	+50	mA	min	A
Sinking	V_O = 2.5V	–70	**–60**	–55	–50	mA	min	A
Closed-Loop Output Impedance	G = +1, R_F = 25Ω, f < 100kHz	0.2				Ω	typ	C
POWER SUPPLY	Single-Supply Operation							
Operating Voltage, Specified		+5				V	typ	C
Maximum		—	**+12**	+12	+12	V	max	A
Quiescent Current, Maximum	V_S = +5V	14.3	**14.9**	15.1	15.3	mA	max	A
Minimum	V_S = +5V	14.3	**13.6**	13.4	13.2	mA	min	A
Power-Supply Rejection Ratio	V_S = 4.5V to 5.5V							
+PSRR (Input Referred)		70				dB	typ	C
OUTPUT VOLTAGE LIMITERS								
Maximum Limiter Voltage	Pins 5 and 8	+3.9				V	typ	C
Minimum Limiter Voltage	Pins 5 and 8	+1.1				V	typ	C
Default Limiter Voltage	Limiter Pins Open	V_{CM} ± 1.1	V_{CM} ± 0.8	V_{CM} ± 0.7	V_{CM} ± 0.6	V	min	B
Minimum Limiter Separation (V_H – V_L)		400	400	400	400	mV	min	B
Maximum Limit Voltage		—	V_{CM} ± 1.8	V_{CM} ± 1.8	V_{CM} ± 1.8	V	max	B
Limiter Input Bias Current Magnitude(6)	V_O = 2.5V	16				µA	typ	C
Limiter Input Impedance		3.4 || 1				MΩ || pF	typ	C
Limiter Feedthrough(7)	f = 5MHz	–60				dB	typ	C
DC Performance in Limit Mode	V_{IN} = V_{CM} ± 1.2V							
Limiter Voltage Accuracy	(V_O – V_H) or (V_O – V_L)	±15	**±30**	±35	±40	mV	max	A
Op Amp Bias Current Shift(4)	Linear to Limited Output	5				µA	typ	C
AC Performance in Limit Mode								
Limiter Small-Signal Bandwidth	V_{IN} = V_{CM} ± 1.2V, V_O < 0.02V_{PP}	450				MHz	typ	C
Limiter Slew Rate(8)	2x Overdrive, V_H or V_L	100				V/µs	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V (Cont.)

Boldface limits are tested at **+25°C.**

G = +2, R_L = 500Ω tied to V_{CM} = 2.5V, R_F = 402Ω, V_L = V_{CM} –1.2V, and V_H = V_{CM} +1.2V (see Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA698ID TYP +25°C	MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
OUTPUT VOLTAGE LIMITERS (Cont.)								
Limited Step Response	2x Overdrive							
Overshoot	V_{IN} = V_{CM} to V_{CM} ± 1.2V Step	55				mV	typ	C
Recovery Time	V_{IN} = V_{CM} ± 1.2V to V_{CM} Step	3				ns	typ	C
Linearity Guardband(9)	f = 5MHz, V_O = $2V_{PP}$	30				mV	typ	C
THERMAL CHARACTERISTICS								
Temperature Range	Specification: I	–40 to +85				°C	typ	C
Thermal Resistance	Junction-to-Ambient							
D SO-8		125	—	—	—	°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications.

(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive out of node.

(5) CMIR tested as < 3dB degradation from minimum CMRR at specified limits.

(6) I_{VH} (V_H bias current) is negative, and I_{VL} (V_L bias current) is positive, under these conditions. See Note 3, Figures 2, and Figure 8.

(7) Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.

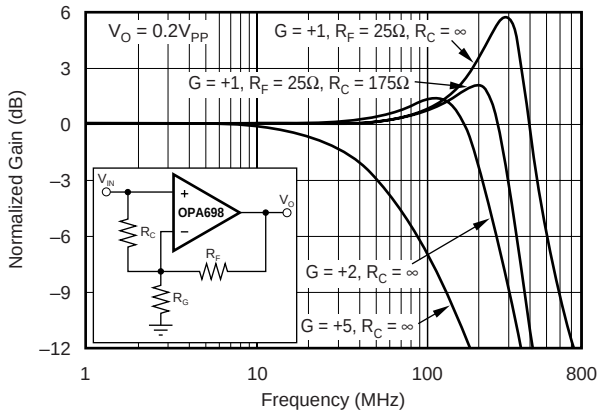
(8) V_H slew rate conditions are: V_{IN} = V_{CM} + 0.4V, G = +2, V_L = V_{CM} – 1.2V, V_H = step between V_{CM} + 1.2V and V_{CM}. V_L slew rate conditions are similar.

(9) Linearity Guardband is defined for an output sinusoid (f = 5MHz, V_O = V_{CM} ± $1V_{PP}$) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 9).

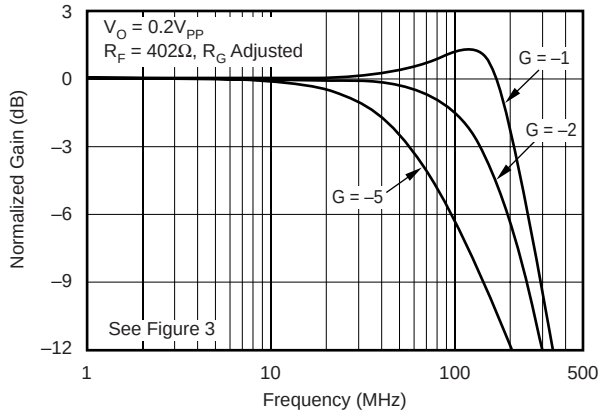
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω, $V_H = -V_L$ = 2V, unless otherwise noted.

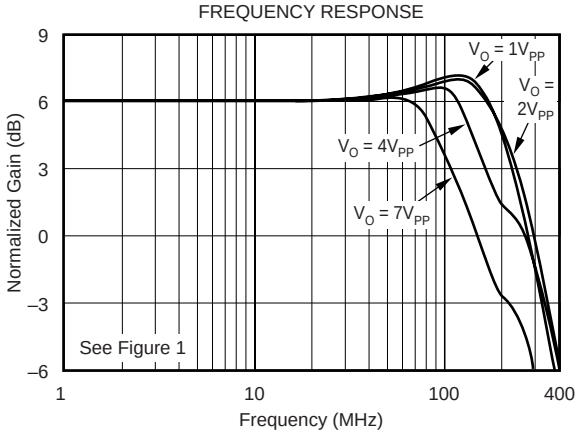
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



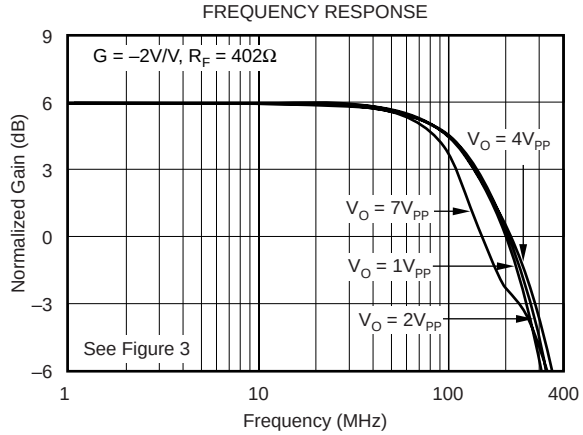
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



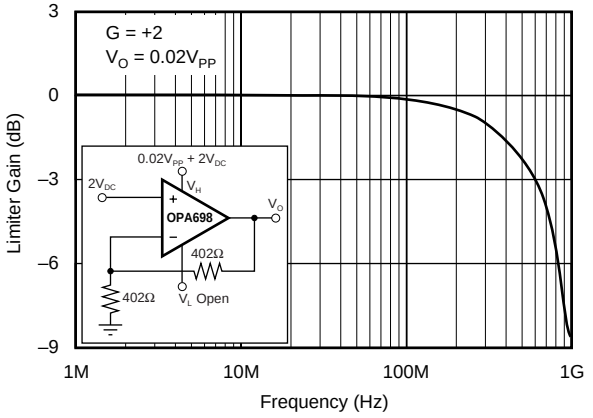
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



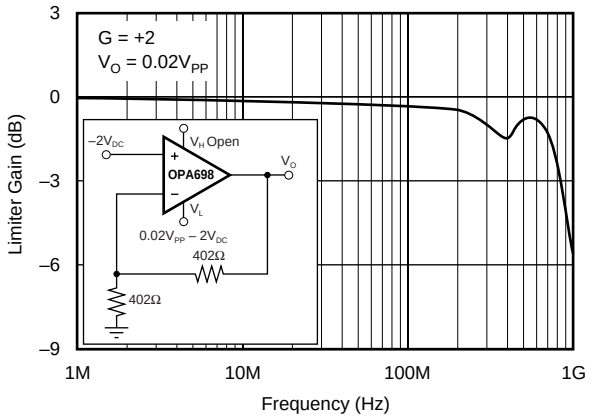
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



V_H—LIMITER SMALL-SIGNAL FREQUENCY RESPONSE



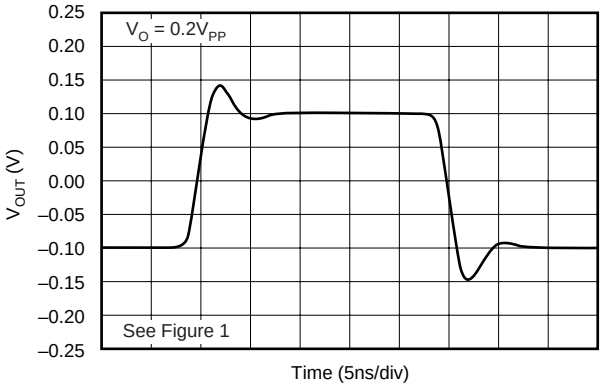
V_L—LIMITER SMALL-SIGNAL FREQUENCY RESPONSE



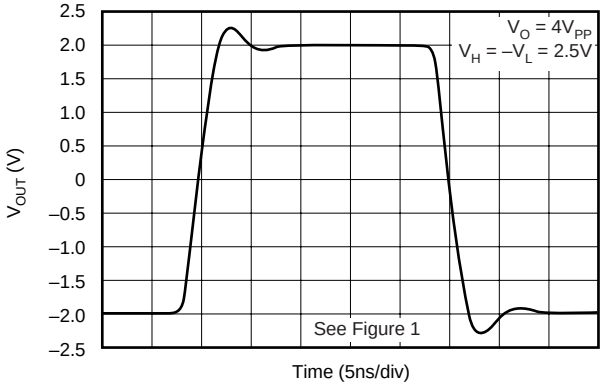
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω, V_H = –V_L = 2V, unless otherwise noted.

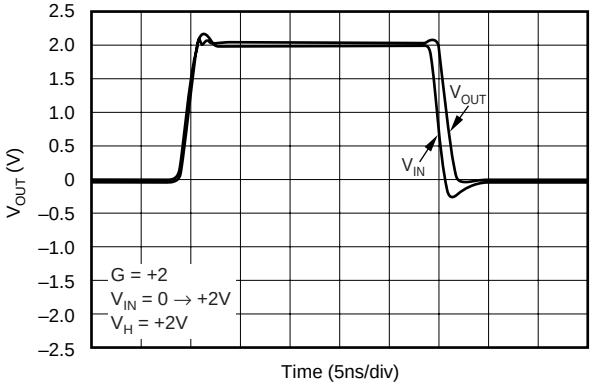
SMALL-SIGNAL PULSE RESPONSE



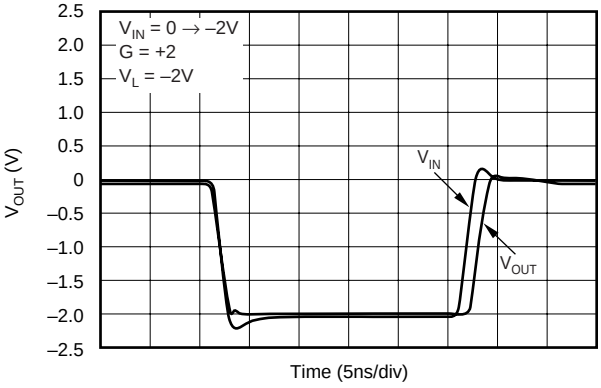
LARGE-SIGNAL PULSE RESPONSE



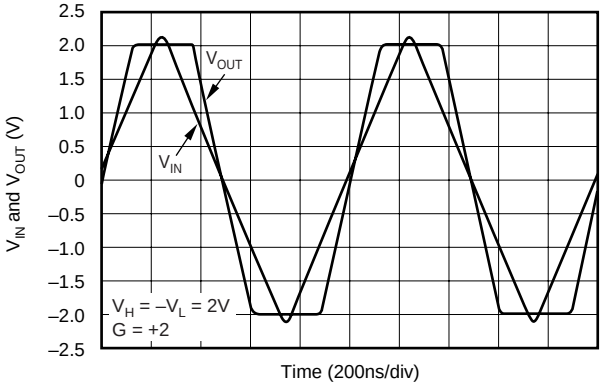
V_H—LIMITED PULSE RESPONSE



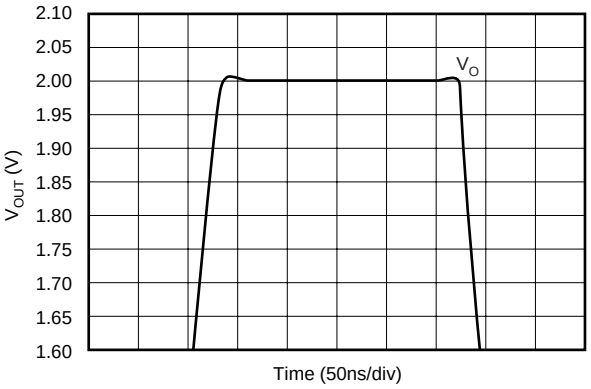
V_L—LIMITED PULSE RESPONSE (20MHz)



LIMITED OUTPUT RESPONSE

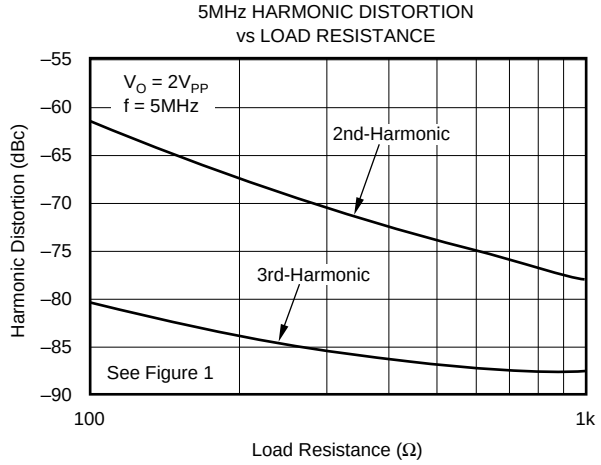


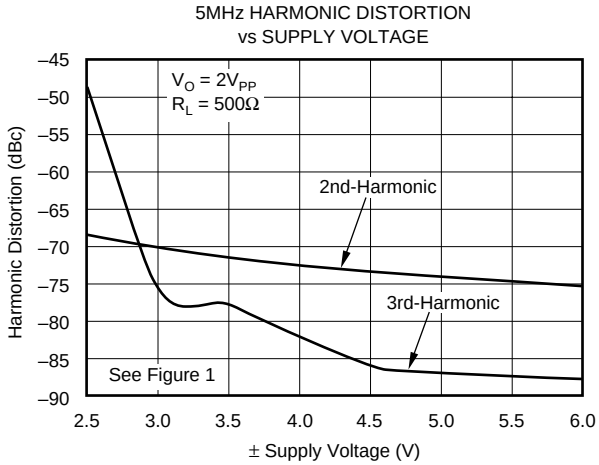
DETAIL OF LIMITED OUTPUT VOLTAGE

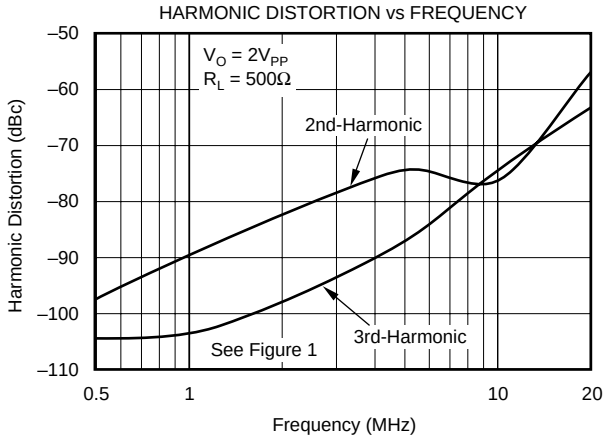


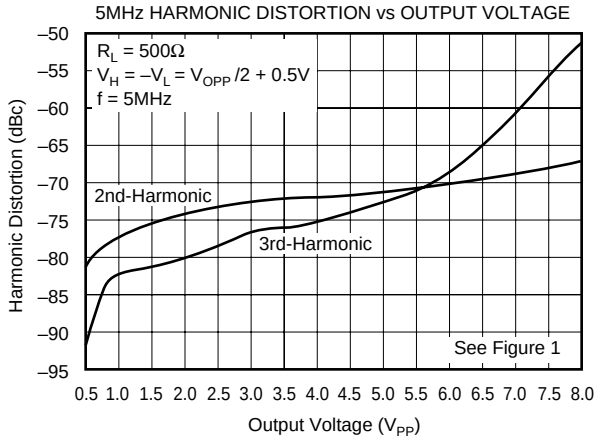
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

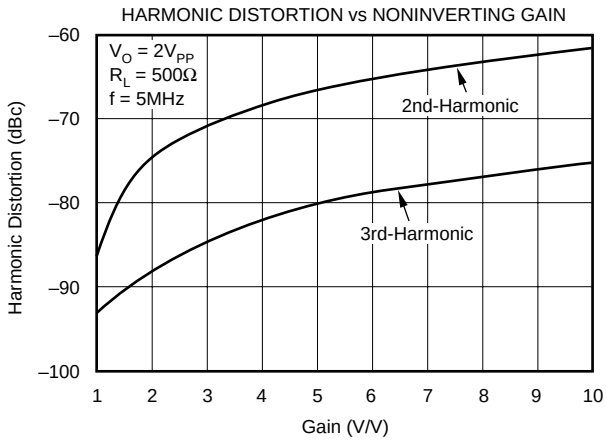
T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω, V_H = –V_L = 2V, unless otherwise noted.

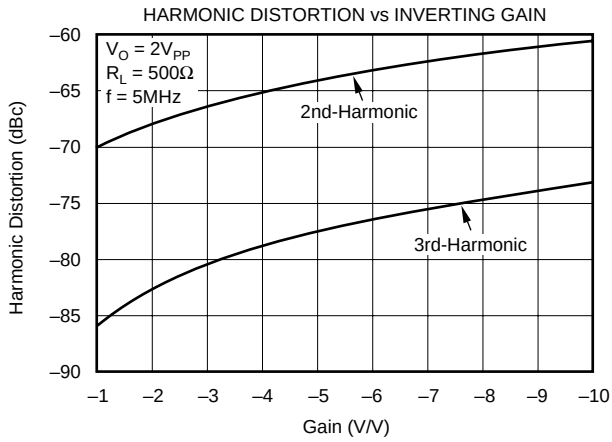








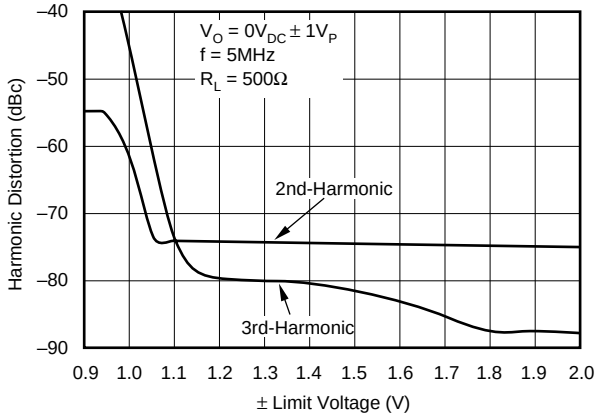




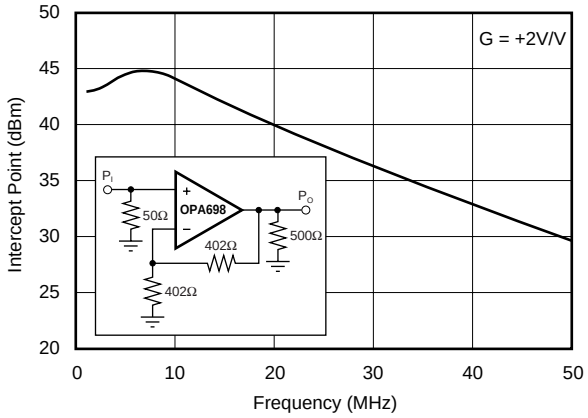
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω, V_H = –V_L = 2V, unless otherwise noted.

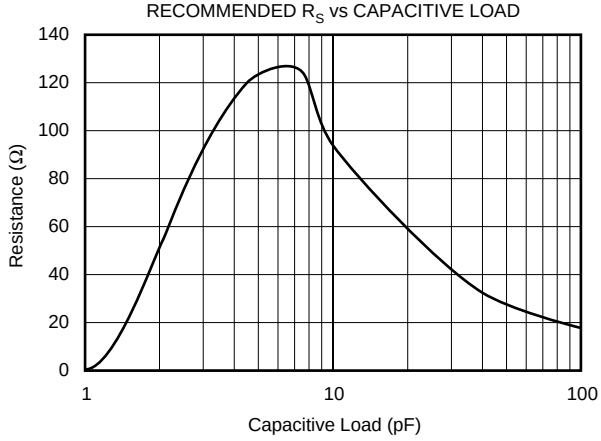
HARMONIC DISTORTION NEAR LIMITING VOLTAGES



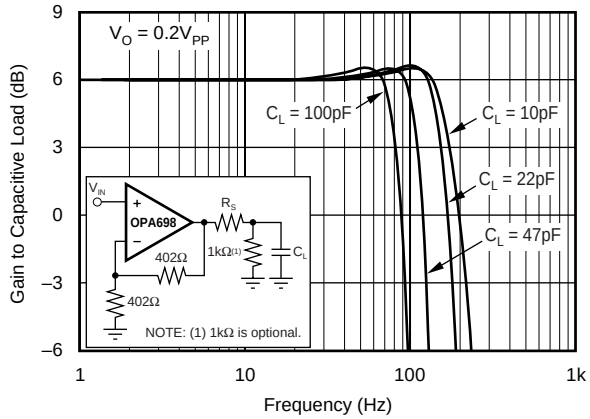
2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT ±5V 500Ω



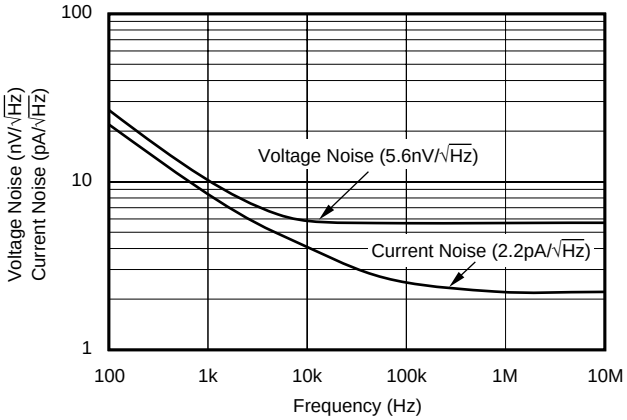
RECOMMENDED R_S vs CAPACITIVE LOAD



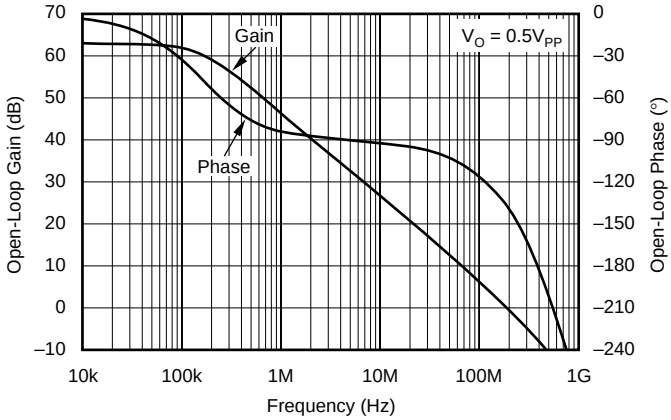
FREQUENCY RESPONSE vs CAPACITIVE LOAD



INPUT VOLTAGE AND CURRENT NOISE DENSITY

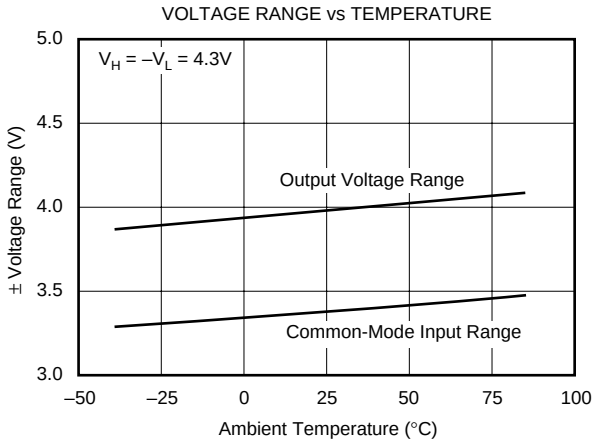


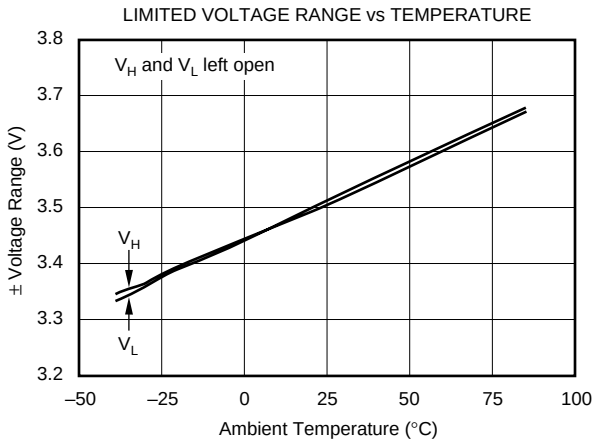
OPEN-LOOP FREQUENCY RESPONSE

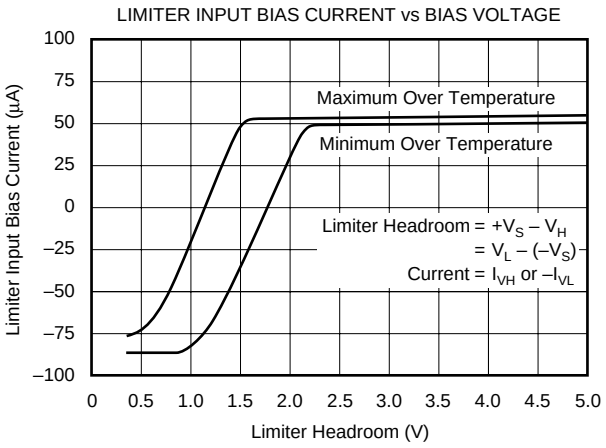


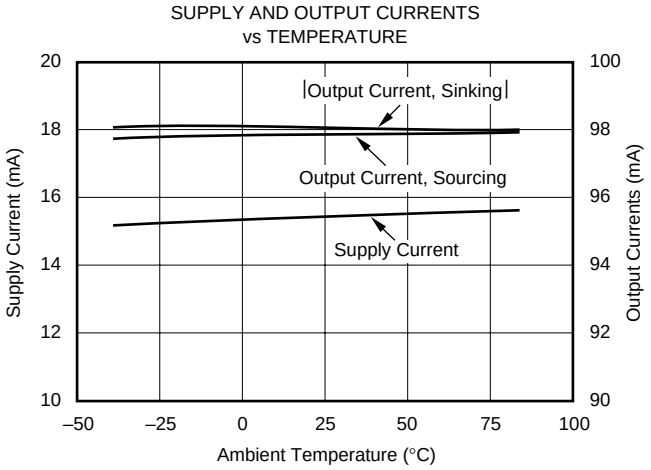
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

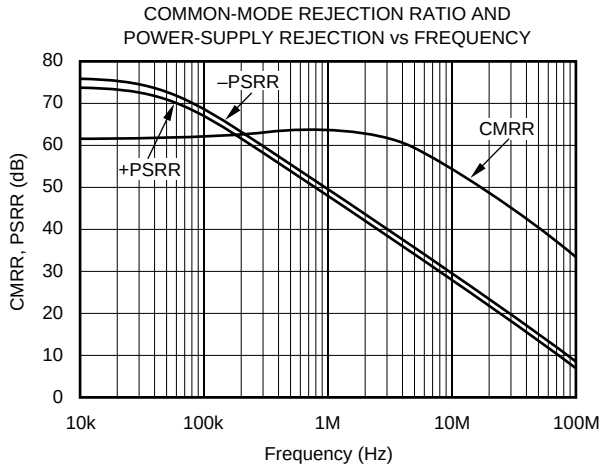
T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω, V_H = –V_L = 2V, unless otherwise noted.

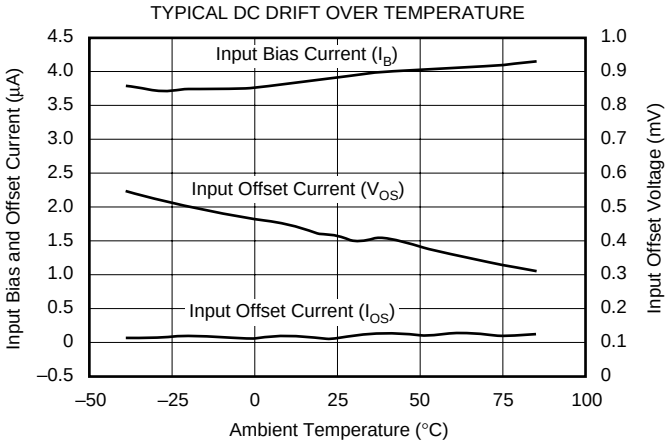






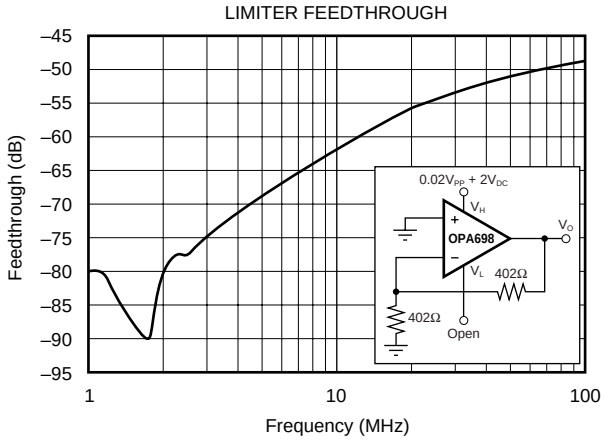


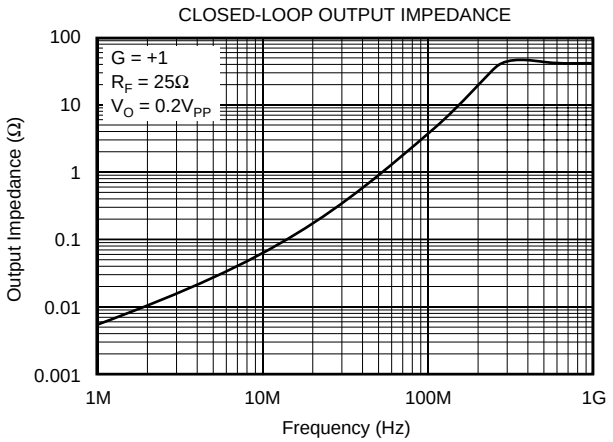


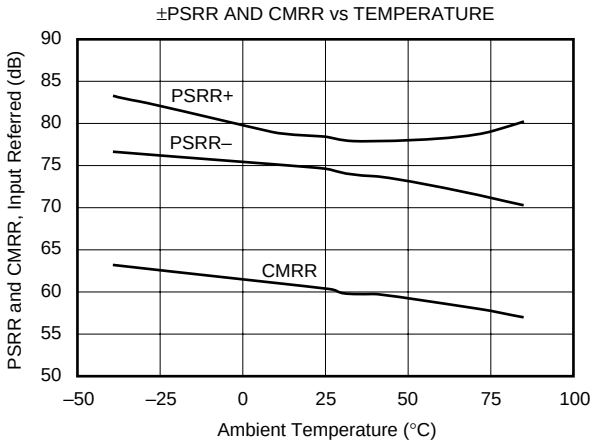


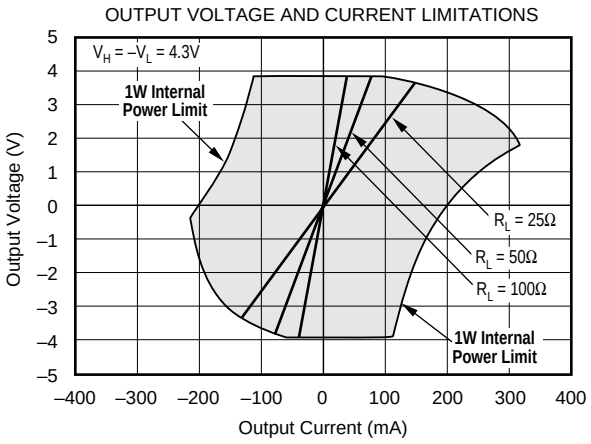
TYPICAL CHARACTERISTICS: V_S = ±5V (Cont.)

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω, V_H = –V_L = 2V, unless otherwise noted.





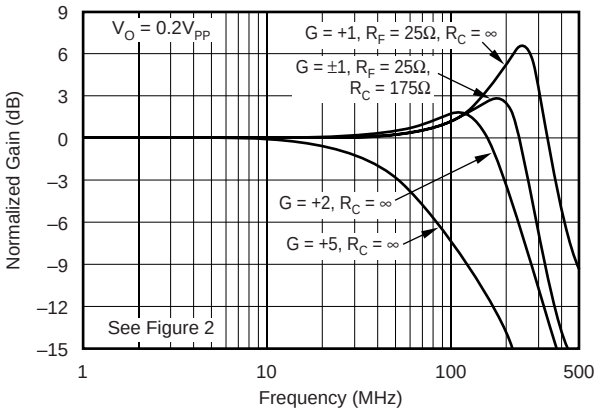




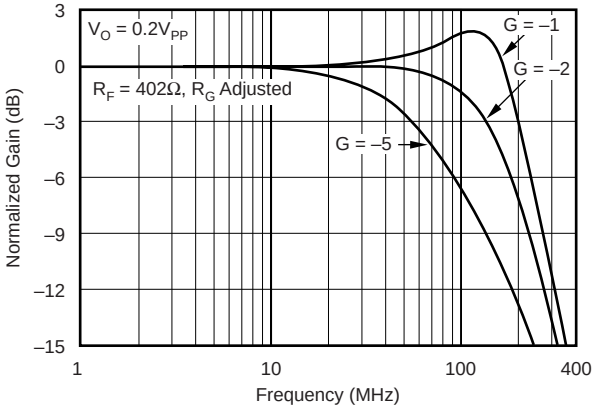
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω to V_{CM} = +2.5V, V_L = V_{CM} – 1.2V, V_H = V_{CM} + 1.2V, unless otherwise noted.

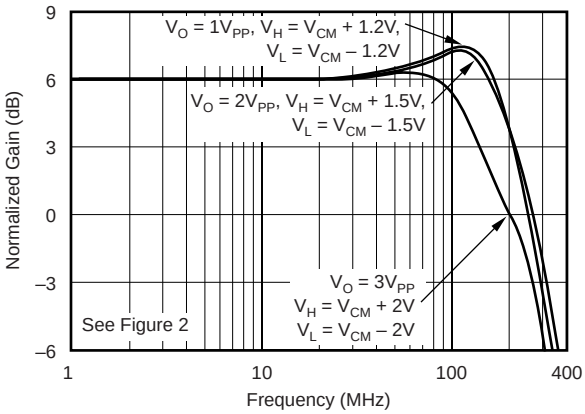
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



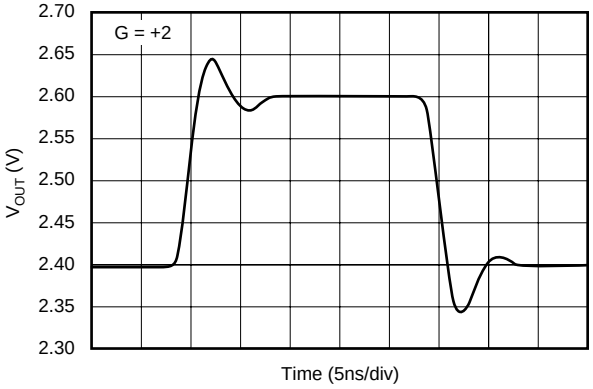
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



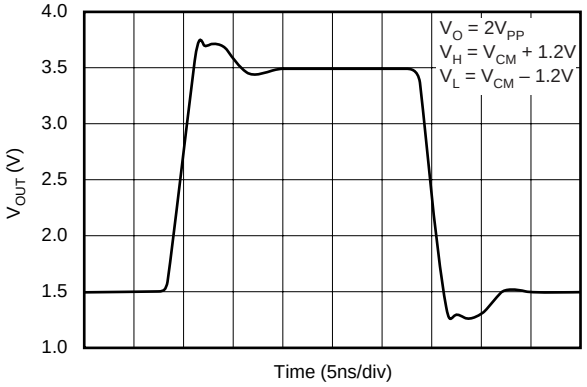
LARGE-SIGNAL FREQUENCY RESPONSE



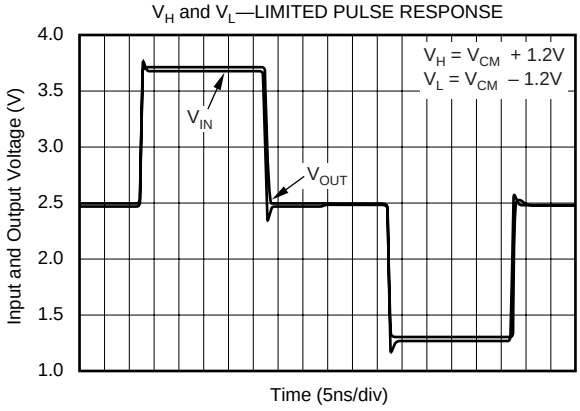
SMALL-SIGNAL PULSE RESPONSE



LARGE-SIGNAL PULSE RESPONSE



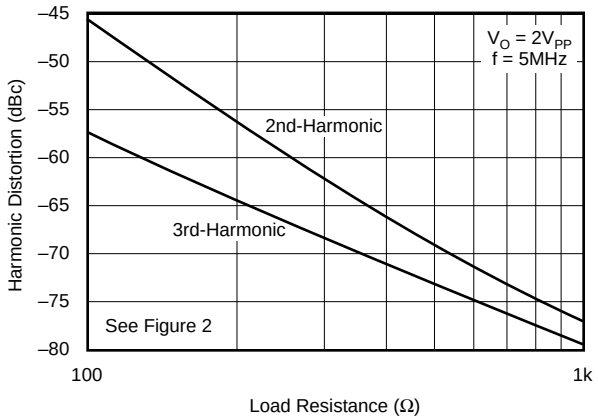
V_H and V_L—LIMITED PULSE RESPONSE



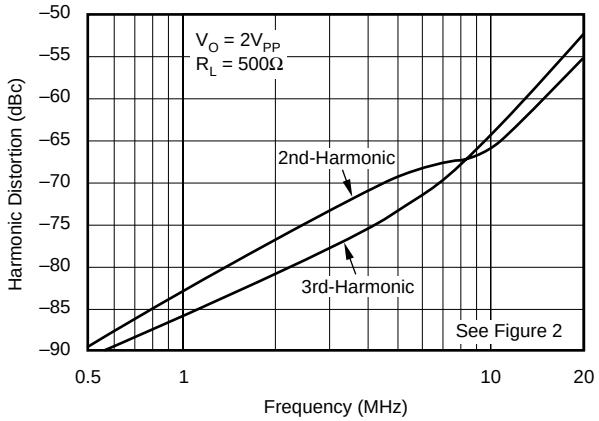
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 500Ω to V_{CM} = +2.5V, V_L = V_{CM} – 1.2V, V_H = V_{CM} + 1.2V, unless otherwise noted.

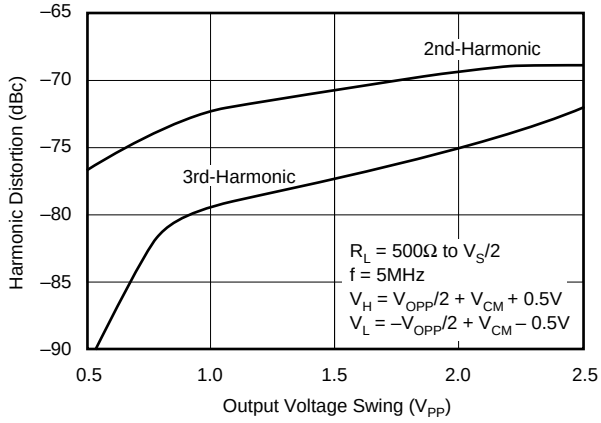
HARMONIC DISTORTION vs LOAD RESISTANCE



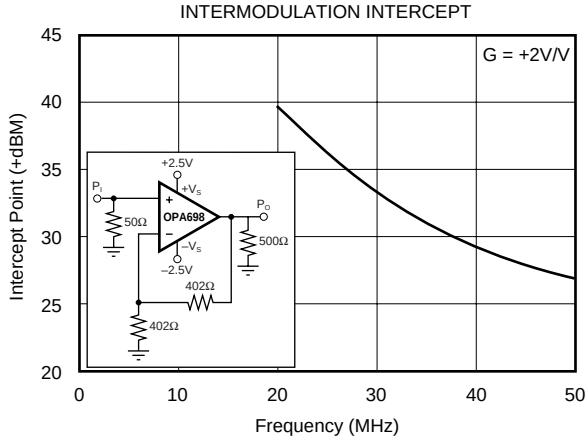
HARMONIC DISTORTION vs FREQUENCY



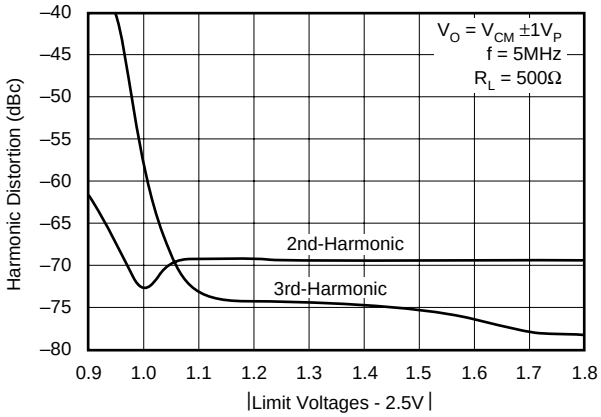
HARMONIC DISTORTION vs OUTPUT VOLTAGE



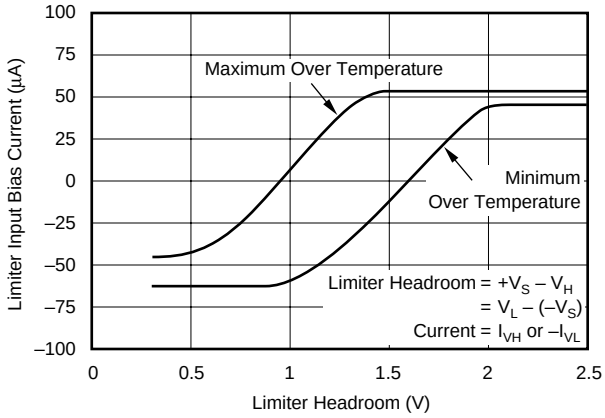
2-TONE, 3RD-ORDER
INTERMODULATION INTERCEPT



HARMONIC DISTORTION NEAR LIMITING VOLTAGES



LIMITER INPUT BIAS CURRENT vs BIAS VOLTAGE



TYPICAL APPLICATIONS

WIDEBAND VOLTAGE LIMITING OPERATION

The OPA698 is a voltage feedback amplifier that combines features of a wideband, high slew rate amplifier with output voltage limiters. Its output can swing up to 1V from each rail and can deliver up to 120mA. These capabilities make it an ideal interface to drive ADC while adding overdrive protection for the ADC inputs.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 500Ω. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 1, the total output load will be 500Ω || 804Ω = 308Ω. The voltage limiting pins are set to ±2V through a voltage divider network between the +Vs and ground for V_H, and between –Vs and ground for V_L. These limiter voltages are adequately bypassed with a 0.1µF ceramic capacitor to ground. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. One additional component is included in Figure 1. An additional resistor (174Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current-canceling resistance that matches the 200Ω source resistance seen at the inverting input (see the DC accuracy and offset control section). The power-supply bypass for each supply consists of two capacitors: one electrolytic 2.2µF and one ceramic 0.1µF. The power-supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. An additional 0.01µF power-supply decoupling capacitor (not shown here) can be included between the two power-supply pins. In practical PC board layouts, this optional-added capacitor will typically improve the 2nd harmonic distortion performance by 3dB to 6dB.

SINGLE-SUPPLY, NONINVERTING AMPLIFIER

Figure 2 shows an AC-coupled, noninverting gain amplifier for single +5V supply operation. This circuit was used for AC characterization of the OPA698, with a 50Ω source (which it matches) and a 500Ω load. The mid-point reference on the noninverting input is set by two 806Ω resistors. This gives an input bias current-canceling resistance that matches the 402Ω DC source resistance seen at the inverting input (see the DC accuracy and offset control section). The power-supply bypass for the supply consists of two capacitors: one electrolytic 2.2µF and one ceramic 0.1µF. The power-supply bypass capacitors are shown explicitly in Figures 1 and 2, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and the respective bias currents (I_{VH} and I_{VL}) have the polarities shown. These limiter voltages are adequately bypassed with a 0.1µF ceramic capacitor to ground. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground. While this circuit shows +5V operation, the same circuit may be used for single supplies up to +12V.

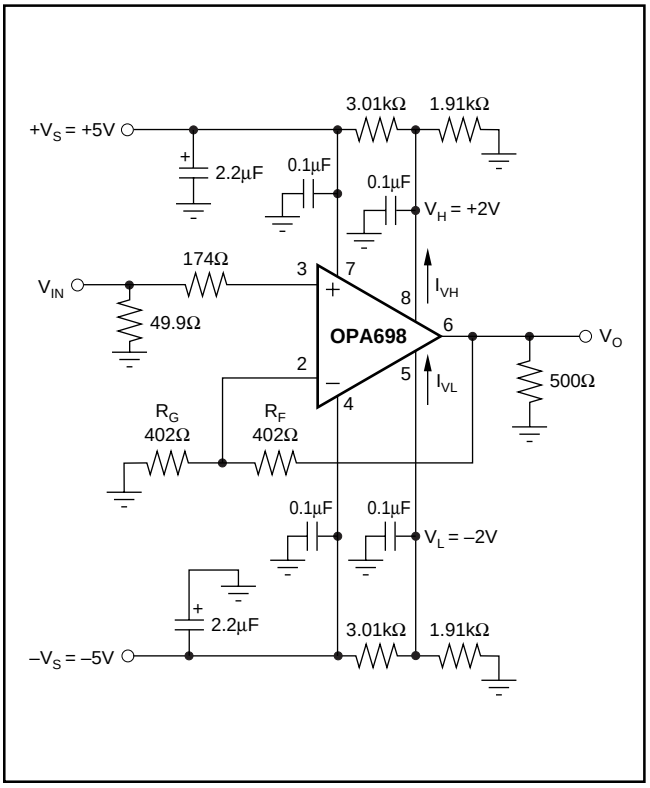


FIGURE 1. DC-Coupled, Dual-Supply Amplifier.

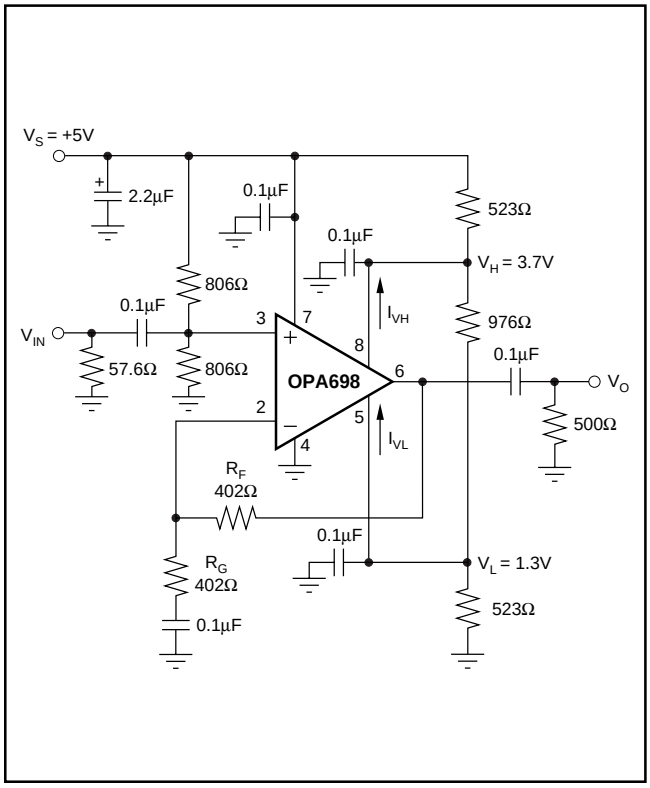


FIGURE 2. AC-Coupled, Single-Supply Amplifier.

WIDEBAND INVERTING OPERATION

Operating the OPA698 as an inverting amplifier has several benefits and is particularly useful when a matched 50Ω source and input impedance are required. Figure 3 shows the inverting gain of –2 circuit used as the basis of the inverting mode typical characteristics.

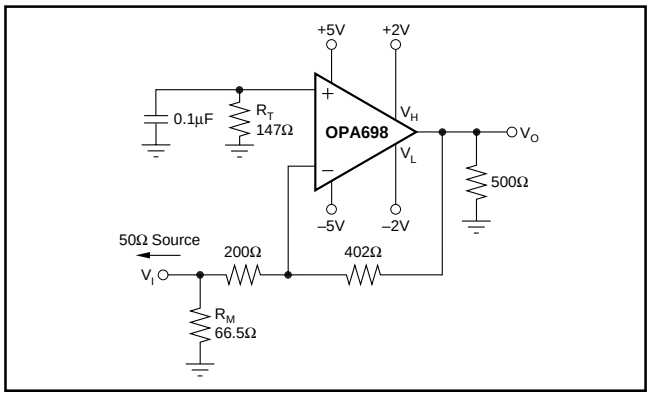


FIGURE 3. Inverting G = –2 Specifications and Test Circuit.

In the inverting case, only the feedback resistor appears as part of the total output load in parallel with the actual load. For a 500Ω load used in the typical characteristics, this gives a total load of 222Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case, 200Ω for a gain of –2) while an additional input resistor (R_M) can be used to set the total input impedance equal to the source, if desired. In this case, R_M = 66.5Ω in parallel with the 200Ω gain setting resistor gives a matched input impedance of 50Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 3.

For bias current-cancellation matching, the noninverting input requires a 147Ω resistor to ground. The calculation for this resistor includes a DC-coupled 50Ω source impedance along with R_G and R_M. Although this resistor will provide cancellation for the bias current, it must be well-decoupled (0.1µF in Figure 3) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50Ω at higher gains, the bandwidth for the circuit in Figure 3 will far exceed the bandwidth at that same gain magnitude for the noninverting circuit of Figure 1. This occurs due to the lower noise gain for the circuit of Figure 3 when the 50Ω source impedance is included in the analysis. For instance, at a signal gain of –8 (R_G = 50Ω, R_M = open, R_F = 402Ω) the noise gain for the circuit of Figure 3 will be 1 + 402Ω/(50Ω + 50Ω) = 5 due to the addition of the 50Ω source in the noise gain equation. This approach gives considerably higher bandwidth than the noninverting gain of +8. Using the 250MHz gain bandwidth product for the OPA698, an inverting gain of –8 from a 50Ω source to a 50Ω R_G will give 52MHz bandwidth, whereas the noninverting gain of +8 will give 28MHz, as shown in Figure 4.

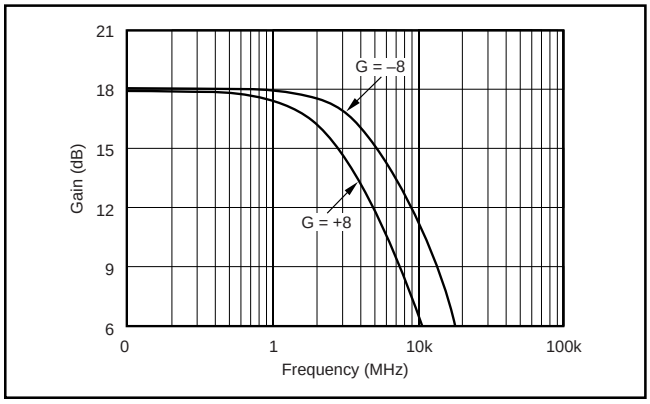


FIGURE 4. G = +8 and –8 Frequency Response.

LIMITED OUTPUT, ADC INPUT DRIVER

Figure 5 shows a simple ADC driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive. Note that the limiting voltages have been set 100mV above/below the corresponding reference voltage from the converter.

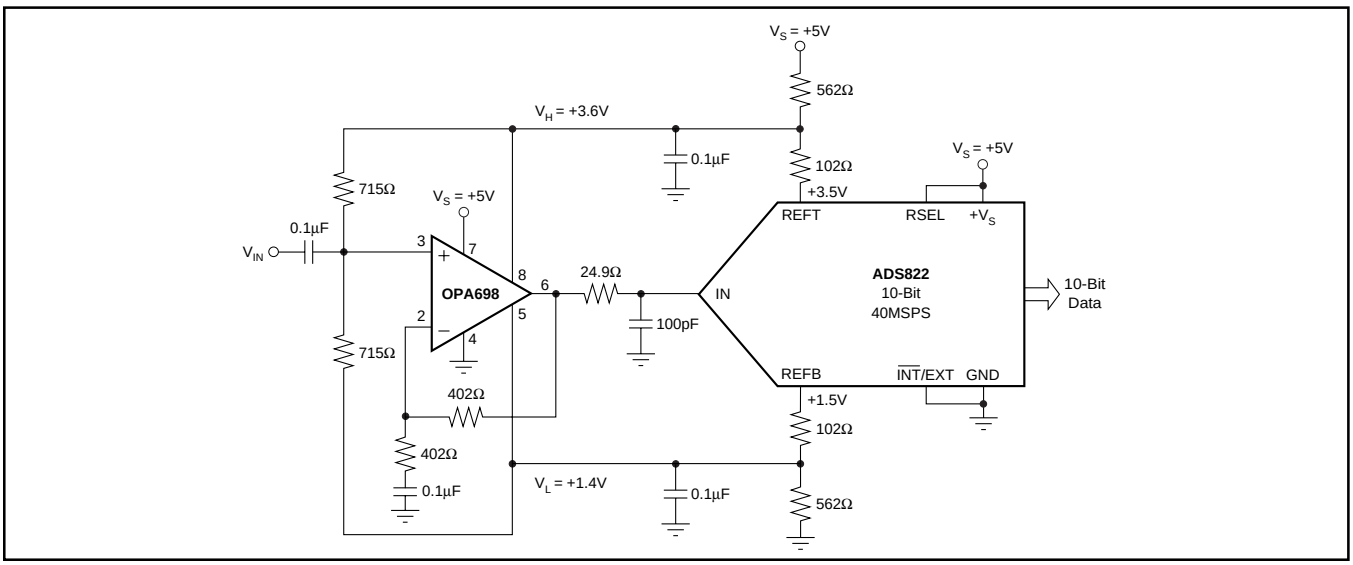


FIGURE 5. Single Supply, Limiting ADC Input Driver.

LIMITED OUTPUT, DIFFERENTIAL ADC INPUT DRIVER

Figure 6 shows a differential ADC driver that takes advantage of the OPA698 limiters to protect the input of the ADC.

Two OPA698s are used. The first one is an inverting configuration at a gain of –2. The second one is in a noninverting configuration at a gain of +2. Each amplifier is swinging $2V_{PP}$ providing a $4V_{PP}$ differential signal to drive the input of the ADC. Limiters have been set 100mV away from the magnitude of each amplifier's maximum signal to provide input protection for the ADC while maintaining an acceptable distortion level.

PRECISION HALF WAVE RECTIFIER

Figure 7 shows a half wave rectifier with outstanding precision and speed. V_H (pin 8) will default to a voltage between 3.1V and 3.8V if left open, while the negative limit is set to ground.

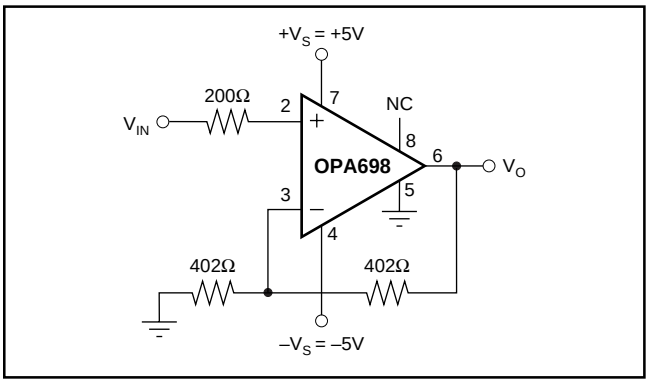


FIGURE 7. Precision Half Wave Rectifier.

The gain for the circuit in Figure 5 is set at +2. Figure 8 shows a 100MHz sinewave amplifier, with a gain of +2 and rectified.

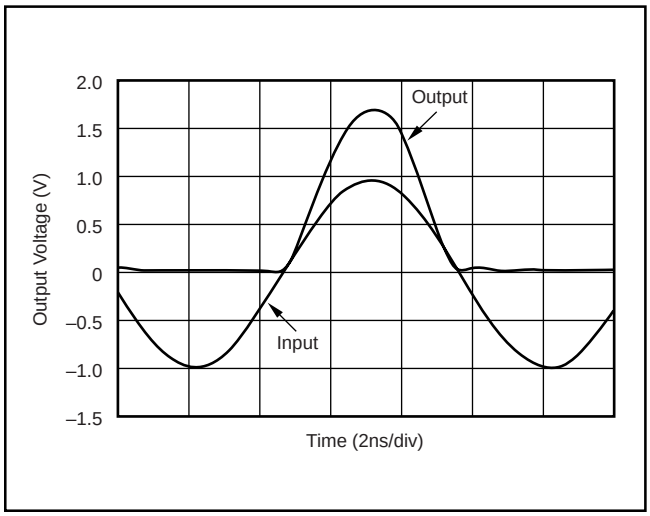


FIGURE 8. 100MHz Sinewave Rectified.

HIGH-SPEED FULL WAVE RECTIFIER

There are two methods shown here to build a high-speed full wave rectifier with a limiting amplifier: use the half-wave rectifier described previously with another amplifier to obtain the full wave rectified, or use the input to set the limiting voltage.

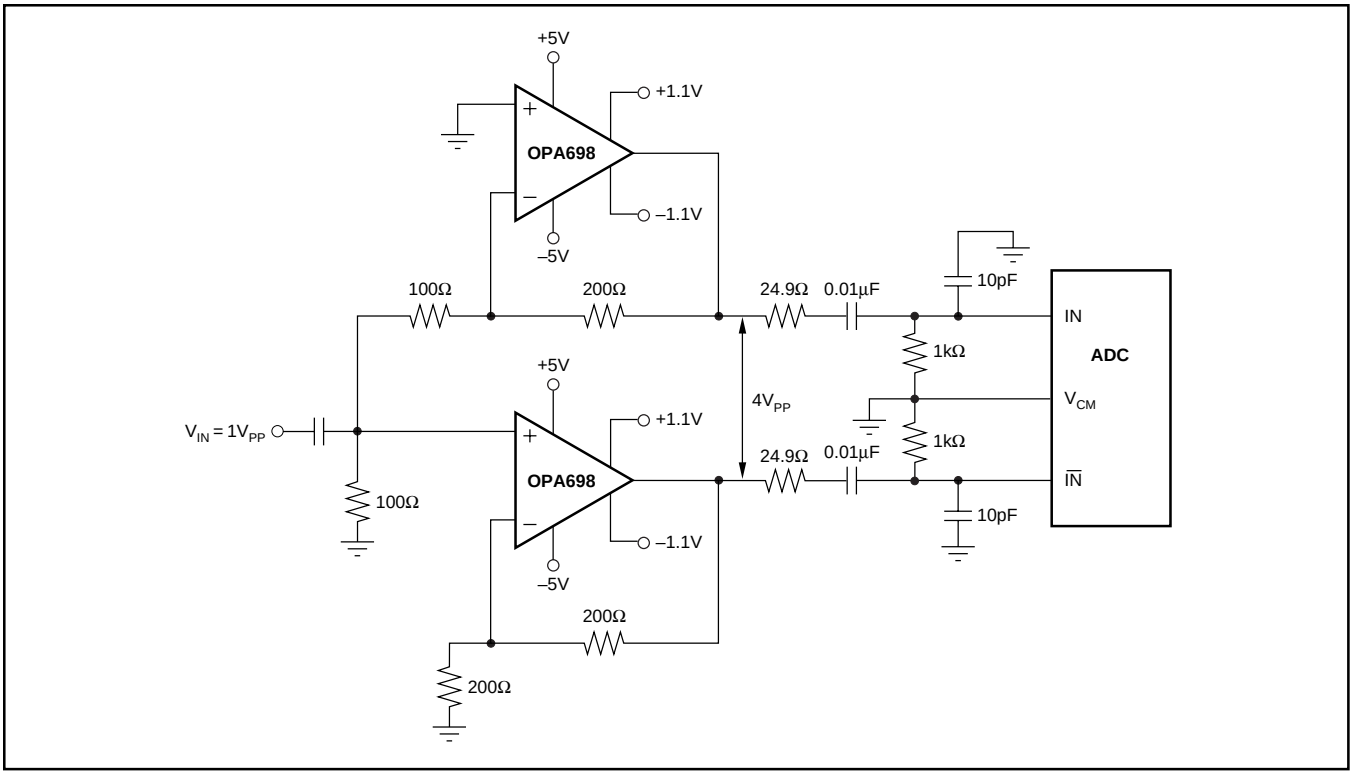


FIGURE 6. Single to Differential AC-Coupled, Output Limited ADC Driver.

High-Speed Full Wave rectifier #1

The circuit shown in Figure 9 uses only one amplifier, in an inverting gain of –1 configuration. The upper limiting voltage is left open, resulting in an upper limiting voltage of +3.5V. The lower limiting voltage is connected to the input signal, resulting in the following behavior. When the input voltage is negative, the amplifier is not limiting, resulting in the inversion of the input sinewave to the output. During the positive excursion of the input signal, the output signal is being driven by the limiting input pin. Since the output is driven from the limiter input pin from positive inputs, the lower slew rate in the input path restricts the application of this approach to lower amplitude and/or frequencies. A 2MHz fully rectified sinewave is shown in Figure 10.

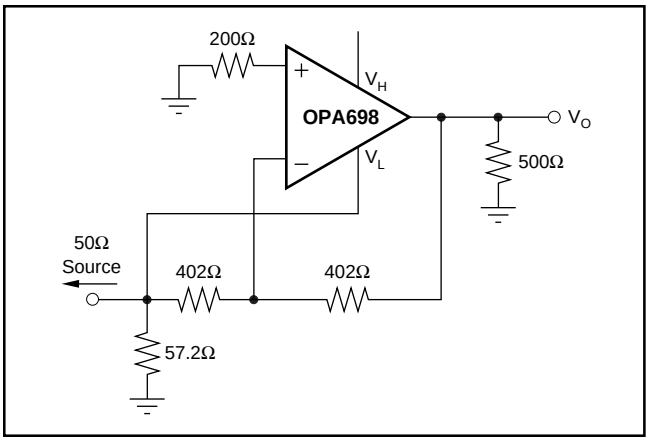


FIGURE 9. High-Speed Full Wave Rectifier #1.

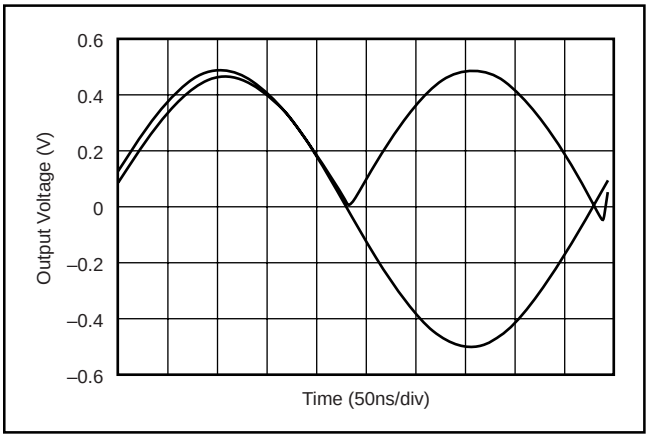


FIGURE 10. 2MHz Sinewave Rectified.

In order to reach higher frequencies, a second method is recommended.

High Speed Full Wave rectifier #2

The circuit shown in Figure 11 combines a half-wave rectifier driving the OPA693 in an inverting configuration, while the input signal drives the noninverting input of the fixed gain amplifier OPA693, resulting in a full wave rectifier function. Results are shown in Figure 12.

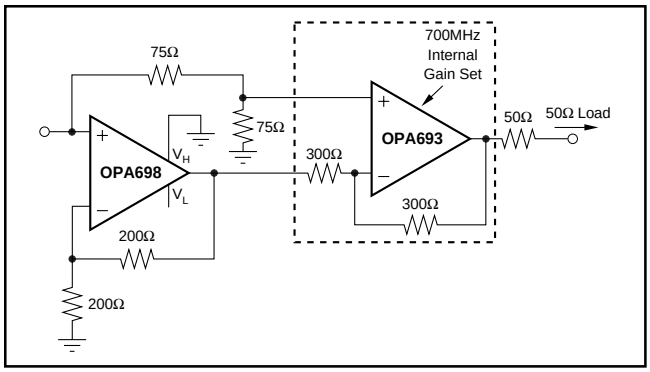


FIGURE 11. High-Speed Full Wave Rectifier #2.

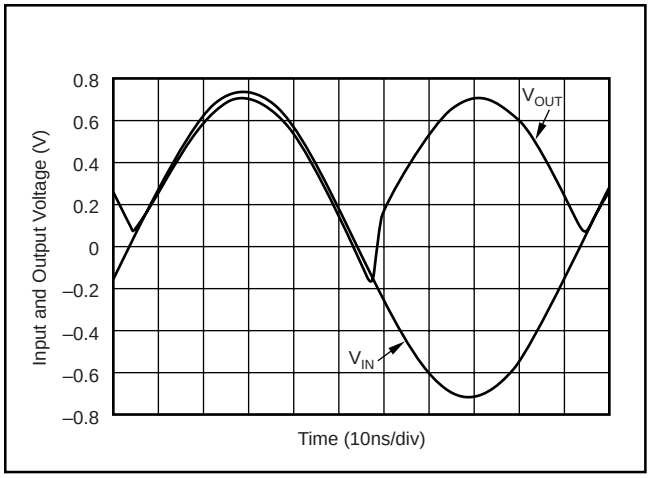


FIGURE 12. 10MHz Sinewave Rectified.

If the negative excursion of the rectified signal is not desired, it can easily be removed by replacing the OPA693 with the OPA698 configured as a difference amplifier with V_L connected to ground and V_H left floating.

SOFT-CLIPPING (Compression) CIRCUIT

Figure 13 shows a soft-clipping circuit. As soon as the input voltage exceeds either V_{CH} or V_{CL}, the limiting voltages are driven by the following equations:

$$V_H = V_H = \frac{R_2 \times V_{CH} + R_1 \times V_{IN}}{R_1 + R_2} \quad (1)$$

$$V_L = \frac{R_4 \times V_{CL} + R_3 \times V_{IN}}{R_3 + R_4} \quad (2)$$

As the amplifier is operating in the limiting mode, the output voltage is compressed with a gain of R_1+R_2/R_1 for the positive excursion above V_{CH}, and by a gain of R_3+R_4/R_3 for the negative excursion below V_{CL}. Figure 14 shows a $5V_{PP}$ on the input being compressed above ±1V with a compression gain of one-third.

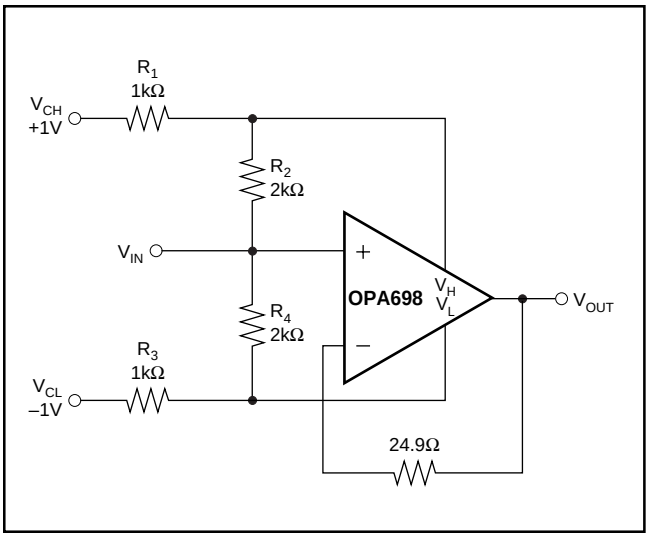


FIGURE 13. Soft-Clipping Circuit.

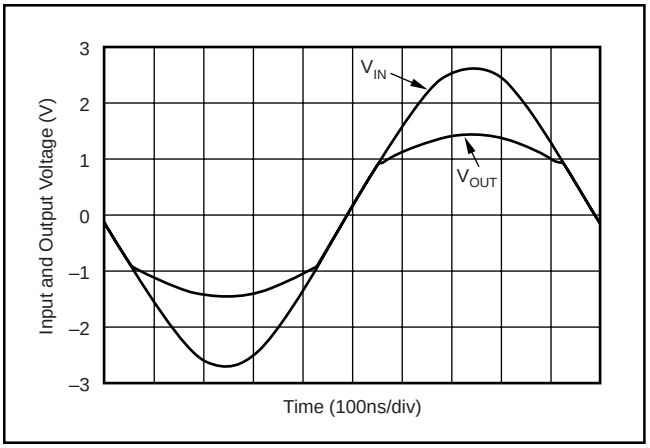


FIGURE 14. Soft Clipping with a Gain of 1/3 above the clamp level (±1V).

VERY HIGH-SPEED SCHMITT TRIGGER

Figure 15 shows a very high-speed Schmitt Trigger. The output levels are precisely defined, and the switching time is exceptional. The output voltage swings between V_H and V_L.

The circuit operates as follow. When the input voltage is less than V_{HL} then the output is limiting at V_H. When the input is greater than V_{HH} then the output is limiting at V_L, with V_{HL} and V_{HH} defined as the following:

$$V_{HL,\,HH} = \frac{R_1 \,||\, R_2 \,||\, R_3}{R_1} \times V_{REF} + \frac{R_1 \,||\, R_2 \,||\, R_3}{R_2} \times V_{OUT}$$

Due to the inverting function realized by the Schmitt Trigger, V_{HL} corresponds to $V_{OUT} = V_H$, and V_{HH} corresponds to $V_{OUT} = V_L$.

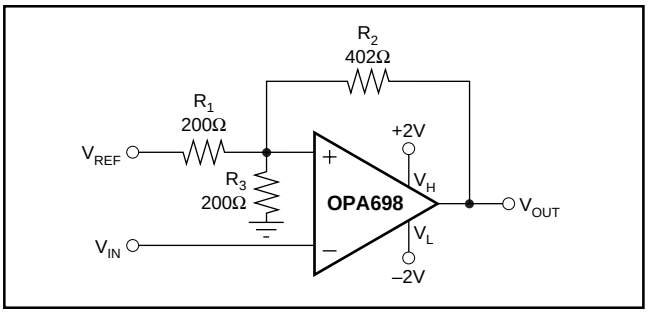


FIGURE 15. Very High-Speed Schmitt Trigger.

Figure 16 shows the Schmitt Trigger operating with V_{REF} = +5V. This gives us V_{HH} = 2.4V and V_{HL} = 1.6V. The propagation delay for the OPA698 in a Schmitt Trigger configuration is 6ns from high-to-low, and 5ns from low-to-high.

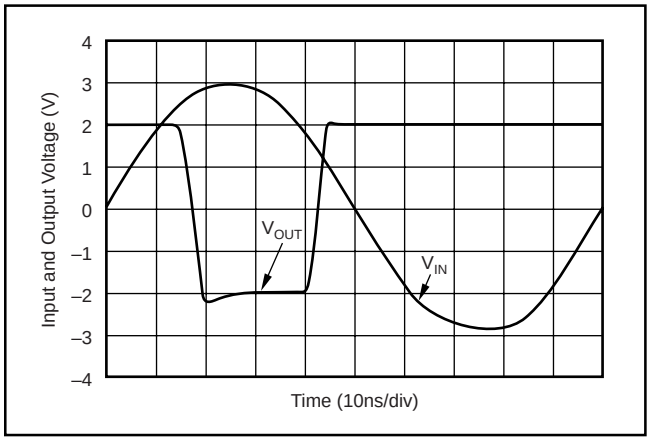


FIGURE 16. Schmitt Trigger Time Domain Response for a 10MHz Sinewave.

UNITY-GAIN BUFFER

Figure 17 shows a unity-gain voltage buffer using the OPA698. The feedback resistor (R_F) isolates the output from the input capacitance at the inverting input. R_F = 24.9Ω is recommended for unity-gain buffer applications. R_C is an optional compensation resistor that reduces the peaking typically seen at G = +1. Choosing $R_C = R_S + R_F$ gives a unity-gain buffer with approximately the G = +2 frequency response. The frequency response for this circuit is shown in the electrical characteristics curves.

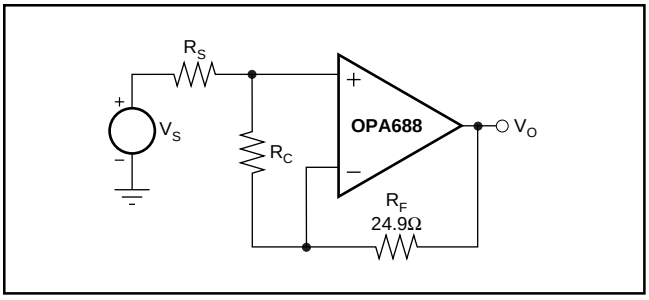


FIGURE 17. Unity-Gain Buffer.

DC RESTORER

Figure 18 shows a DC restore circuit using the OPA698 and OPA660. The buffer element of the OPA660 is used to buffer the input signal while the transconductance element is used to restore the DC level after the decoupling capacitor C_1. The DC level is set using R_1 and R_2. The OPA698 is configured at a gain of 2 to compensate for the 75Ω series into a 75Ω load. The OPA698 also limits the output to ground.

VIDEO SYNC STRIPPER

Figure 19 shows a sync stripper using two OPA698 output-limiting op amps. One OPA698 is configured as a limiting inverting comparator. Referred to the input, the negative excursions lower than –0.2V are clipped to ground, and all excursions greater than –0.2V generate an output voltage set by the default limiting value (–3.5V). The second OPA698 is using this waveform to effectively remove the sync pulse from the video signal.

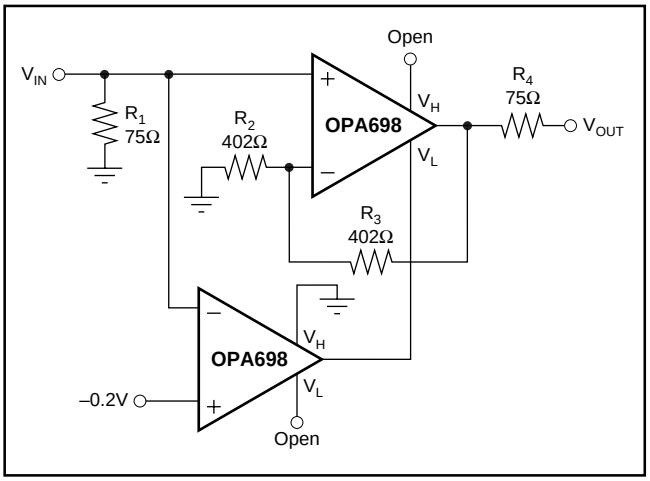


FIGURE 19. Sync Stripper Circuit.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURE

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA698. The fixture is offered free of charge as an unpopulated PCB, delivered with user's guide. The summary information for this fixture is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA698ID	SO-8	DEM-OPA-SO-1A	SBOU009

TABLE I. Demonstration Fixture.

This demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA698 product folder.

OPERATING SUGGESTIONS

THEORY OF OPERATION

The OPA698 is a voltage-feedback op amp that is unity-gain stable. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This action from the limiters avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain. The limiters have a very sharp transition from the linear region of operation to output limiting. This transition allows the limiter voltages to be set very near (< 100mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

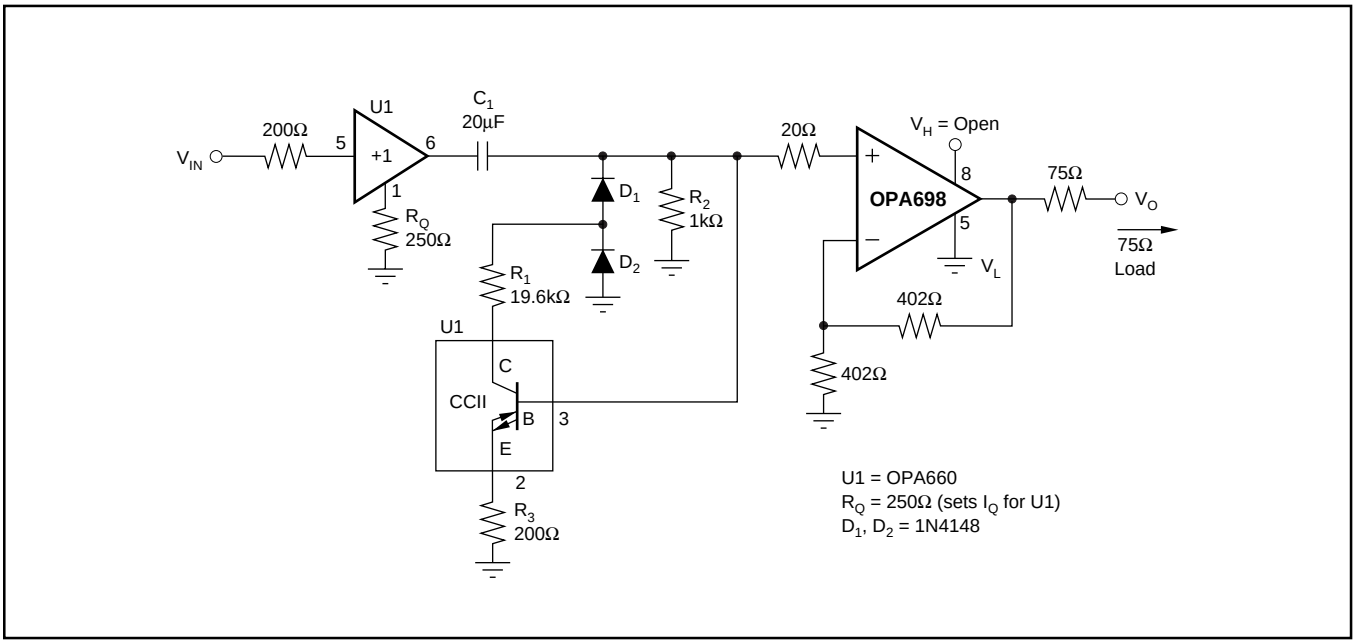


FIGURE 18. DC Restore to Ground.

OUTPUT LIMITERS

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L. Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is very sharp—the desired output signal can safely come to within 30mV of V_H or V_L with no onset of non-linearity. The limiter voltages can be set to within 0.7V of the supplies ($V_L \geq -V_S + 0.7V$, $V_H \leq +V_S - 0.7V$). They must also be at least 400mV apart ($V_H - V_L \geq 0.4V$). When pins 5 and 8 are left open, V_H and V_L go to the default voltage limit; the minimum values are given in the electrical specifications. Looking at Figure 20 for the zero bias current case shows the expected range of (V_S – default limit voltages) = headroom.

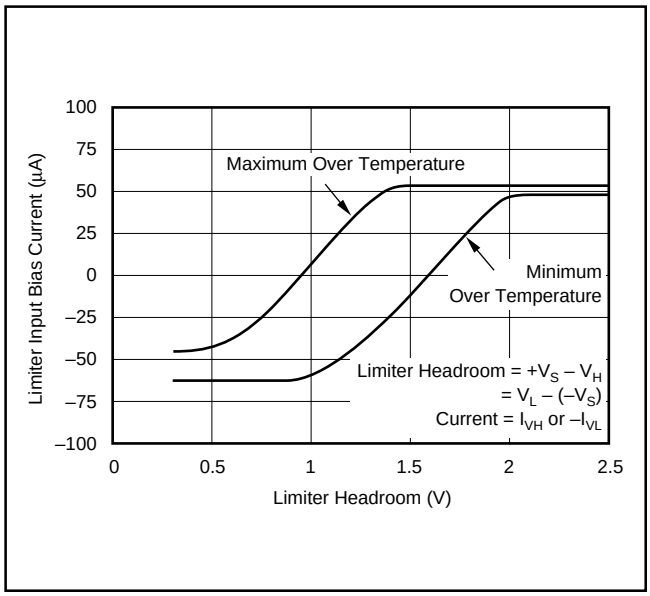


FIGURE 20. Limiter Bias Current vs Bias Voltage.

When the limiter voltages are more than 2.1V from the supplies ($V_L \geq -V_S + 2.1V$ or $V_H \leq +V_S - 2.1V$), you can use simple resistor dividers to set V_H and V_L (see Figure 1). Make sure to include the limiter input bias currents (Figure 8) in the calculations (that is, $I_{VL} = -50\mu A$ out of pin 5, and $I_{VH} = +50\mu A$ out of pin 8). For good limiter voltage accuracy, run at least 1mA quiescent bias current through these resistors. When the limiter voltages need to be within 2.1V of the supplies ($V_L \leq -V_S + 2.1V$ or $V_H \geq +V_S - 2.1V$), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This condition will typically be the case for single-supply operation ($V_S = +5V$). Figure 2 runs 2.5mA through the resistive divider that sets V_H and V_L. This limits errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages. The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (for example, ±5%). Using a more accurate source, and bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

  Other error sources also contribute, but should have little impact on the limiters' DC accuracy:
- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to uncertainty in the useable output swing.
- The limiter offset voltage only slightly degrades limiter accuracy. Figure 21 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages.

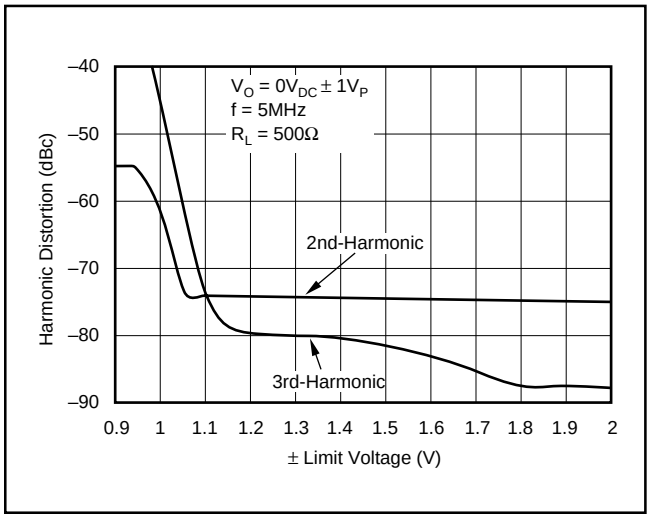


FIGURE 21. Harmonic Distortion Near Limit Voltages.

OUTPUT DRIVE

The OPA698 has been optimized to drive 500Ω loads, such as ADCs. It still performs very well driving 100Ω loads; the specifications are shown for the 500Ω load. This makes the OPA698 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve *Output Impedance vs Frequency*, the OPA698 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

THERMAL CONSIDERATIONS

The OPA698 will not require heat sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that determines internal power dissipation.

The operating junction temperature is: $T_J = T_A + P_D \times \theta_{JA}$, where T_A is the ambient temperature. For example, the maximum T_J for a OPA698ID with G = +2, $R_F = 402\Omega$, $R_L = 100\Omega$, and $\pm V_S = \pm 5V$ at the maximum $T_A = +85°C$ is calculated as:

$$P_{DQ} = (10V \times 15.5mA) = 155mW$$

$$P_{DL} = \frac{(5V)^2}{4 \times (100\Omega \parallel 804\Omega)} = 70mW$$

$$P_D = 155mW + 70mW = 225mW$$

$$T_J = 85°C + 225mW \times 125°C/W = 113°C$$

This would be the maximum T_J from $V_O = \pm 2.5V_{DC}$. Most applications will be at a lower output stage power and have a lower T_J.

CAPACITIVE LOADS

Capacitive loads, such as the input to ADCs, will decrease the amplifier phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads ≥ 2pF should be isolated by connecting a small resistor in series with the output, as shown in Figure 22. Increasing the gain from +2 will improve the capacitive drive capabilities due to increased phase margin.

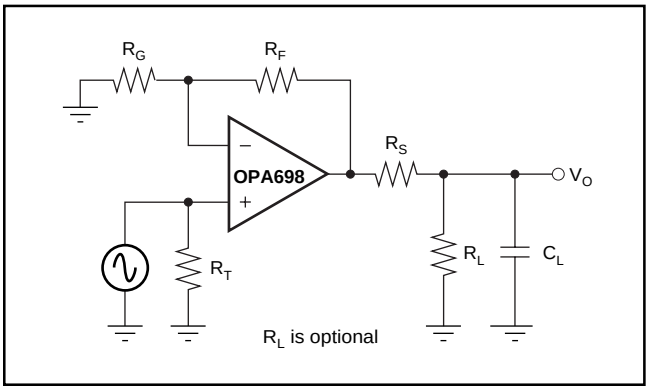


FIGURE 22. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

FREQUENCY RESPONSE COMPENSATION

The OPA698 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of +2. Phase margin and peaking improve at higher gains. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes (that is, noise gain = 2). Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps, or use the high-gain optimized OPA699.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high-gain applications, use a three-resistor *Tee* network to reduce the RC time constants set by the parasitic capacitances. Be careful not to increase the noise generated by this feedback network too much.

PULSE SETTLING TIME

The OPA698 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve *R_S vs Capacitive Load*. Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics, when recovering from overdrive, are very good.

DISTORTION

The OPA698 distortion performance is specified for a 500Ω load, such as an ADC. Driving loads with smaller resistance will increase the distortion, as illustrated in Figure 23. Remember to include the feedback network in the load resistance calculations.

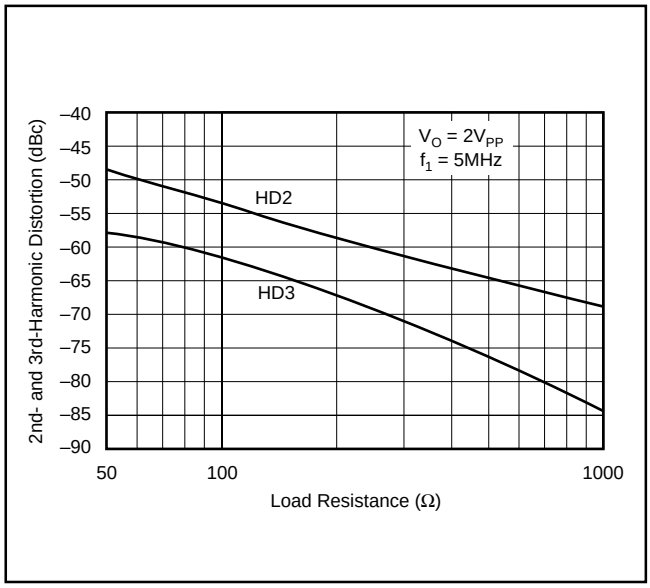


FIGURE 23. 5MHz Harmonic Distortion vs Load Resistance.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 5.6nV/$\sqrt{Hz}$ input voltage noise for the OPA698, however, is much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 24 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

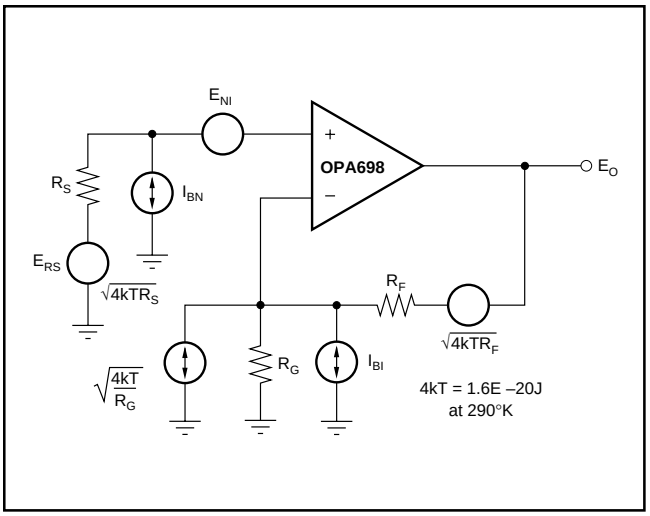


FIGURE 24. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms shown in Figure 25.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (3)$$

Dividing this expression by the noise gain (NG = (1+R_F/R_G)) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 4.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (4)$$

Evaluating these two equations for the OPA698 circuit and component values (see Figure 1) will give a total output spot noise voltage of 11.9nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 6nV/$\sqrt{Hz}$. This total input-referred spot noise voltage is only slightly higher than the 5.6nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to a maximum value of 300Ω. Keeping both (R_F || R_G) and the noninverting input source impedance less than 300Ω will satisfy both noise and frequency response flatness considerations. Since the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_T) for the inverting op amp configuration of Figure 3 is not required, but is still desirable.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage feedback op amp allows good output DC accuracy in a large variety of applications. The power-supply current trim for the OPA698 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically ±8µA at each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. The total output offset voltage may be considerably reduced by matching the DC source resistances appearing at the two inputs. This reduces the output DC error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to: –(NG = noninverting signal gain)

$\pm(NG \bullet V_{OS(MAX)}) \pm (R_F \bullet I_{OS(MAX)})$

$= \pm(2 \bullet 5mV) \pm (402\Omega \bullet 1.4\mu A)$

$= \pm 10.6mV$

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques eventually reduce to adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the DC offset voltage on the summing junction will set up a DC current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 25 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the DC offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain as well as the frequency response.

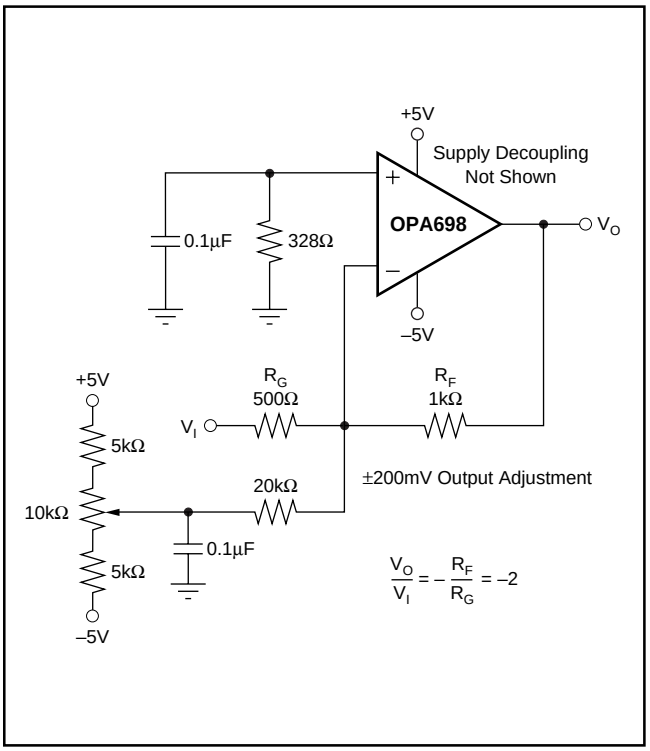


FIGURE 25. DC-Coupled, Inverting Gain of –2, with Offset Adjustment.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with the high-frequency OPA698 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

a) **Minimize parasitic capacitance to any AC ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.

b) **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high frequency 0.1µF decoupling capacitors < 0.2" away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2µF to 6.8µF) high-frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.

c) **Place external components close** to the OPA698. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.

d) **Use high-frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances. Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use R_F type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2µF to 6.8µF) should be tantalum for better high frequency and pulse performance.

e) **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2pF parasitic parallel capacitance. For resistors > 1.5kΩ, this adds a pole and/or zero below 500MHz. Make sure that the output loading is not too heavy. The recommended 402Ω feedback resistor is a good starting point in most designs.

f) **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve, *R_S vs Capacitive Load*. Parasitic loads < 2pF may not need the isolation resistor.

g) **When long traces are necessary,** use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the source from the reactive load presented by the line, but the frequency response will be degraded. Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.

h) **Do not use sockets** for high-speed parts like the OPA698. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

POWER SUPPLIES

The OPA698 is nominally specified for operation using either ±5V supplies or a single +5V supply. The maximum specified total supply voltage of 12V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common-mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single-supply operation circuits. Figure 2 shows one approach to single-supply operation.

INPUT AND ESD PROTECTION

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for very high-speed, fine geometry processes. ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA698.

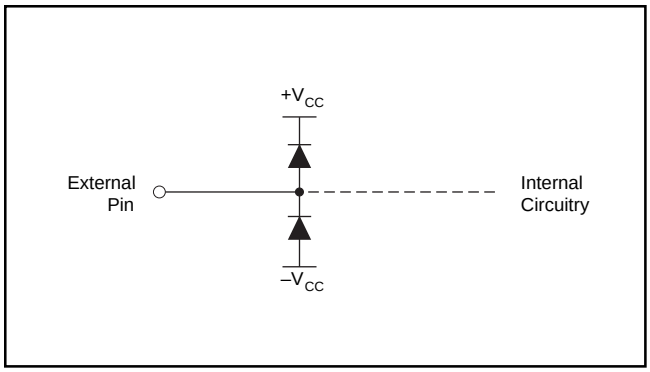


FIGURE 26. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
12/08	D	2	Absolute Maximum Ratings	Changed minimum Storage Temperature Range from –40°C to –65°C.
3/06	C	20	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA698ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA698IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA698IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA698IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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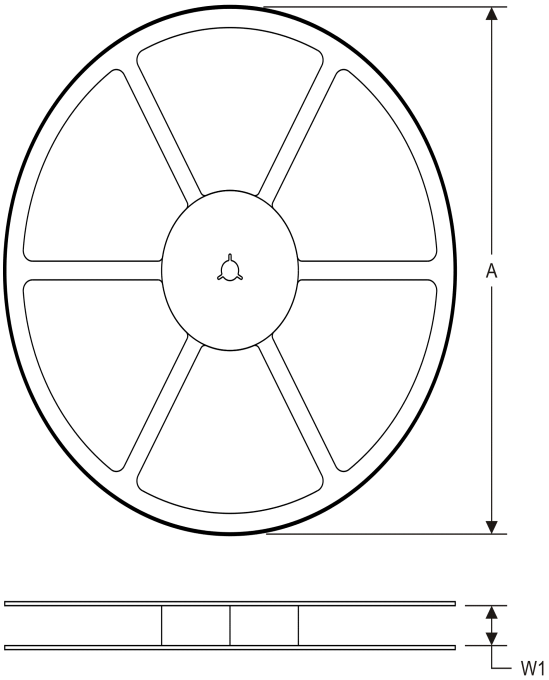
OTHER QUALIFIED VERSIONS OF OPA698 :
- Military: OPA698M

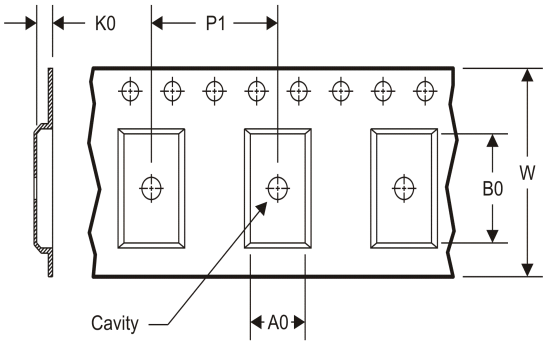
NOTE: Qualified Version Definitions:
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



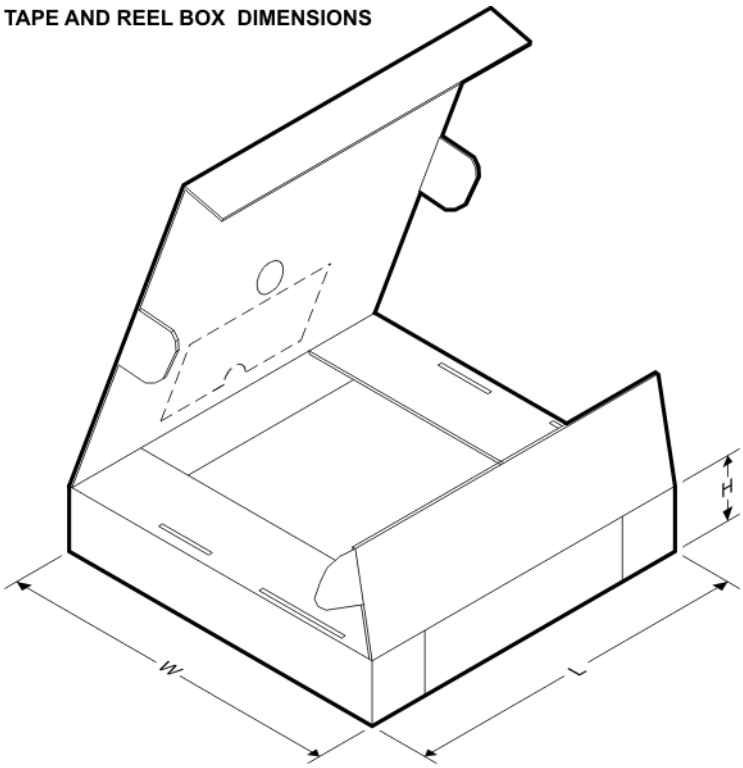
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA698IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

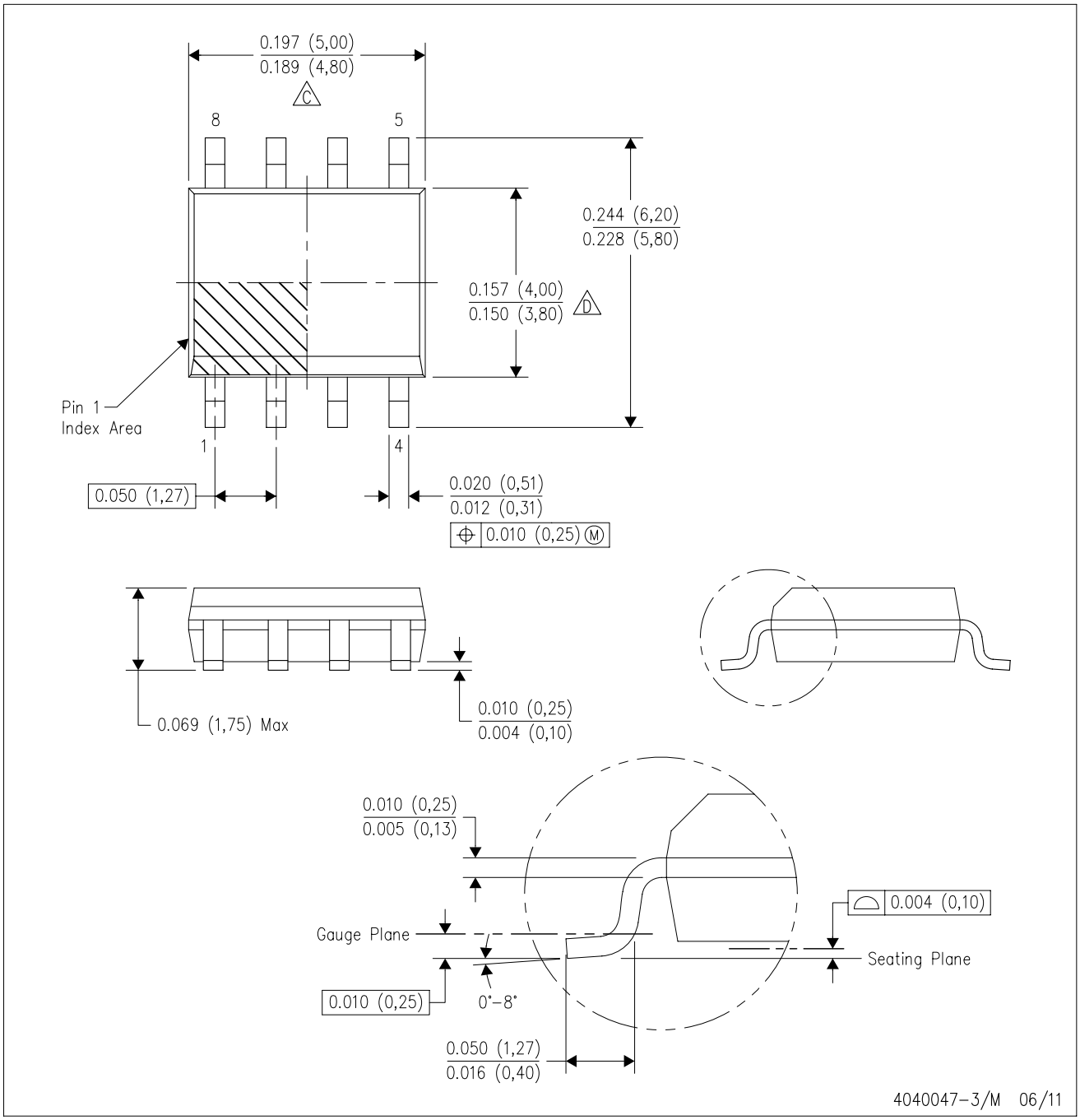
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

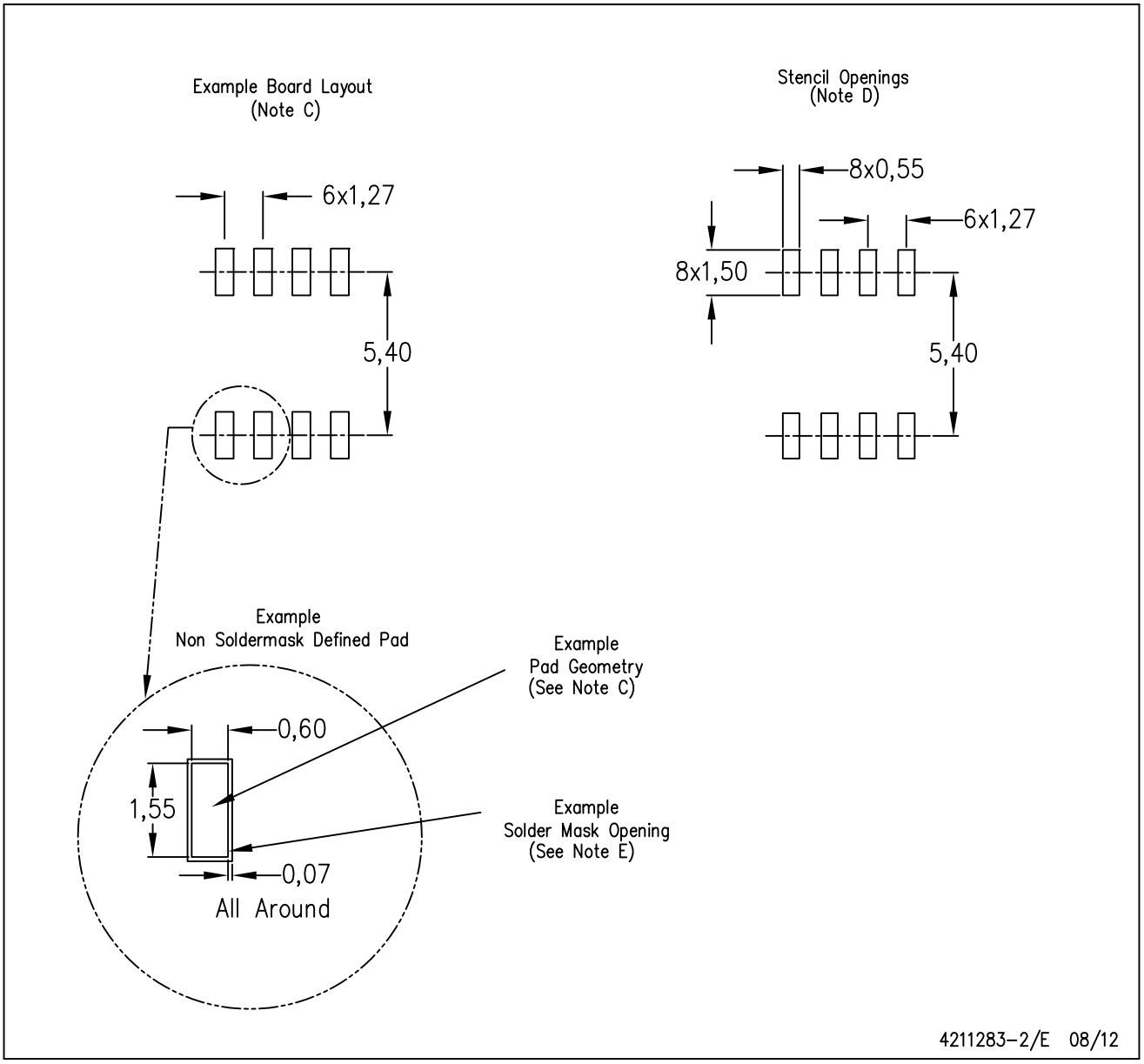
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA698IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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