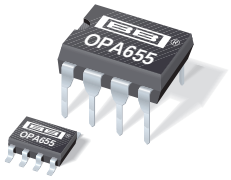
BURR - BROWN®



OPA655

Wideband, Unity Gain Stable, FET-Input OPERATIONAL AMPLIFIER

FEATURES

- 400MHz UNITY GAIN BANDWIDTH
- LOW INPUT BIAS CURRENT: 5pA
- HIGH INPUT IMPEDANCE: $10^{12}\Omega$ || 1.0pF
- ULTRA-LOW dG/dP: 0.006%/0.009°
- LOW DISTORTION: 90dB SFDR at 5MHz
- FAST SETTLING: 17ns (0.01%)
- HIGH OUTPUT CURRENT: 60mA
- FAST OVERDRIVE RECOVERY

APPLICATIONS

- WIDEBAND PHOTODIODE AMPLIFIER
- PEAK DETECTOR
- CCD OUTPUT BUFFER
- ADC INPUT BUFFER
- HIGH SPEED INTEGRATOR
- TEST AND MEASUREMENT FRONT END

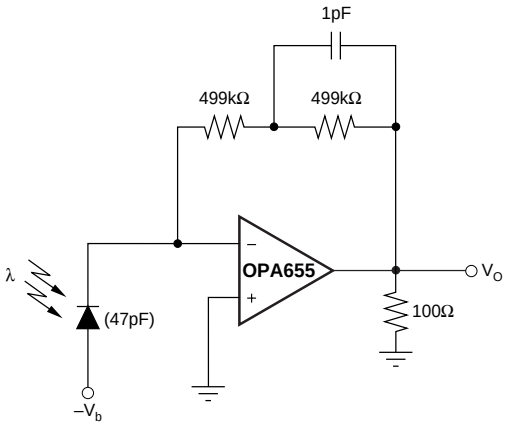
DESCRIPTION

The OPA655 combines a very wideband, unity gain stable, voltage feedback op amp with a FET input stage to offer an ultra high dynamic range amplifier for ADC buffering and transimpedance applications. Extremely low harmonic distortion along with excellent pulse settling characteristics will support even the most demanding ADC input buffer requirements.

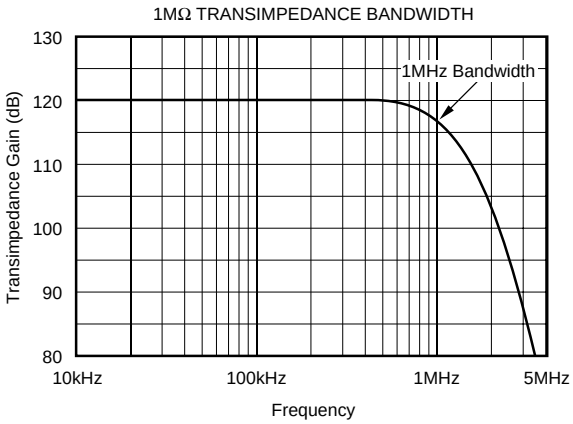
The broad unity gain stable bandwidth and FET input allows exceptional performance in high speed, low noise integrators.

The high input impedance and low bias current provided by the FET input is further supported by the ultra-low $6nV/\sqrt{Hz}$ input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

Broad transimpedance bandwidths are achievable given the OPA655's high 240MHz gain bandwidth product. As shown below, a –3dB bandwidth of 1MHz is provided even for a high 1MΩ transimpedance gain from a 47pF source capacitance.



Wideband Photodiode Transimpedance Amplifier



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SBOS048

SPECIFICATIONS

At T_A = +25°C, V_S = ±5V, R_{FB} = 100Ω, and R_L = 100Ω, unless otherwise noted. R_{FB} = 0 for G = +1.

PARAMETER	CONDITIONS	OPA655P, U MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Closed-Loop Response	Gain = +1V/V, V_O = 200mVp-p		400		MHz
	Gain = +2V/V, V_O = 200mVp-p		185		MHz
	Gain = +5V/V, V_O = 200mVp-p		57		MHz
	Gain = +10V/V, V_O = 200mVp-p		24		MHz
Gain-Bandwidth Product			240		MHz
Slew Rate	G = +1, 1V Step	210	290		V/µs
Over Temperature		200			V/µs
Rise Time	0.2V Step		1		ns
Fall Time	0.2V Step		1		ns
Settling Time: 0.01%	G = +1, 1V Step		17		ns
0.1%	G = +1, 1V Step		8		ns
1%	G = +1, 1V Step		6		ns
Spurious-Free Dynamic Range	G = +1, f = 5MHz	75	90		dBc
	V_O = ±1V, R_L = 100Ω				
Differential Gain	3.58MHz, 0 to 1.4V, R_L = 150Ω		0.006		%
Differential Phase	3.58MHz, 0 to 1.4V, R_L = 150Ω		0.009		degrees
Bandwidth for 0.1dB flatness	G = +2, 2Vp-p		30		MHz
OFFSET VOLTAGE					
Input Offset Voltage			±1	±2	mV
Over Temperature			±10		µV/°C
Power Supply Rejection (+V_S)	$\|V_S\|$ = 4.50V to 5.50V	55	70		dB
(–V_S)		50	65		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		–5	–125	pA
Over Temperature	V_{CM} = 0V			–8.0	nA
Input Offset Current	V_{CM} = 0V		±2	±125	pA
Over Temperature	V_{CM} = 0V			±8	nA
NOISE					
Input Voltage Noise					
Noise Density: f = 100Hz			20		nV/√Hz
f = 1kHz			8		nV/√Hz
f = 10kHz			6		nV/√Hz
f = 0.1MHz to 100MHz			6		nV/√Hz
Integrated Voltage Noise, BW = 1MHz to 100MHz			60		µVrms
Input Bias Current Noise Current Noise Density, f = 10Hz to 10kHz			1.3	4	fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±2.75		V
Over Temperature		±2.5			V
Common-Mode Rejection	V_{CM} = ±0.5V	55	70		dB
INPUT IMPEDANCE					
Differential			10^{12} || 1.2		Ω || pF
Common-Mode			10^{12} || 1.0		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	53	58		dB
Over Temperature	V_O = ±2V, R_L = 100Ω	50			dB
OUTPUT					
Voltage Output	R_L = 100Ω, G = +1	±3.0	±3.4		V
Over Temperature		±2.8			V
Current Output		±35	±60		mA
Over Temperature		±28			mA
Short-Circuit Output Current			±140		mA
Output Resistance	0.1MHz, G = +1		0.04		Ω
POWER SUPPLY					
Specified Operating Voltage			±5		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.75		±5.25	V
Quiescent Current	T_{MIN} to T_{MAX}	±21	±25	±29	mA
Over Temperature				±31	mA
TEMPERATURE RANGE					
Specification: P, U		–40		+85	°C
Thermal Resistance, θ_{JA}					
P			100		°C/W
U			125		°C/W

NOTE: (1) Junction temperature ≈ +25°C for room temperature tested input bias and offset current.

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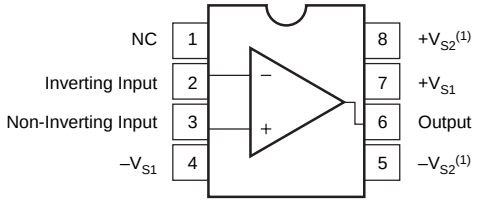
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage Across Device ($V_{S\ (TOTAL)}$)	11V
Internal Power Dissipation	See Thermal Considerations
Differential Input Voltage	$V_{S\ (TOTAL)}$
Common-Mode Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, U	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO-8, 3s)	+260°C
Junction Temperature (T_J)	+175°C

PIN CONFIGURATION

Top View **DIP/SO-8**



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of pins 4 and 7 only, will reduce the effective pin impedance and substantially improve distortion.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA655P	8-Pin Plastic DIP	006
OPA655U	SO-8	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
OPA655P	8-Pin Plastic DIP	–40°C to +85°C
OPA655U	SO-8	–40°C to +85°C

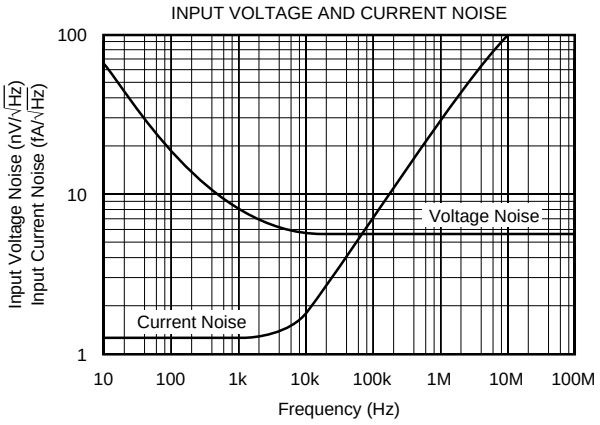
ELECTROSTATIC DISCHARGE SENSITIVITY

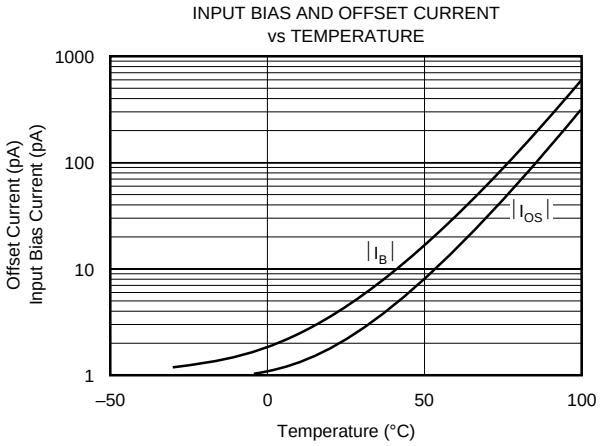
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

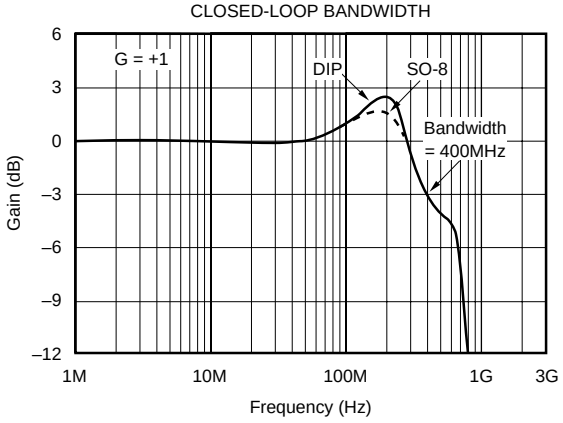
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

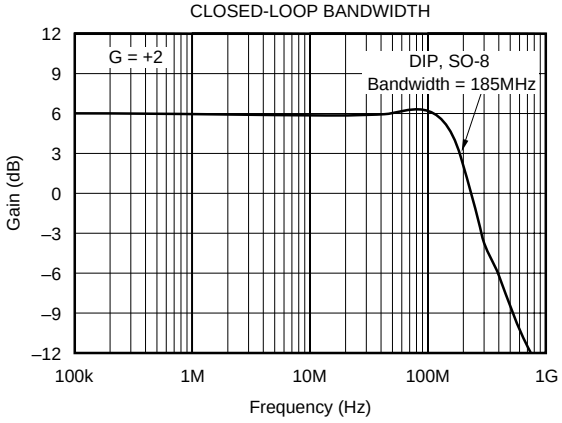
TYPICAL PERFORMANCE CURVES

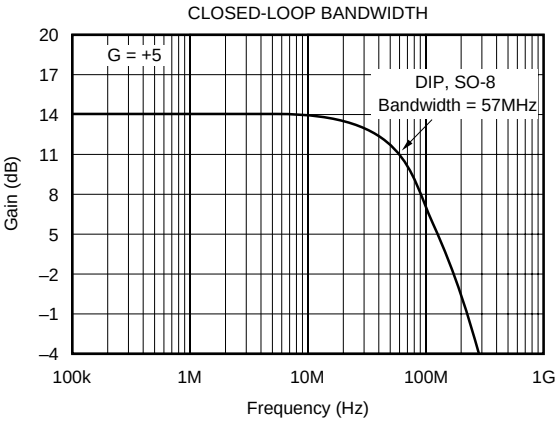
At T_A = +25°C, V_S = ±5V, R_{FB} = 100Ω, and R_L = 100Ω, unless otherwise noted. R_{FB} = 0 for G = +1.

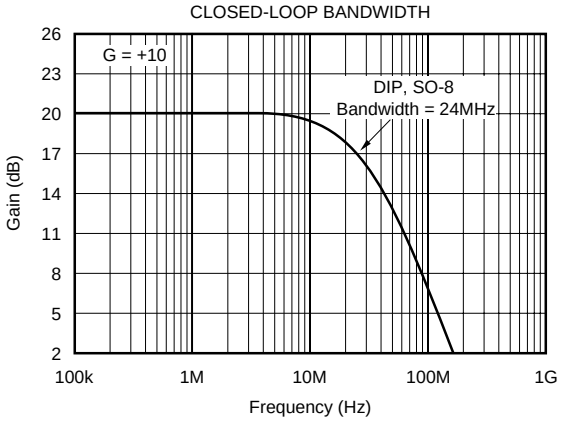








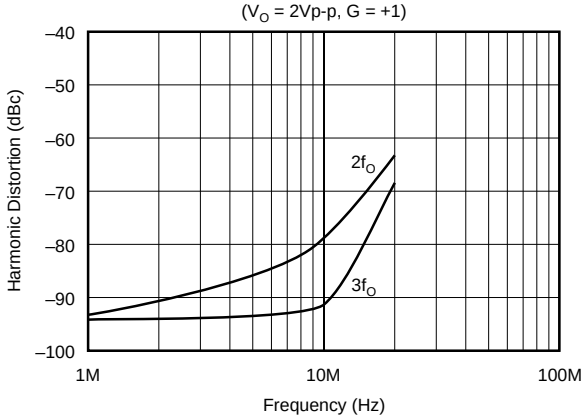




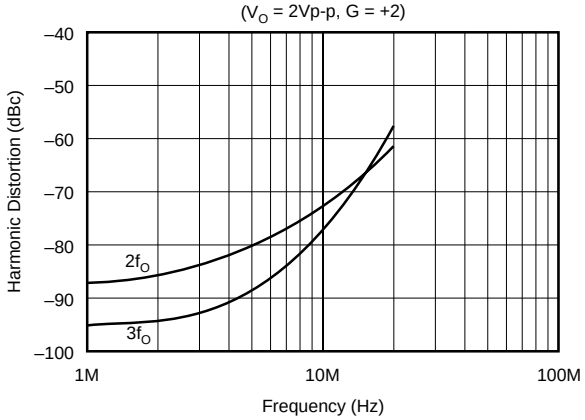
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_{FB} = 100Ω, and R_L = 100Ω, unless otherwise noted. R_{FB} = 0 for G = +1.

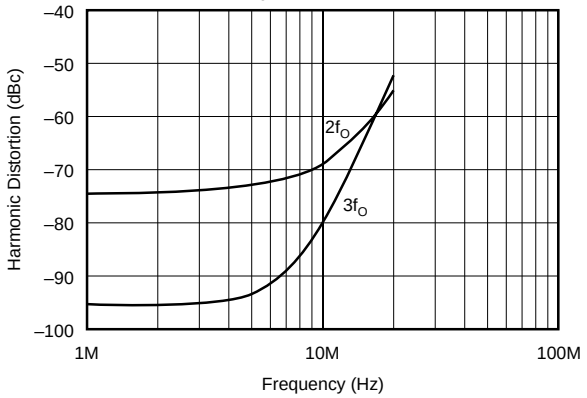
HARMONIC DISTORTION vs FREQUENCY
(V_O = 2Vp-p, G = +1)



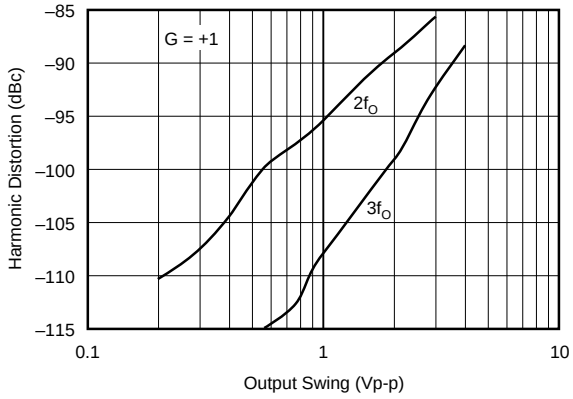
HARMONIC DISTORTION vs FREQUENCY
(V_O = 2Vp-p, G = +2)



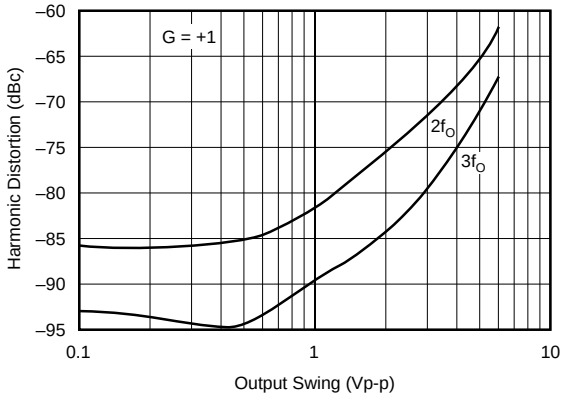
HARMONIC DISTORTION vs FREQUENCY
(V_O = 2Vp-p, G = +5)



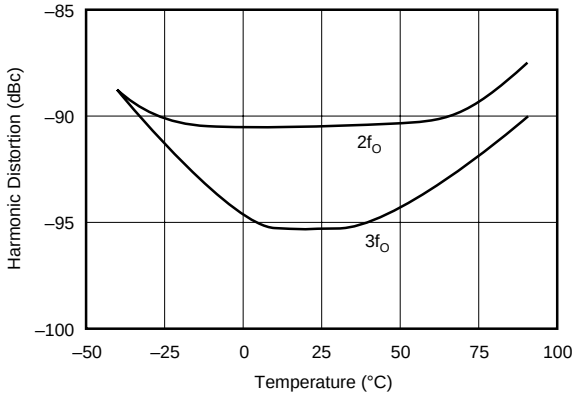
5MHz HARMONIC DISTORTION
vs OUTPUT SWING



10MHz HARMONIC DISTORTION
vs OUTPUT SWING



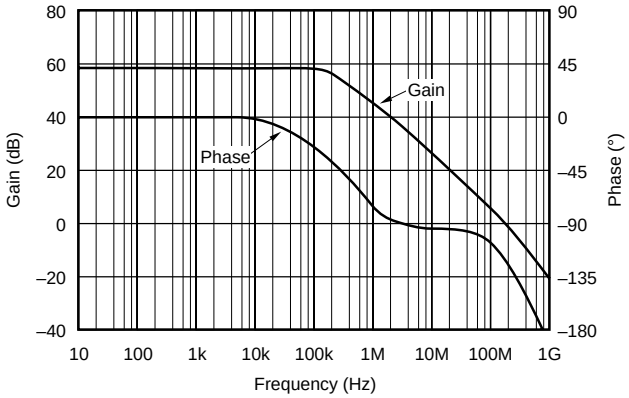
HARMONIC DISTORTION vs TEMPERATURE
(V_O = 2Vp-p, G = +1, f_O = 5MHz)



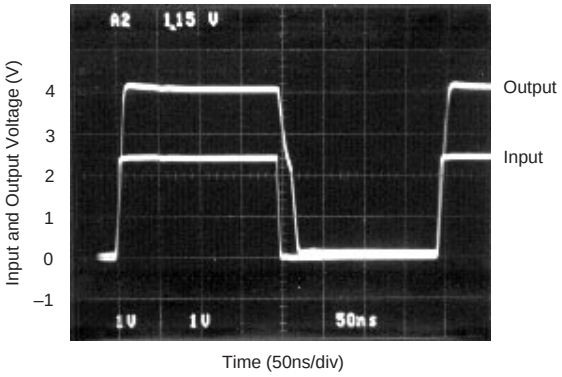
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_{FB} = 100Ω, and R_L = 100Ω, unless otherwise noted. R_{FB} = 0 for G = +1.

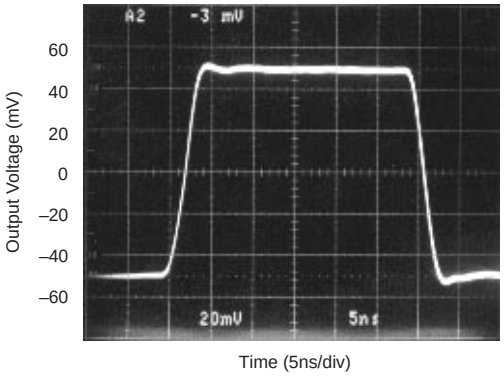
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



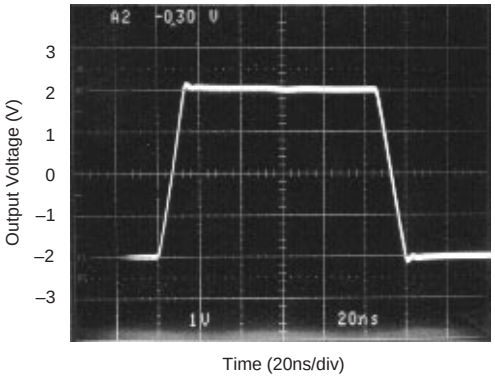
OVERDRIVE RECOVERY, G = +3



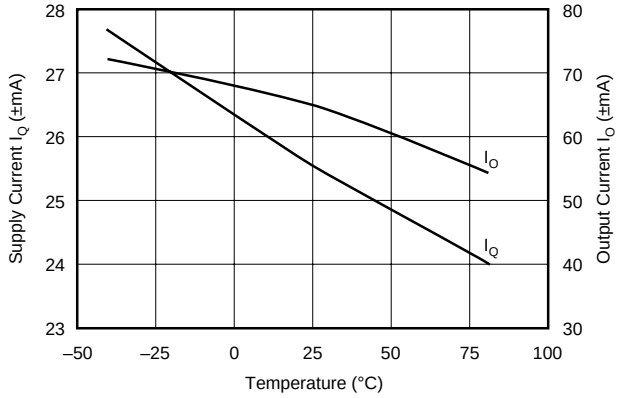
SMALL-SIGNAL TRANSIENT RESPONSE



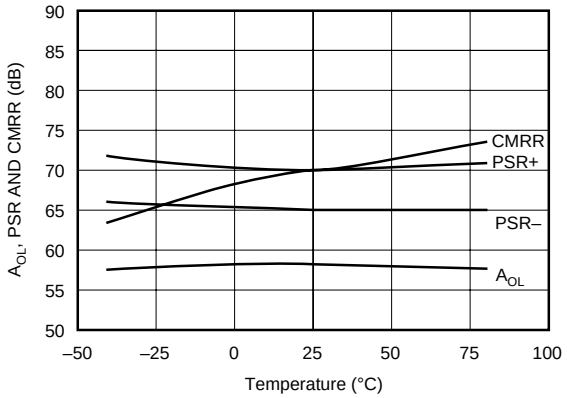
LARGE-SIGNAL TRANSIENT RESPONSE



SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



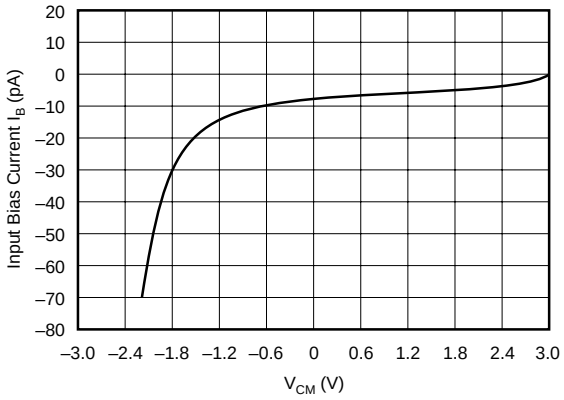
A_{OL}, PSR AND CMRR vs TEMPERATURE



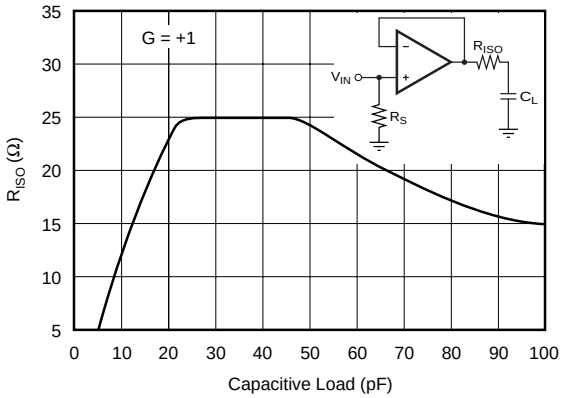
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_{FB} = 100Ω, and R_L = 100Ω, unless otherwise noted. R_{FB} = 0 for G = +1.

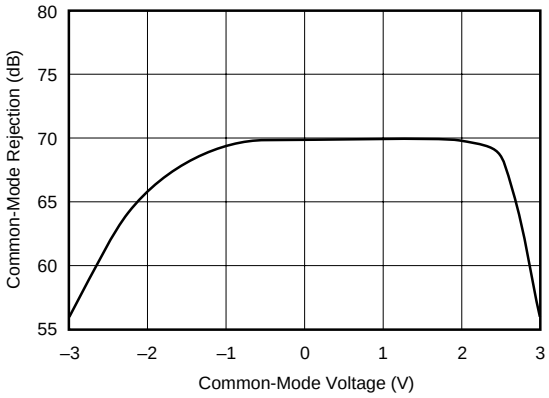
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



RECOMMENDED RESISTANCE
vs CAPACITIVE LOAD



COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



DISCUSSION OF PERFORMANCE

Amplifiers using FET input transistors operate in a similar manner to those using bipolar transistors, with some important advantages. In standard op amp applications, the very low input bias currents reduce the DC error voltage due to a high or possibly unknown source impedance. In most OPA655 applications, the output DC error will be due only to the low 1mV input offset voltage. Similarly, input noise currents will contribute very little to the total output noise in most applications. Wideband transimpedance applications (e.g., photodiode amplifiers) will particularly benefit from the low current noise combined with the OPA655's very low $6nV/\sqrt{Hz}$ input voltage noise.

The OPA655's high gain bandwidth and very linear output stage hold the harmonic distortion below –90dBc through 5MHz for a 2Vp-p swing into 100Ω. Significantly less distortion is observed at lower frequencies and/or higher load impedance. The voltage feedback architecture supports this level of accuracy with greater than 65dB power supply and common mode rejection ratios. This very high dynamic range, along with the low DC errors and noise of the FET input stage, can provide an exceptional buffering capability for ADC's, PMT's and other applications requiring high impedance sensing of a high speed signal. For similar distortion performance with a bipolar input stage, refer to the OPA642.

OPERATING CONSIDERATIONS

Careful attention to PC board layout will deliver the exceptional performance shown in the Typical Performance Curves. Generally, very low impedance paths to the power supplies, along with low parasitic connections to the signal I/O pins are required for best performance (See Layout and Interconnect Considerations). Use of a guard ring around the non-inverting input can reduce the leakage current due to common mode input signals. However, driving the guard from the inverting node, can increase the differential input capacitance, possibly leading to instability or increased broadband noise. Non-inverting buffer applications require a very low inductance short to be connected between the output and inverting input to minimize peaking in the frequency response. Use a wide trace (0.1") directly between the output and inverting input pins on the component side of the board for this connection.

The OPA655 is nominally designed to operate from ±5V supplies. The maximum voltage between the supply pins should be limited to less than 11V. Since a supply independent bias is used, very little change in AC performance is observed as the supply voltage is changed.

BASIC OP AMP CONNECTIONS

Figures 2 through 4 illustrate the basic op amp connections suitable for the OPA655. The non-inverting buffer (voltage follower) application (Figure 2) will benefit from the very

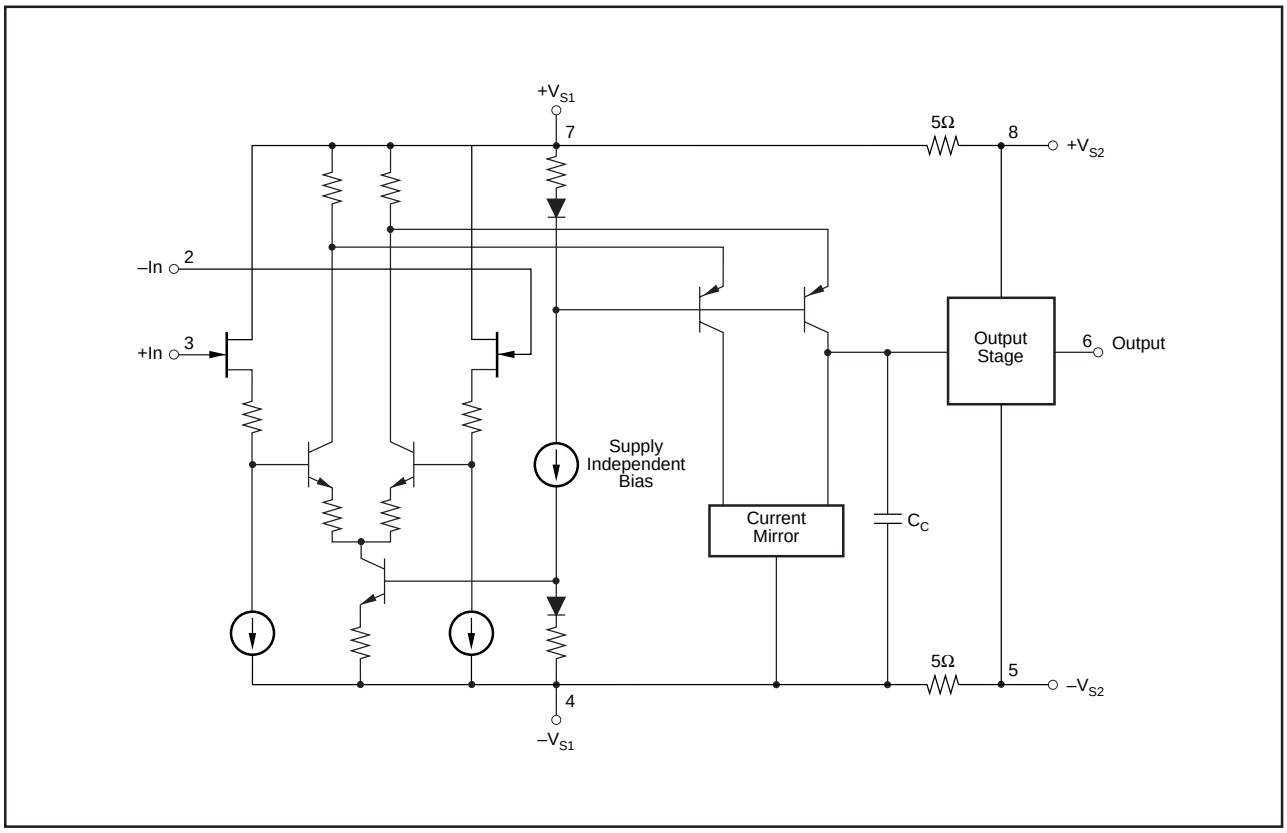


FIGURE 1. Simplified Internal Schematic.

high FET input impedance and low closed loop output impedance. Remember that a DC path to the input is still necessary; even with the ultra low FET input bias current (5pA), open or capacitively coupled sources will cause the input to saturate. For best frequency response, a direct short between the output and inverting inputs is suggested. Since the input bias currents are not necessarily correlated, matching the non-inverting source resistance with a resistor in the feedback network is not recommended.

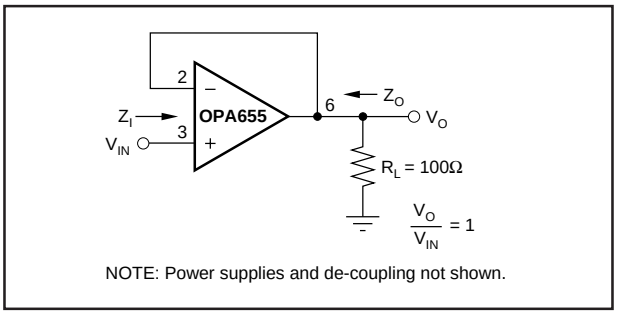


FIGURE 2. Non-Inverting Unity Gain Buffer.

The non-inverting amplifier configuration (Figure 3) will again present a very high input impedance to the input signal and a low output impedance drive with signal gain. The 100Ω shown for R_F will give the frequency response shown in the Typical Performance Curves. Higher values for R_F and R_1 are possible but for high frequency non-inverting op amp applications, should be limited to less than 1.0kΩ. The amplifier will be loaded by (R_F + R_1) in parallel with the load impedance.

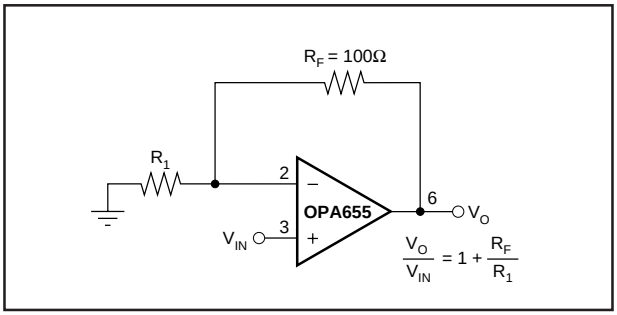


FIGURE 3. Non-Inverting Op Amp.

The inverting amplifier configuration (Figure 4) offers a broadband, low DC error amplifier with a controlled input impedance. The input impedance may be set by adjusting R_1 to the desired value and then adjusting R_F to the desired gain, or by setting R_F and R_1 to the desired values then controlling the input impedance independently as the parallel combination of R_1 and an optional R_T resistor to ground. To estimate the bandwidth in any configuration, first calculate the gain as a non-inverting amplifier. This is often referred to as "noise gain" or NG, and is simply the inverse of the feedback factor β.

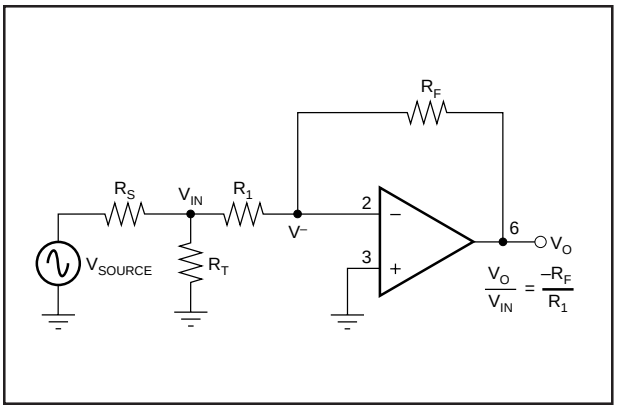


FIGURE 4. Inverting Op Amp.

$\beta = V^-/V_O$

Non-Inverting Gain = Noise Gain = NG = 1/β

Taking the inverting amplifier as an example, β is found by setting V_{SOURCE} to zero and calculating the voltage divider ratio from V_O to V^-:

$R_1 + R_T \parallel R_S$ = total resistance to ground on the inverting input

$$\beta = \frac{V^-}{V_O} = \frac{R_1 + R_T \| R_S}{R_F + R_1 + R_T \| R_S}$$

$$NG = \frac{1}{\beta} = 1 + \frac{R_F}{R_1 + R_T \| R_S}$$

The resulting bandwidth is approximately the amplifier's gain bandwidth product divided by the calculated noise gain:

$$BW \approx GBW/NG$$

In practice, low noise gains (< 5) will produce a wider bandwidth than predicted due to the peaking effect of second order poles. For example, at an inverting gain of –1 from a zero ohm source impedance, this yields a non-inverting gain of 2 and an approximate signal bandwidth of 185MHz.

TYPICAL APPLICATIONS

WIDEBAND TRANSIMPEDANCE AMPLIFIER

The high gain bandwidth product and low noise of the OPA655 make it particularly suitable for wideband transimpedance applications. The front page of the data sheet shows measured results for a 1MΩ transimpedance gain from a relatively large diode having 47pF parasitic capacitance. The key to broadband transimpedance applications is to set the compensation capacitance across the feedback resistor to achieve a flat, or bandlimited, frequency

response. Figure 5 shows the analysis circuit for setting the feedback compensation capacitor, C_F, while Figure 6 shows the Bode analysis.

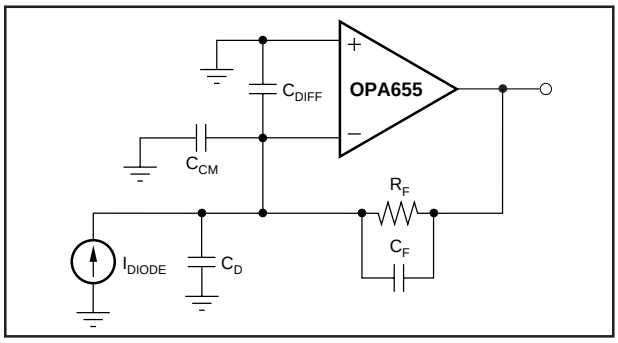


FIGURE 5. Transimpedance Analysis Circuit.

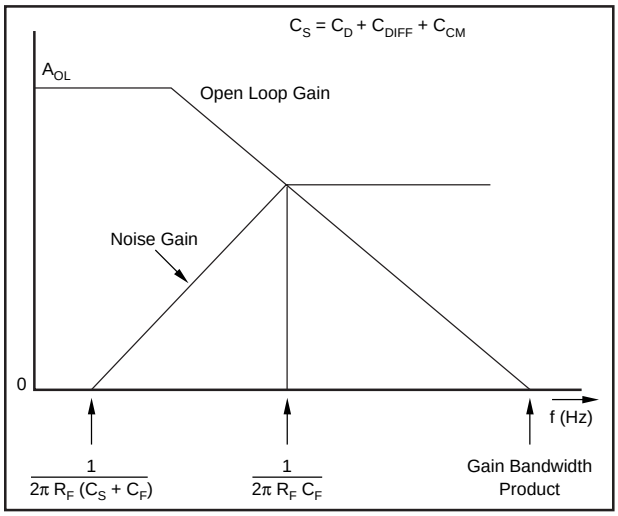


FIGURE 6. Bode Analysis for Transimpedance Circuit.

The total capacitance to ground on the inverting input of the OPA655 will set the source capacitance (C_S) for analysis purposes. C_S is the sum of the diode capacitance (C_D), the common mode input capacitance C_{CM} and the differential input capacitance (C_{DIFF}). Looking at the Bode analysis for the transimpedance configuration, at low frequencies the noise gain is 1 (0dB) but will increase for frequencies above $1/2\pi(R_F \bullet (C_S + C_F))$ due to the zero formed by the capacitance on the inverting node. It is important to note that the gain for the op amp input noise voltage will increase similarly. To get maximum bandwidth, C_F is often set to form a high frequency pole at the intersection of this increasing noise gain and the open loop gain rolloff. This is accomplished by setting $1/2\pi(R_F \bullet C_F)$ equal to the geometric mean of the zero frequency and the gain bandwidth product of the op amp. If the gain bandwidth product is in Hz, and assuming that $C_F << C_S$, C_F may be calculated as:

$$C_F = \left[\frac{1}{R_F \bullet \sqrt{\frac{(2\pi \bullet GBWP)}{(R_F \bullet C_S)}}} \right]$$

to set the high frequency pole for the noise gain at its intersection with the open loop gain response.

If the $1/2\pi R_F C_F$ pole for the noise gain were set exactly at the intersection with the amplifier's open loop gain rolloff, the circuit would be operating with a 45° phase margin yielding a highly peaked frequency response. To reduce broadband noise and pulse response ringing, it is preferable to set this pole at a slightly lower frequency than the simplified analysis shown above. A second order analysis for the transimpedance configuration yields the following results to achieve a maximally flat Butterworth characteristic for the transimpedance frequency response. Using the OPA655's gain bandwidth product (GBW) in Hz, define a variable:

$$\alpha = R_F \bullet C_S \bullet GBW \bullet 2\pi \text{ (where } C_S = C_D + C_{CM} + C_{DIFF})$$

Then, the required C_F to produce a maximally flat frequency response is:

$$C_F = C_S \bullet \frac{\sqrt{2\alpha - 1}}{\alpha} \approx C_S \sqrt{\frac{2}{\alpha}}$$

and the resulting –3dB bandwidth for the transimpedance gain will be:

$$F_{-3dB} = GBW \bullet \sqrt{\frac{2}{\alpha + \sqrt{2\alpha - 1}}}$$

Figure 7 plots the required C_F vs R_F (given different values for the diode capacitance) to achieve the maximally flat response. Figure 8 plots the resulting bandwidth for the same range of R_F and C_D assuming C_F has been set as shown in Figure 7. These plots include a parasitic input capacitance of 2.2pF in parallel with the diode capacitance (C_D). Very low effective values for the compensation capacitor (C_F) can be produced by splitting the feedback resistor as shown on the front page application circuit.

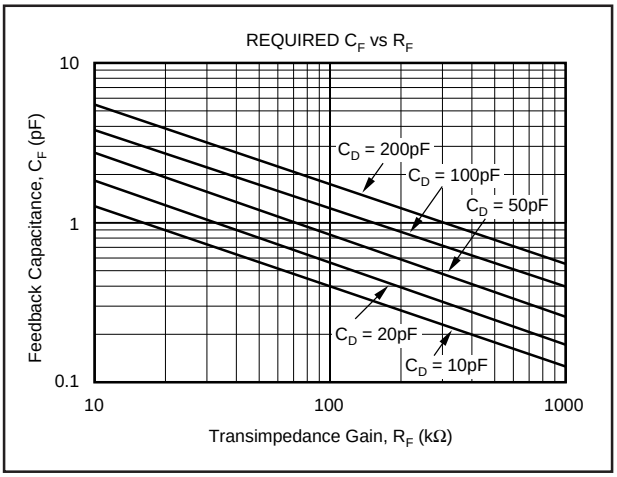


FIGURE 7. Compensation Capacitance vs Feedback Resistance.

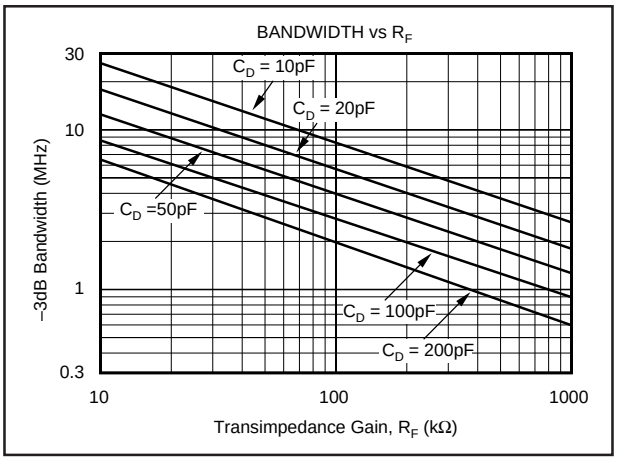


FIGURE 8. Maximally Flat Bandwidth.

HIGH SPEED INSTRUMENTATION DIFFERENTIAL AMPLIFIER

Very high speed differential amplifiers can be implemented using the OPA655. The very low input bias currents allow relatively high resistor values to be used in a standard single op amp differential configuration. Alternatively, a very high input impedance differential amplifier can be implemented using a three op amp instrumentation amplifier topology as shown in Figure 9.

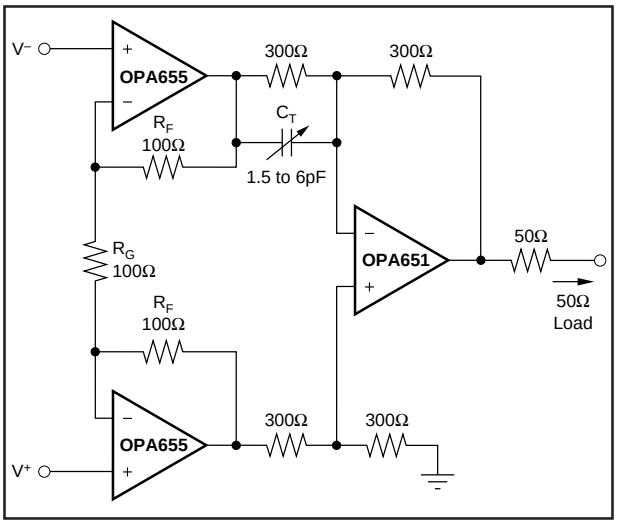


FIGURE 9. High Input Impedance, Broadband INA.

In this example, the OPA655's provide a differential gain of:

$$\left(1+\frac{2R_F}{R_G}\right)=3$$

and a common mode gain of 1 to the input of the OPA651 differential stage. The OPA651, a gain of 2 stable, broadband voltage feedback op amp, rejects the common mode signal and provides a differential gain of 1/2 the matched 50Ω load. This circuit delivers a 136MHz bandwidth at a differential gain of 1.5V/V (3.5dB) to the matched load as shown in Figure 10. The C_T tuning capacitor is used to match the high frequency gains for the two signal paths to improve the high frequency CMRR. Using this adjustment, a CMRR > 40dB through 100MHz was achieved.

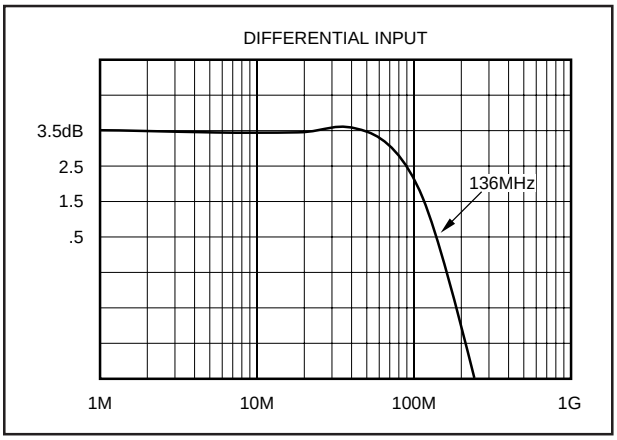


FIGURE 10. Measured Frequency Response for INA.

OPTIMIZING PERFORMANCE

DC ACCURACY

The OPA655 is laser trimmed for low input offset voltage, limiting the need for external trim circuits. In most cases, the low bias current of the FET input will not contribute significantly to the output DC error. For example, at minimum gain (G = +1) and maximum temperature (85°C), the error contribution due to the inverting input bias current would only exceed the input offset voltage for feedback resistors > (1mV/3.2nA) = 312kΩ. Only for relatively high source and/or feedback resistor values will the input bias current contribute significantly to the output DC error. Similarly, since the two input bias currents are very low, but not tightly matched, input bias current cancellation through source impedance matching is not recommended.

Changes in the power supply voltages contribute to shifts in the input offset voltage. This can be calculated using the PSR specifications. For example, a 0.5V change in the negative power supply will show up typically as a $0.5V \cdot 10^{(-65/20)} = 0.28mV$ change in the input offset voltage.

Negative common mode voltage inputs can cause an increase in the input bias currents as shown in the Typical Performance Curves. This can have an effect on DC accuracy when the source and/or feedback resistors are large and the common mode input voltage approaches the negative limit of –2.5V. Positive input biases are therefore preferred for diode transimpedance applications requiring a bias voltage on the non-inverting op amp input.

FREQUENCY RESPONSE COMPENSATION

The OPA655 is internally compensated to be stable at unity gain into a 100Ω load with a nominal phase margin of 58°. This unity gain phase margin shows a slight peaking in the frequency response and requires a very low inductance shorting connection from the output pin to the inverting input pin for minimal peaking. This stable broadband performance at unity gain lends itself well to integrator and buffer applications.

Phase margin and flatness will improve at higher gains. Since phase margin is slightly load dependent, flatness in a gain of +2 can be modified by changing the loading. Very flat performance is shown in the Typical Performance Curves using a 100Ω feedback and 100Ω load. This may be peaked up by increasing the load or feedback resistors or rolled off by decreasing them. Recall that an inverting gain of –1 is equivalent to a gain of +2 for bandwidth purposes, i.e. noise gain equal to 2. The external compensation techniques developed for voltage feedback op amps can be applied to this device. For example, in the non-inverting configuration, placing a capacitor across the feedback resistor will reduce the gain to +1 starting at $f = 1/(2\pi R_F C_F)$ Hz. Alternatively, in the inverting configuration, the bandwidth may be limited without modifying the low frequency inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at higher frequencies, thereby limiting the bandwidth for the inverting input signal through the gain-bandwidth product.

At higher gains, the gain-bandwidth product (240MHz) of this voltage feedback topology will limit the achievable signal bandwidth. If FET input is not required and higher bandwidths at higher gains are needed, consider the broad bandwidth available from a current feedback op amp such as the OPA658.

DRIVING CAPACITIVE LOADS

The high open loop gain and Class AB output stage of the OPA655 are optimized for driving the low impedance of doubly terminated cables. Capacitive loads directly on the output pin can decrease phase margin leading to frequency response peaking and possibly sustained oscillations. This effect is particularly pronounced at unity gain and becomes less significant at higher gains. Frequency response flatness can be maintained into a capacitive load by isolating it with a resistor as shown in Figure 11. The Typical Performance Curves show a plot of the minimum value for R_{ISO} to hold a flat frequency response as C_L is increased. The 1kΩ shunt load across C_L shown in Figure 11 was the probe load for this measurement and should be considered optional.

PULSE AND OVERDRIVE PERFORMANCE

High speed amplifiers like the OPA655 can provide an extremely fast settling time for a pulse input. Excellent frequency response flatness and phase linearity are required

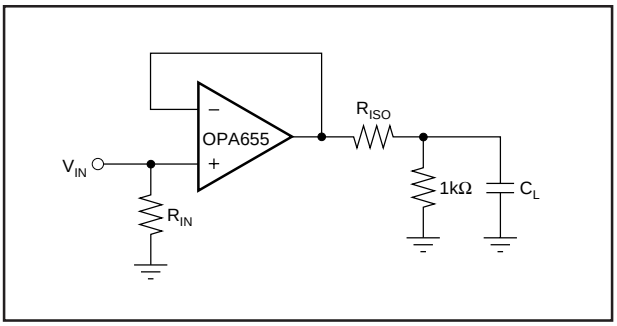


FIGURE 11. Driving a Capacitive Load.

to get the best settling times. As shown in the specifications table, settling time for a 1V step at a gain of +1 for the OPA655 is an extremely fast 8ns to 0.1%. This specification is defined as the time required, after the input transition, for the output to settle within a specified error band around its final value. For a 1V step, 0.1% settling corresponds to an error band of ±1mV. For the best settling times, little or no peaking in the frequency response can be allowed. Using the recommended R_{ISO} for capacitive loads will limit this peaking and reduce the settling times. Fast, extremely fine scale settling (0.01%) requires close attention to the ground return currents in the supply de-coupling capacitors. De-coupling the output stage power supply connections ($+V_{S2}$ + ($-V_{S2}$)) separately from the main supply inputs will improve both settling and harmonic distortion performance.

As can be observed in the typical performance curves, the OPA655 recovers very quickly from an input overdrive. For non-inverting operation, recovery is immediate for negative overdrives and < 10ns for a positive going overdrive signal. For inverting mode operation, such as transimpedance amplifiers, recovery is immediate to input overdrives that do not build up input voltages that exceeds the common mode input range. Unlike older FET input amplifiers, overdriving the inputs does not cause the output to invert phase and/or latch. Inputs that exceed the positive supply voltage will, however, cause the output to reverse and swing negative—but no latching will occur.

HARMONIC DISTORTION

The Typical Performance Curves show the very low harmonic distortion that OPA655 can deliver into a 100Ω load over a wide range of operating conditions. Generally, distortion improves at lower gains, lower signal swings, lower frequencies, and higher loads. Figure 12 shows significant improvement in second harmonic distortion as the load is increased, and relative insensitivity of the third harmonic to load conditions. For measurement purposes, these distortion levels were increased from those listed in the specification table by increasing the gain to +5. Narrowband communications systems will benefit from the very low third order distortion vs load which will provide very low intermodulation spurs.

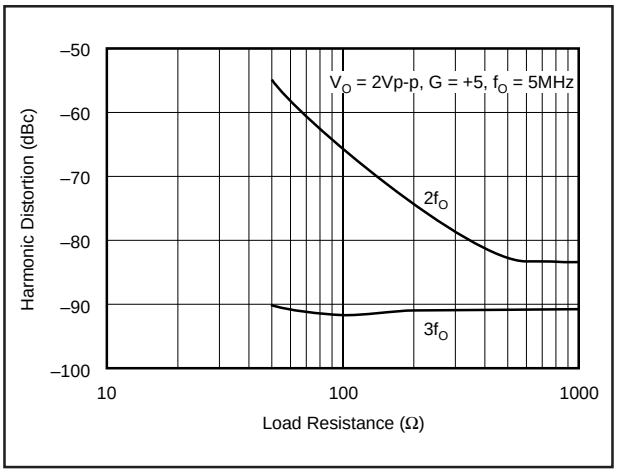


FIGURE 12. 5MHz Harmonic Distortion vs Load Resistance.

DIFFERENTIAL GAIN AND DIFFERENTIAL PHASE

The OPA655 provides one of the lowest dG/dP errors of any op amp. This specification is the change in the small signal gain and phase for a composite video color carrier frequency when the output voltage is slowly ramped over the luminance range. The specifications show less than 0.01%/0.01° for positive NTSC into a single video load. This level of performance challenges the accuracy of commercially available video test equipment. Measurements were taken using an HP9480 IC parametric test system.

OUTPUT DRIVE CAPABILITY

The guaranteed output current of ±28mA will drive a 100Ω load over the full guaranteed output voltage range of ±2.8V. These minimum performance levels are only applicable at cold temperatures, with higher output voltage and current available in most applications. Many demanding high speed applications, such as driving ADC's, require amplifiers with low, broadband, output impedance. As shown in Figure 13, the OPA655 maintains a very low closed loop output impedance over frequency. Closed loop output impedance increases with frequency as the loop gain rolls off.

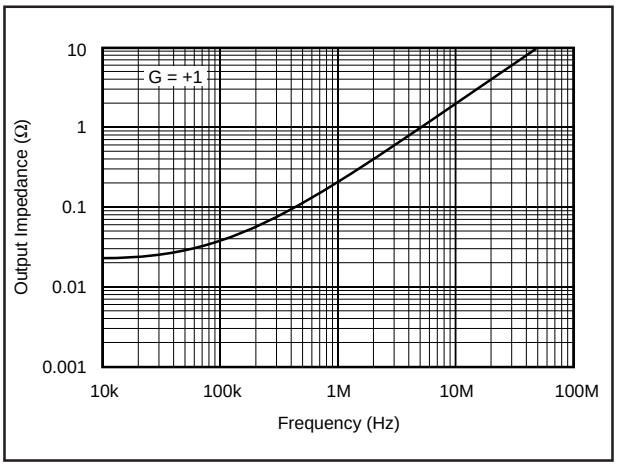


FIGURE 13. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA655 will not require heatsinking under most operating conditions. Maximum desired junction temperature will limit the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is a combination of the quiescent power plus the power dissipated in the output stage to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is a fixed DC voltage equal to 1/2 of either supply voltage (assuming equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading. Note that it is the power dissipated in the output stage and not in the load that determines internal power dissipation. As an example, compute the maximum T_J for the OPA655U at G = +2, R_L = 100Ω, R_F = 100Ω, $\pm V_S$ = ±5V, and at the specified maximum T_A = 85°C. P_D = 10V • 31mA + $(5^2)/[4 \bullet (100 \parallel 200)]$ = 404mW. Maximum T_J = 85°C + 0.404W • 125°C/W = 136°C.

LAYOUT AND INTERCONNECT CONSIDERATIONS

Achieving optimum performance with a high frequency amplifier like the OPA655 requires careful attention to layout parasitics and selection of external components. Suggestions include:

- **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the non-inverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- **Minimize the distance** (< 0.25") from the four power pins to high frequency 0.1µF decoupling capacitors. At the pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. The OPA655 may be operated with only pins 4 and 7 connected as supply pins allowing a direct replacement into existing 8 pin op amp pinouts. Connecting the output stage power pins separately, and decoupling them, will give the best distortion and settling performance. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

- **Careful selection and placement of external components will preserve the high frequency performance of the OPA655.** Resistors should be a very low reactance type. Surface mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in the signal path for a high frequency application. For the lowest parasitic capacitance, consider the PR8351 style resistor from Precision Resistive Products (Phone No. 319-394-9131). These precision buffed resistors typically have less than 0.02pF shunt parasitic capacitance.

  Since the output pin and inverting input pin are most sensitive to parasitic capacitance, always place the feedback, gain setting, and series output resistor (if any) as close as possible to the package pins. For a voltage follower buffer application, a wide trace (0.1") on the component side of the board between pins 6 and 2 will reduce frequency response peaking. Be sure to open up ground and power planes around this trace to limit parasitic capacitance to an AC ground on the output pin.

- **Connections to other wideband devices** on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA655 is nominally compensated to operate with a 5pF parasitic load.

  If a long trace is required and the 6dB signal loss intrinsic to doubly terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

- **Socketing a high speed part like the OPA655 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high frequency flush mount pins (e.g. McKenzie Technology No. 710C) can give good results.

SPICE MODEL AND EVALUATION BOARDS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available on a disk from the Burr-Brown Applications Department.

The OPA655 is similar in distortion performance and identical in pinout to the OPA642. The demonstration boards developed for the OPA642 are recommended for the OPA655. The six boards available are:

Contact your local Burr-Brown sales office or distributor to order demonstration boards.

DEM-OPA64XP-F	8-pin DIP, unity gain follower configuration
DEM-OPA64XP-N	8-pin DIP, non-inverting gain configuration
DEM-OPA64XP-I	8-pin DIP, inverting gain configuration
DEM-OPA64XU-F	SO-8 Surface Mount, unity gain follower configuration
DEM-OPA64XU-N	SO-8 Surface Mount, non-inverting gain configuration
DEM-OPA64XU-I	SO-8 Surface Mount, inverting gain configuration

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA655P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA655U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
OPA655U-1	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI
OPA655U/2K5	OBSOLETE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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