

## 0.03 $\mu\text{V}/^\circ\text{C}$ 漂移、低噪声、轨到轨输出、 36V，零漂移运算放大器

查询样品: **OPA2188**

### 特性

- 低偏移电压: **25 $\mu\text{V}$**  (最大值)
- 零漂移: **0.03 $\mu\text{V}/^\circ\text{C}$**
- 低噪声: **8.8 nV/ $\sqrt{\text{Hz}}$**   
**0.1Hz 至 10Hz 噪声: 0.25 $\mu\text{V}_{\text{PP}}$**
- 出色的直流精度:  
电源抑制比 (PSRR): **142dB**  
共模抑制比 (CMRR): **146dB**  
开环路增益: **136dB**
- 增益带宽: **2MHz**
- 静态电流: **475 $\mu\text{A}$**  (最大值)
- 宽电源电压:  **$\pm 2\text{V}$  至  $\pm 18\text{V}$**
- 轨到轨输出:  
输入包括负电源轨
- 已过滤射频干扰 (RFI) 的输入
- 微型尺寸封装

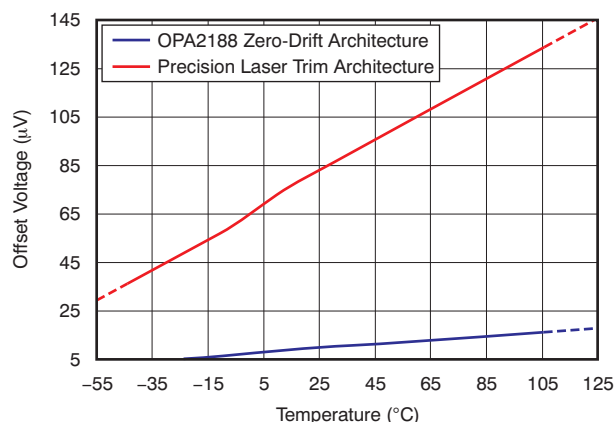
### 应用范围

- 桥式放大器
- 应力计
- 测试设备
- 变频器应用
- 温度测量
- 电子称
- 医疗仪表
- 电阻温度检测器
- 精密有源滤波器

### 说明

OPA2188 运算放大器使用 TI 拥有自主知识产权的自动归零技术来提供低偏移电压 (25 $\mu\text{V}$ , 最大值), 在时间和温度范围的接近零漂移。这些微型的、高精度、低静态电流放大器提供高输入阻抗和摆幅为电源轨 15mV 之内的轨到轨输出。输入共模范围包括负电源轨。单电源或者双电源可在 +4.0V 至 +36V ( $\pm 2\text{V}$  至  $\pm 18\text{V}$ ) 的范围内使用。

OPA2188 采用微型小外形尺寸 (MSOP)-8 和小外形尺寸 (SO)-14 封装。此器件额定工作温度范围为  $-40^\circ\text{C}$  至  $+105^\circ\text{C}$ 。



### 零漂移放大器产品系列

版本	产品	偏移电压 ( $\mu\text{V}$ )	偏移电压漂移 ( $\mu\text{V}/^\circ\text{C}$ )	带宽 (MHz)
单通道	OPA188 (4V 至 36V)	25	0.085	2
	OPA333(5V)	10	0.05	0.35
	OPA378(5V)	50	0.25	0.9
	OPA735(12V)	5	0.05	1.6
双通道	OPA2188 (4V 至 36V)	25	0.085	2
	OPA2333(5V)	10	0.05	0.35
	OPA2378(5V)	50	0.25	0.9
	OPA2735(12V)	5	0.05	1.6
四通道	OPA4188 (4V 至 36V)	25	0.085	2
	OPA4330(5V)	50	0.25	0.35



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2188	SO-8	D	–40°C to +105°C	2188	OPA2188AID	Rails, 100
					OPA2188AIDR	Tape and Reel, 2500
	MSOP-8	DGK	–40°C to +105°C	2188	OPA2188AIDGKT	Tape and Reel, 250
					OPA2188AIDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		VALUE	UNIT
Supply voltage		±20, 40 (single supply)	V
Signal input terminals <sup>(2)</sup>	Voltage	(V–) – 0.5 to (V+) + 0.5	V
	Current	±10	mA
Output short-circuit <sup>(3)</sup>		Continuous	
Temperature range	Operating, T <sub>A</sub>	–55 to +125	°C
	Storage, T <sub>stg</sub>	–65 to +150	°C
	Junction, T <sub>J</sub>	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	1.5	kV
	Charged device model (CDM)	1	kV

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

**ELECTRICAL CHARACTERISTICS:  
High-Voltage Operation,  $V_S = \pm 4\text{ V}$  to  $\pm 18\text{ V}$  ( $V_S = +8\text{ V}$  to  $+36\text{ V}$ )**

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA2188			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
$V_{\text{OS}}$	Input offset voltage		6	25	$\mu\text{V}$
	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		0.03	0.085	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$	0.075	0.3	$\mu\text{V}/\text{V}$
	$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			0.3	$\mu\text{V}/\text{V}$
	Long-term stability		4 <sup>(1)</sup>		$\mu\text{V}$
	Channel separation, dc		1		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>					
$I_B$	Input bias current	$V_{\text{CM}} = V_S / 2$	$\pm 160$	$\pm 850$	$\text{pA}$
	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			$\pm 4$	$\text{nA}$
$I_{\text{OS}}$	Input offset current		$\pm 320$	$\pm 1700$	$\text{pA}$
	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			$\pm 2$	$\text{nA}$
<b>NOISE</b>					
$e_n$	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$	0.25		$\mu\text{V}_{\text{PP}}$
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$	8.8		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$	7		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
$V_{\text{CM}}$	Common-mode voltage range		$V^-$	$(V^+) - 1.5$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V^-) < V_{\text{CM}} < (V^+) - 1.5\text{ V}$	120	134	$\text{dB}$
	$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 18\text{ V}$		130	146	$\text{dB}$
	$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 18\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		120	126	$\text{dB}$
<b>INPUT IMPEDANCE</b>					
	Differential		100    6		$\text{M}\Omega$    $\text{pF}$
	Common-mode		6    9.5		$10^{12}\ \Omega$    $\text{pF}$
<b>OPEN-LOOP GAIN</b>					
$A_{\text{OL}}$	Open-loop voltage gain	$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$	130	136	$\text{dB}$
	$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		120	126	$\text{dB}$
<b>FREQUENCY RESPONSE</b>					
GBW	Gain-bandwidth product		2		$\text{MHz}$
SR	Slew rate	$G = +1$	0.8		$\text{V}/\mu\text{s}$
	Settling time, 0.1%	$V_S = \pm 18\text{ V}$ , $G = 1$ , 10-V step	20		$\mu\text{s}$
	Settling time, 0.01%	$V_S = \pm 18\text{ V}$ , $G = 1$ , 10-V step	27		$\mu\text{s}$
	Overload recovery time	$V_{\text{IN}} \times G = V_S$	1		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	1 kHz, $G = 1$ , $V_{\text{OUT}} = 1\text{ V}_{\text{RMS}}$	0.0001		%

 (1) 1000-hour life test at  $+125^\circ\text{C}$  demonstrated randomly distributed variation in the range of measurement limits—approximately  $4\ \mu\text{V}$ .

**ELECTRICAL CHARACTERISTICS:**  
**High-Voltage Operation,  $V_S = \pm 4\text{ V}$  to  $\pm 18\text{ V}$  ( $V_S = +8\text{ V}$  to  $+36\text{ V}$ ) (continued)**

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA2188			UNIT
			MIN	TYP	MAX	
<b>OUTPUT</b>						
Voltage output swing from rail		No load		6	15	mV
		$R_L = 10\text{ k}\Omega$		220	250	mV
		$R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		310	350	mV
$I_{\text{SC}}$	Short-circuit current			$\pm 18$		mA
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0$		120		$\Omega$
$C_{\text{LOAD}}$	Capacitive load drive			1		nF
<b>POWER SUPPLY</b>						
$V_S$	Operating voltage range			4 to 36 ( $\pm 2$ to $\pm 18$ )		V
$I_Q$	Quiescent current (per amplifier)	$V_S = \pm 4\text{ V}$ to $V_S = \pm 18\text{ V}$		415	475	$\mu\text{A}$
		$I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			525	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>						
Temperature range	Specified			-40	+105	$^\circ\text{C}$
	Operating			-40	+125	$^\circ\text{C}$
	Storage			-65	+150	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS:  
Low-Voltage Operation,  $V_S = \pm 2\text{ V}$  to  $< \pm 4\text{ V}$  ( $V_S = +4\text{ V}$  to  $< +8\text{ V}$ )**

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA2188			UNIT
			MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>						
$V_{\text{OS}}$	Input offset voltage			6	25	$\mu\text{V}$
		$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		0.03	0.085	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$		0.075	0.3	$\mu\text{V}/\text{V}$
		$V_S = 4\text{ V}$ to $36\text{ V}$ , $V_{\text{CM}} = V_S / 2$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			0.3	$\mu\text{V}/\text{V}$
	Long-term stability			4 <sup>(1)</sup>		$\mu\text{V}$
	Channel separation, dc			1		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_{\text{CM}} = V_S / 2$		$\pm 160$	$\pm 850$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			$\pm 4$	$\text{nA}$
$I_{\text{OS}}$	Input offset current			$\pm 320$	$\pm 1700$	$\text{pA}$
		$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			$\pm 2$	$\text{nA}$
<b>NOISE</b>						
$e_n$	Input voltage noise	$f = 0.1\text{ Hz}$ to $10\text{ Hz}$		0.25		$\mu\text{V}_{\text{PP}}$
	Input voltage noise density	$f = 1\text{ kHz}$		8.8		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		7		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{\text{CM}}$	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$		$V^-$	$(V^+) - 1.5$	$\text{V}$
CMRR	Common-mode rejection ratio	$(V^-) < V_{\text{CM}} < (V^+) - 1.5\text{ V}$	106	114		$\text{dB}$
		$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 2\text{ V}$	114	120		$\text{dB}$
		$(V^-) + 0.5\text{ V} < V_{\text{CM}} < (V^+) - 1.5\text{ V}$ , $V_S = \pm 2\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$	110	120		$\text{dB}$
<b>INPUT IMPEDANCE</b>						
	Differential			100    6		$\text{M}\Omega$    $\text{pF}$
	Common-mode			6    95		$10^{12}\ \Omega$    $\text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{\text{OL}}$	Open-loop voltage gain	$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 5\text{ k}\Omega$ , $V_S = 5\text{ V}$	110	120		$\text{dB}$
		$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$	120	130		$\text{dB}$
		$(V^-) + 500\text{ mV} < V_{\text{O}} < (V^+) - 500\text{ mV}$ , $R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$	114	120		$\text{dB}$
<b>FREQUENCY RESPONSE</b>						
GBW	Gain-bandwidth product			2		$\text{MHz}$
SR	Slew rate	$G = +1$		0.8		$\text{V}/\mu\text{s}$
	Overload recovery time	$V_{\text{IN}} \times G = V_S$		1		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	1 kHz, $G = 1$ , $V_{\text{OUT}} = 1\text{ V}_{\text{RMS}}$		0.0001		%

 (1) 1000-hour life test at  $+125^\circ\text{C}$  demonstrated randomly distributed variation in the range of measurement limits—approximately  $4\ \mu\text{V}$ .

**ELECTRICAL CHARACTERISTICS:**  
**Low-Voltage Operation,  $V_S = \pm 2\text{ V}$  to  $< \pm 4\text{ V}$  ( $V_S = +4\text{ V}$  to  $< +8\text{ V}$ ) (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $V_{COM} = V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER		CONDITIONS	OPA2188			UNIT
			MIN	TYP	MAX	
<b>OUTPUT</b>						
Voltage output swing from rail	No load			6	15	mV
	$R_L = 10\text{ k}\Omega$			220	250	mV
	$R_L = 10\text{ k}\Omega$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			310	350	mV
$I_{SC}$	Short-circuit current		$\pm 18$			mA
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0$	120			$\Omega$
$C_{LOAD}$	Capacitive load drive		1			nF
<b>POWER SUPPLY</b>						
$V_S$	Operating voltage range		4 to 36 ( $\pm 2$ to $\pm 18$ )			V
$I_Q$	Quiescent current (per amplifier)	$V_S = \pm 2\text{ V}$ to $V_S = \pm 4\text{ V}$	385		440	$\mu\text{A}$
		$I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$			525	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>						
Temperature range	Specified		-40			$^\circ\text{C}$
	Operating		-40			$^\circ\text{C}$
	Storage		-65			$^\circ\text{C}$

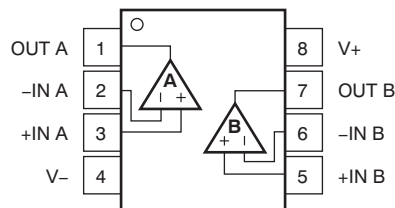
**THERMAL INFORMATION: OPA2188**

THERMAL METRIC <sup>(1)</sup>		OPA2188ID	OPA2188IDGK	UNITS
		D	DGK	
		8 PINS	8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	111.0	159.3	$^\circ\text{C}/\text{W}$
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	54.9	37.4	
$\theta_{JB}$	Junction-to-board thermal resistance	51.7	48.5	
$\psi_{JT}$	Junction-to-top characterization parameter	9.3	1.2	
$\psi_{JB}$	Junction-to-board characterization parameter	51.1	77.1	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) 有关传统和新的热 度量的更多信息，请参阅IC 封装热度量应用报告，SPRA953。

**PIN CONFIGURATION**

**D, DGK PACKAGES  
 SO-8, MSOP-8  
 (TOP VIEW)**



## TYPICAL CHARACTERISTICS

**Table 1. Characteristic Performance Measurements**

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	<a href="#">Figure 1</a>
Offset Voltage Drift Distribution	<a href="#">Figure 2</a>
Offset Voltage vs Temperature	<a href="#">Figure 3</a>
Offset Voltage vs Common-Mode Voltage	<a href="#">Figure 4, Figure 5</a>
Offset Voltage vs Power Supply	<a href="#">Figure 6</a>
$I_B$ and $I_{OS}$ vs Common-Mode Voltage	<a href="#">Figure 7</a>
Input Bias Current vs Temperature	<a href="#">Figure 8</a>
Output Voltage Swing vs Output Current (Maximum Supply)	<a href="#">Figure 9</a>
CMRR and PSRR vs Frequency (Referred-to-Input)	<a href="#">Figure 10</a>
CMRR vs Temperature	<a href="#">Figure 11, Figure 12</a>
PSRR vs Temperature	<a href="#">Figure 13</a>
0.1-Hz to 10-Hz Noise	<a href="#">Figure 14</a>
Input Voltage Noise Spectral Density vs Frequency	<a href="#">Figure 15</a>
THD+N Ratio vs Frequency	<a href="#">Figure 16</a>
THD+N vs Output Amplitude	<a href="#">Figure 17</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 18</a>
Quiescent Current vs Temperature	<a href="#">Figure 19</a>
Open-Loop Gain and Phase vs Frequency	<a href="#">Figure 20</a>
Closed-Loop Gain vs Frequency	<a href="#">Figure 21</a>
Open-Loop Gain vs Temperature	<a href="#">Figure 22</a>
Open-Loop Output Impedance vs Frequency	<a href="#">Figure 23</a>
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	<a href="#">Figure 24, Figure 25</a>
No Phase Reversal	<a href="#">Figure 26</a>
Positive Overload Recovery	<a href="#">Figure 27</a>
Negative Overload Recovery	<a href="#">Figure 28</a>
Small-Signal Step Response (100 mV)	<a href="#">Figure 29, Figure 30</a>
Large-Signal Step Response	<a href="#">Figure 31, Figure 32</a>
Large-Signal Settling Time (10-V Positive Step)	<a href="#">Figure 33</a>
Large-Signal Settling Time (10-V Negative Step)	<a href="#">Figure 34</a>
Short-Circuit Current vs Temperature	<a href="#">Figure 35</a>
Maximum Output Voltage vs Frequency	<a href="#">Figure 36</a>
Channel Separation vs Frequency	<a href="#">Figure 37</a>
EMIRR IN+ vs Frequency	<a href="#">Figure 38</a>

### TYPICAL CHARACTERISTICS

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

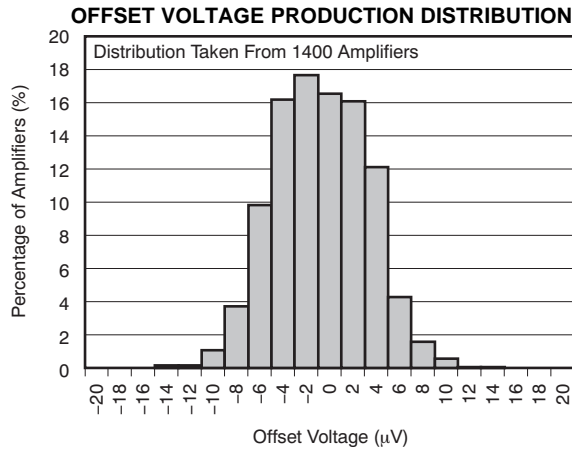


Figure 1.

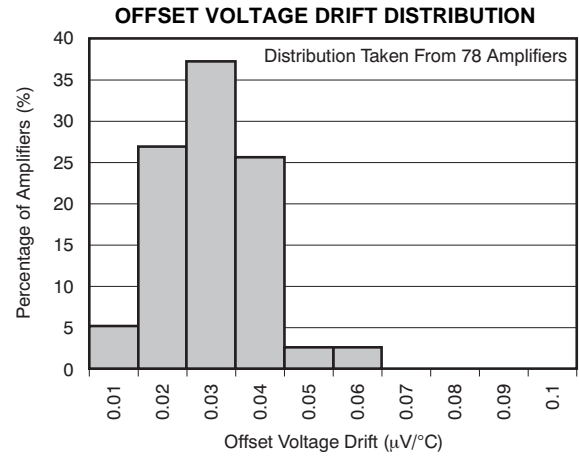


Figure 2.

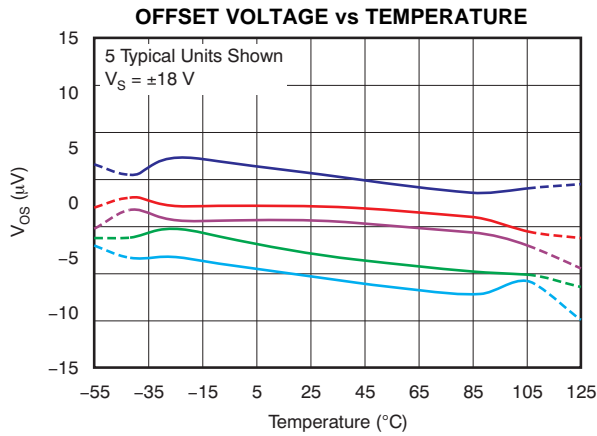


Figure 3.

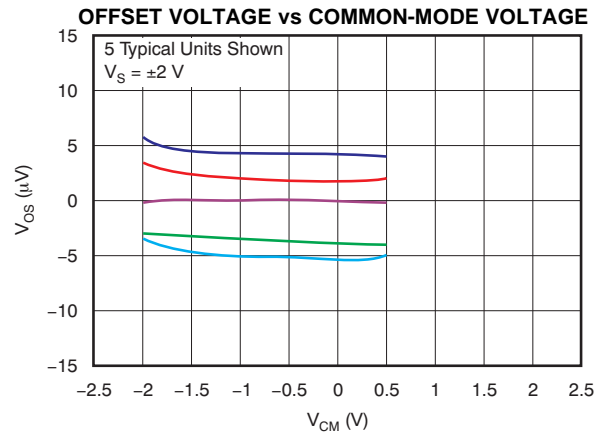


Figure 4.

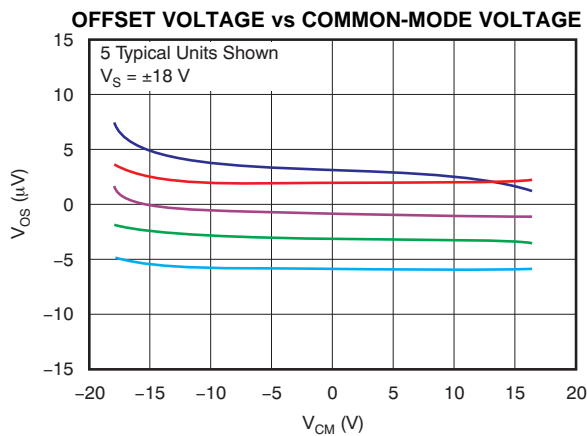


Figure 5.

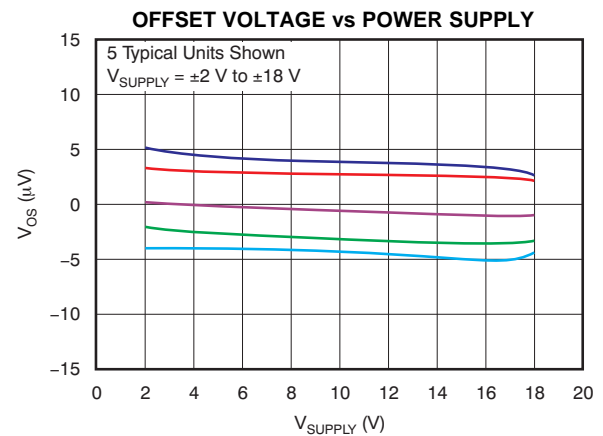


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

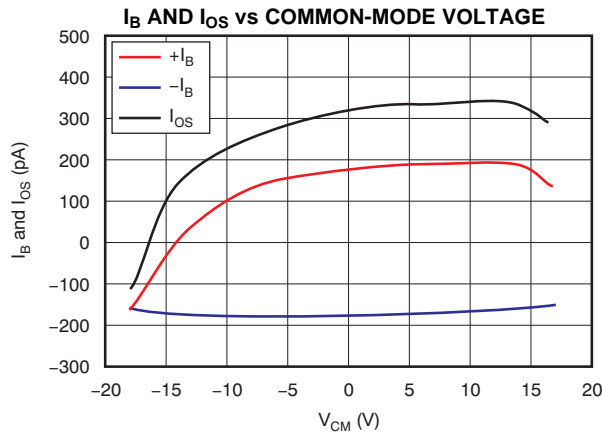


Figure 7.

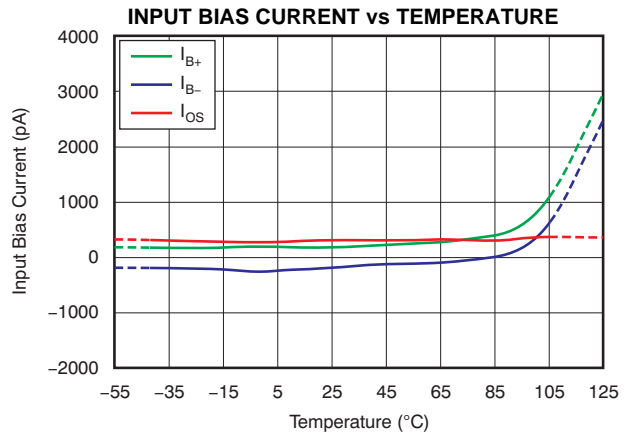


Figure 8.

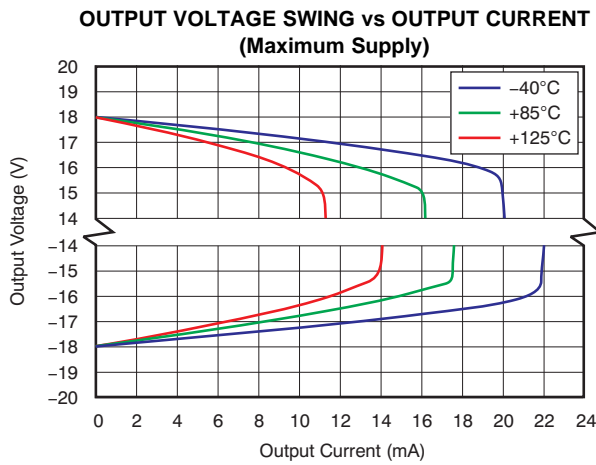


Figure 9.

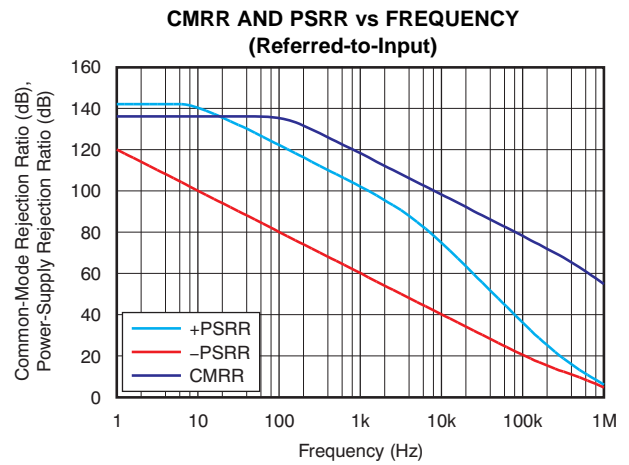


Figure 10.

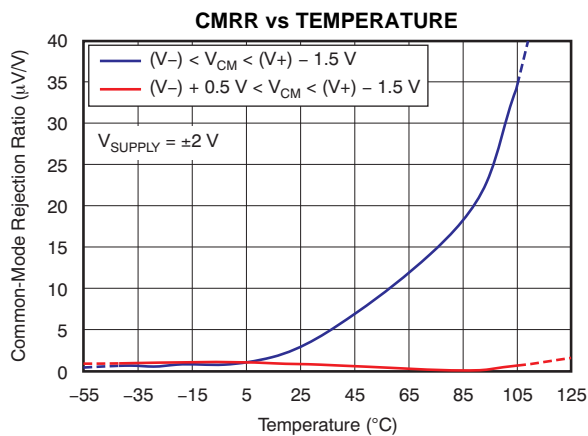


Figure 11.

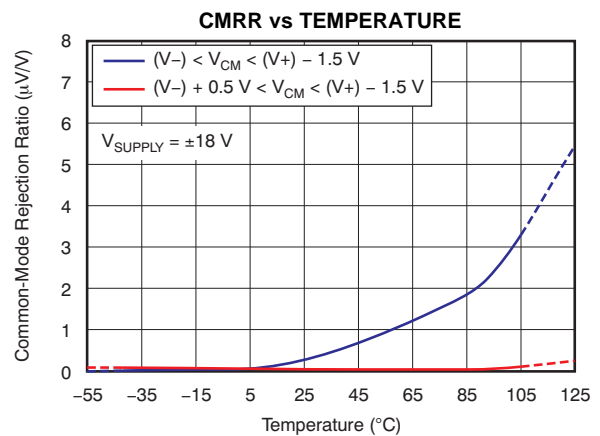


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

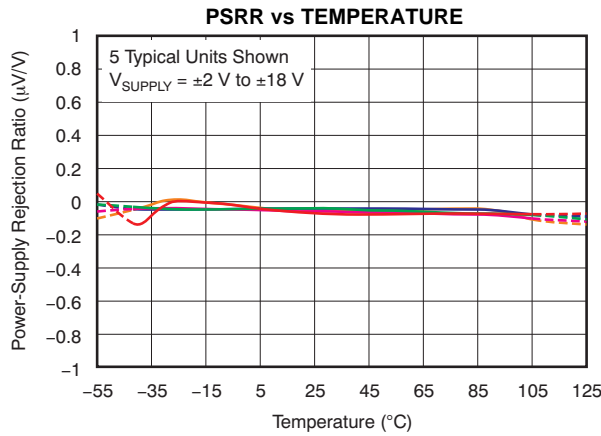


Figure 13.

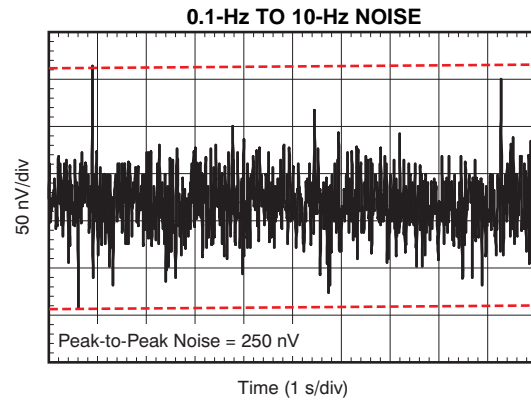


Figure 14.

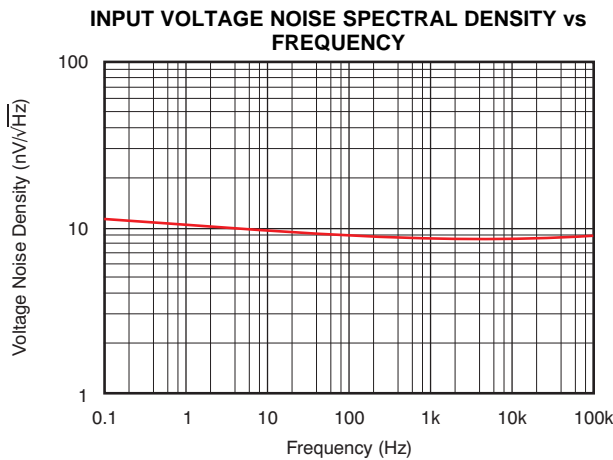


Figure 15.

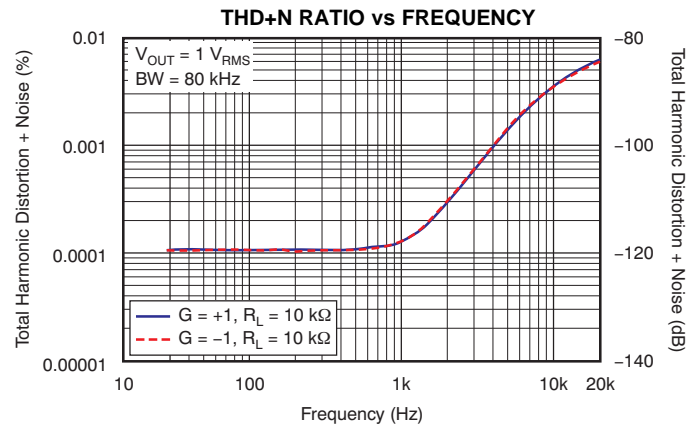


Figure 16.

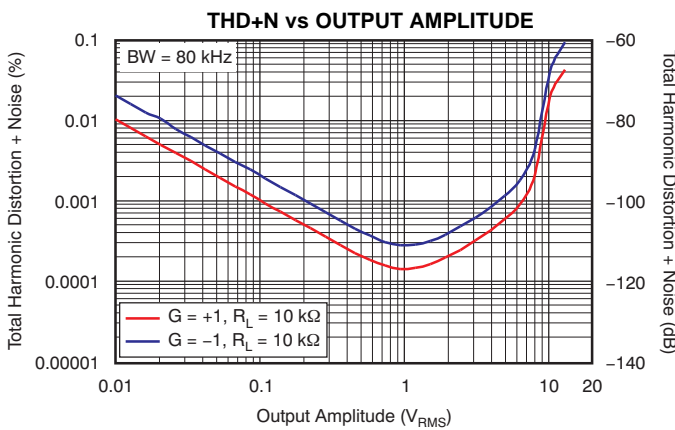


Figure 17.

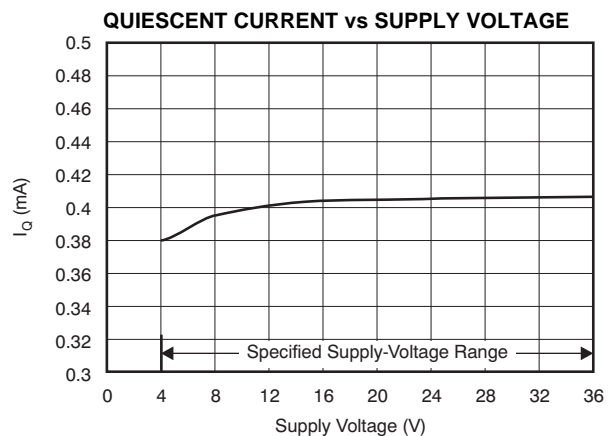


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

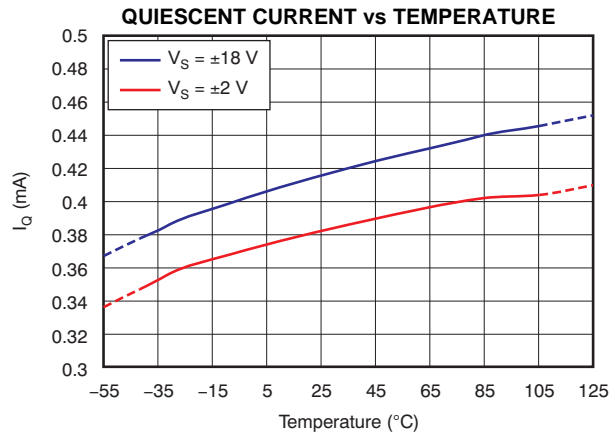


Figure 19.

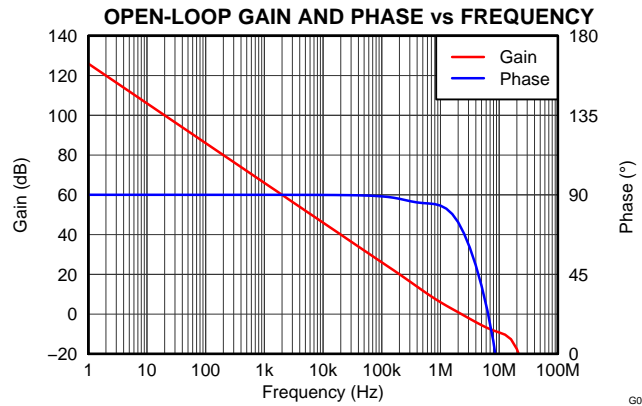


Figure 20.

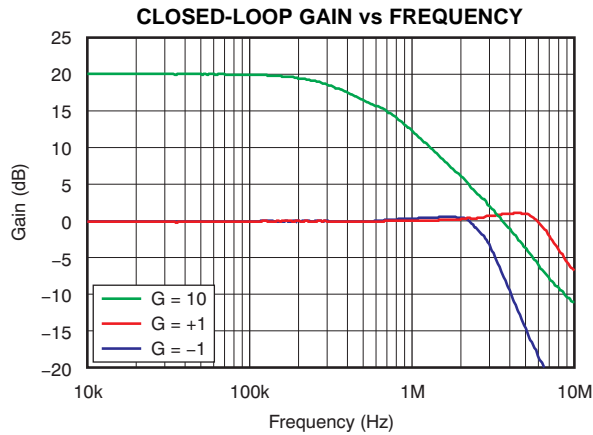


Figure 21.

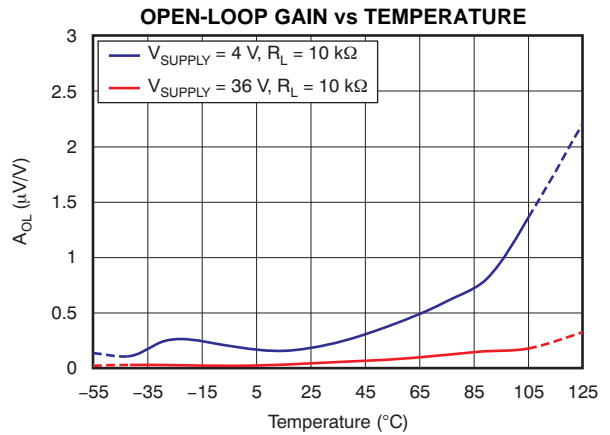


Figure 22.

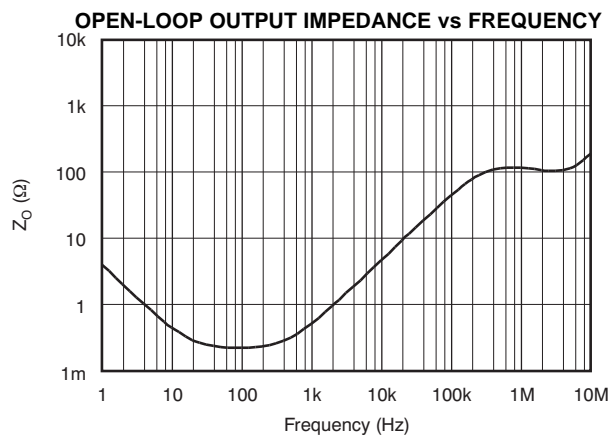


Figure 23.

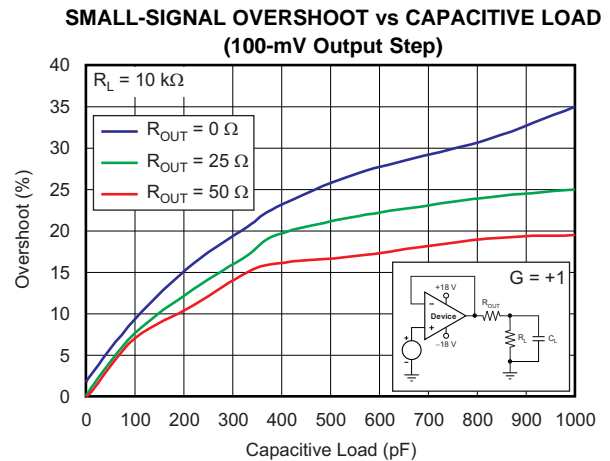


Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD  
(100-mV Output Step)**

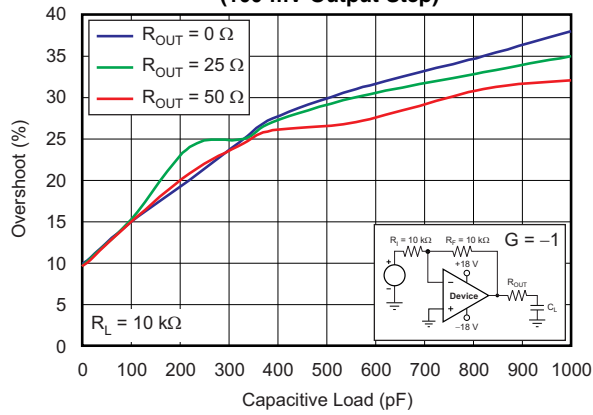


Figure 25.

**NO PHASE REVERSAL**

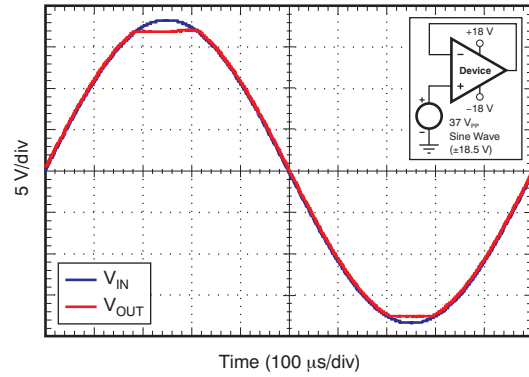


Figure 26.

**POSITIVE OVERLOAD RECOVERY**

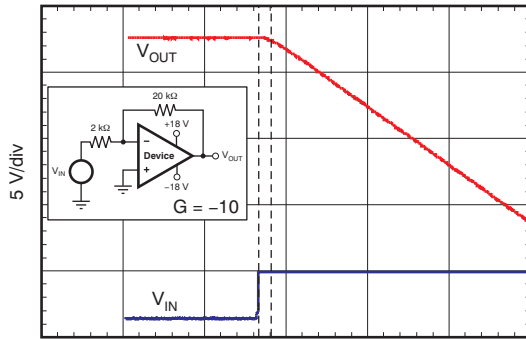


Figure 27.

**NEGATIVE OVERLOAD RECOVERY**

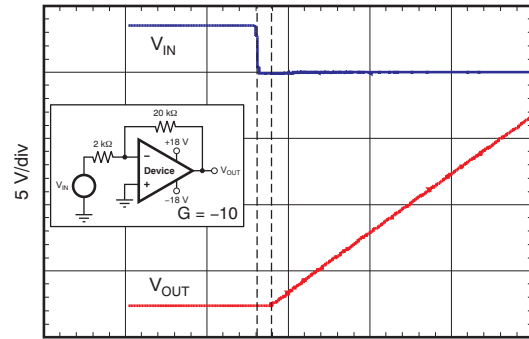


Figure 28.

**SMALL-SIGNAL STEP RESPONSE  
(100 mV)**

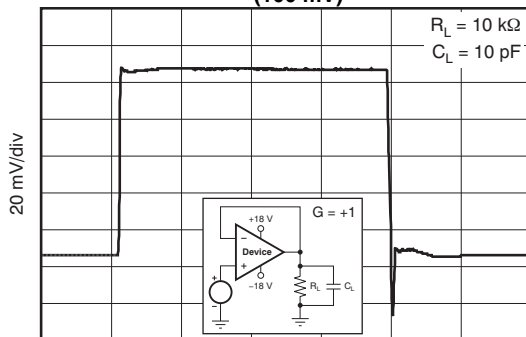


Figure 29.

**SMALL-SIGNAL STEP RESPONSE  
(100 mV)**

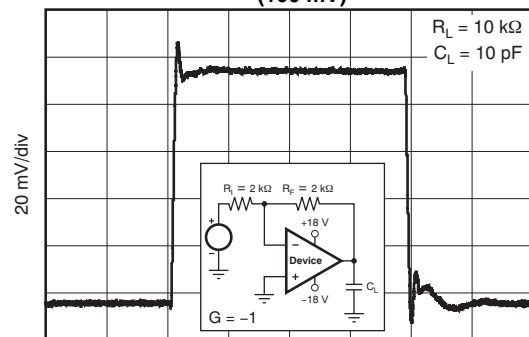


Figure 30.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

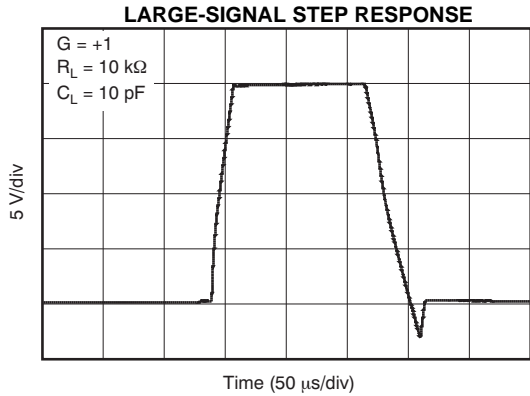


Figure 31.

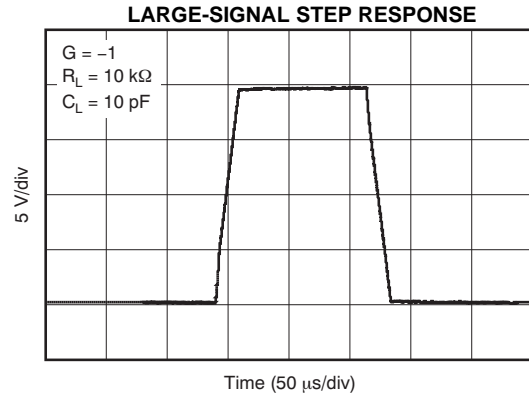


Figure 32.

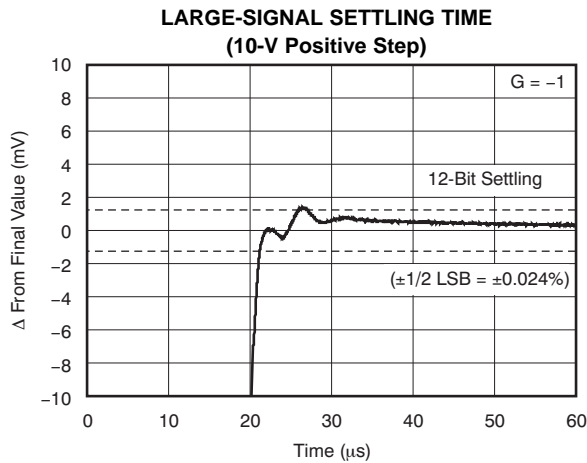


Figure 33.

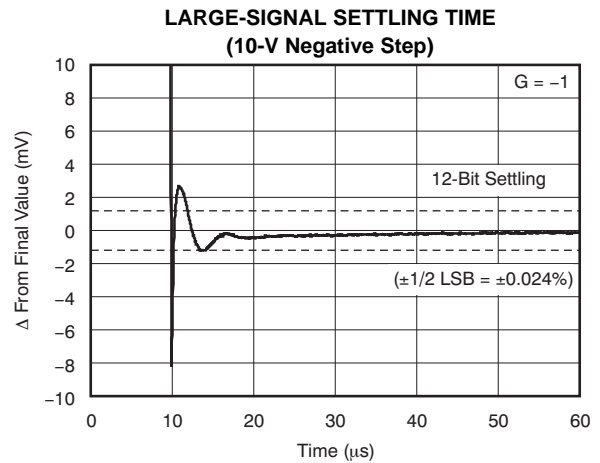


Figure 34.

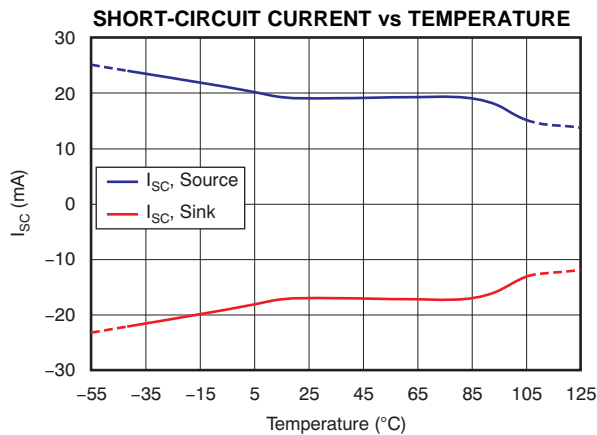


Figure 35.

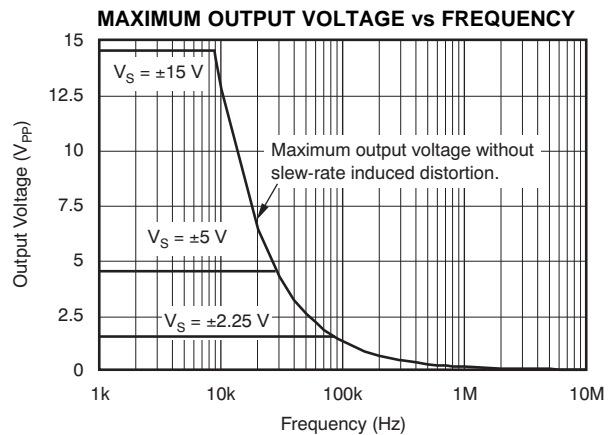


Figure 36.

**TYPICAL CHARACTERISTICS (continued)**

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

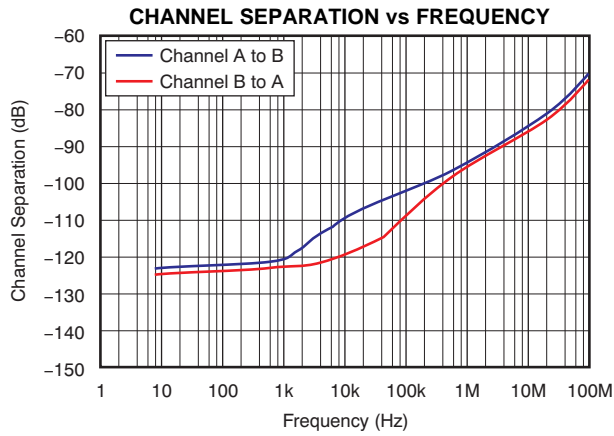


Figure 37.

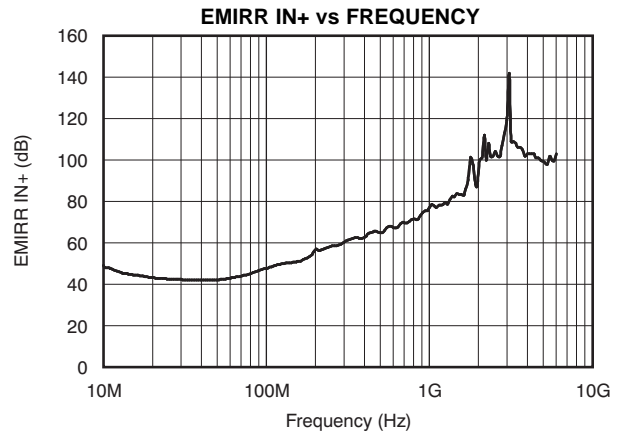


Figure 38.

## APPLICATION INFORMATION

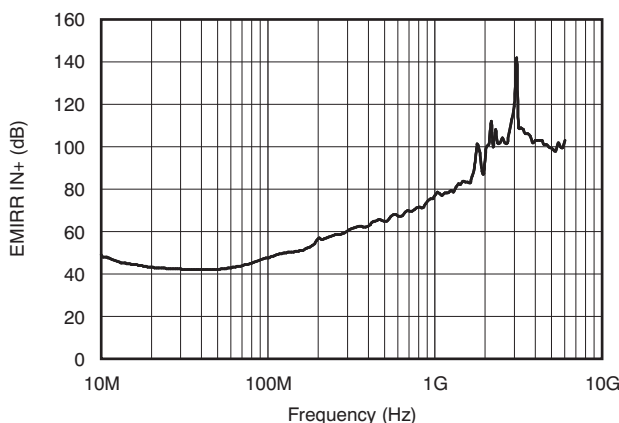
The OPA2188 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085  $\mu\text{V}$  per degree Celsius provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and  $A_{OL}$ . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- $\mu\text{F}$  capacitors are adequate.

### OPERATING CHARACTERISTICS

The OPA2188 is specified for operation from 4 V to 36 V ( $\pm 2$  V to  $\pm 18$  V). Many of the specifications apply from  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### EMI REJECTION

The OPA2188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [Figure 39](#) shows the results of this testing on the OPA2188. Detailed information can also be found in the [Application Report EMI Rejection Ratio of Operational Amplifiers \(SBOA128\)](#), available for download from the TI website.



**Figure 39. EMIRR Testing**

### GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1- $\mu$ F bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

### PHASE-REVERSAL PROTECTION

The OPA2188 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA2188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 40](#).

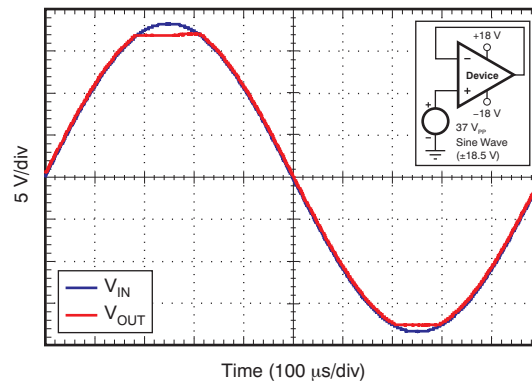


Figure 40. No Phase Reversal

### CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPA2188 have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example,  $R_{OUT}$  equal to 50  $\Omega$ ) in series with the output. [Figure 41](#) and [Figure 42](#) illustrate graphs of small-signal overshoot versus capacitive load for several values of  $R_{OUT}$ . Also, refer to the [Applications Report, Feedback Plots Define Op Amp AC Performance \(SBOA015\)](#), available for download from the TI website, for details of analysis techniques and application circuits.

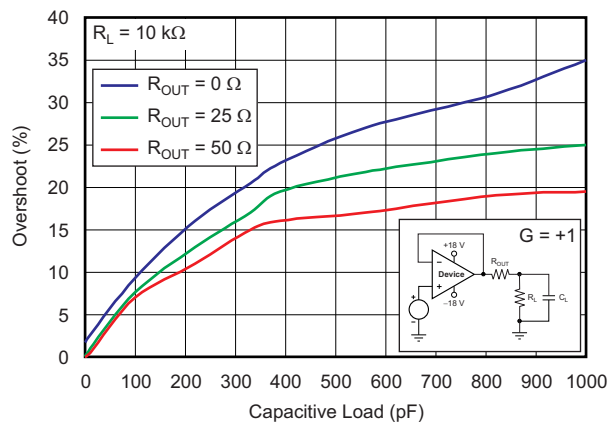


Figure 41. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

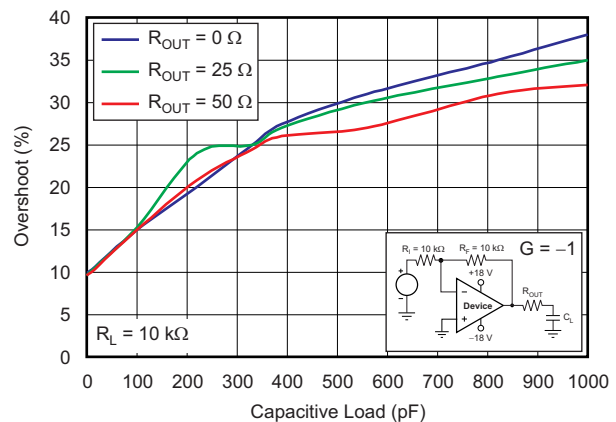
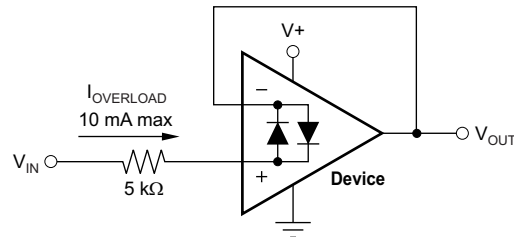


Figure 42. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

## ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#). [Figure 43](#) shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.



**Figure 43. Input Current Protection**

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

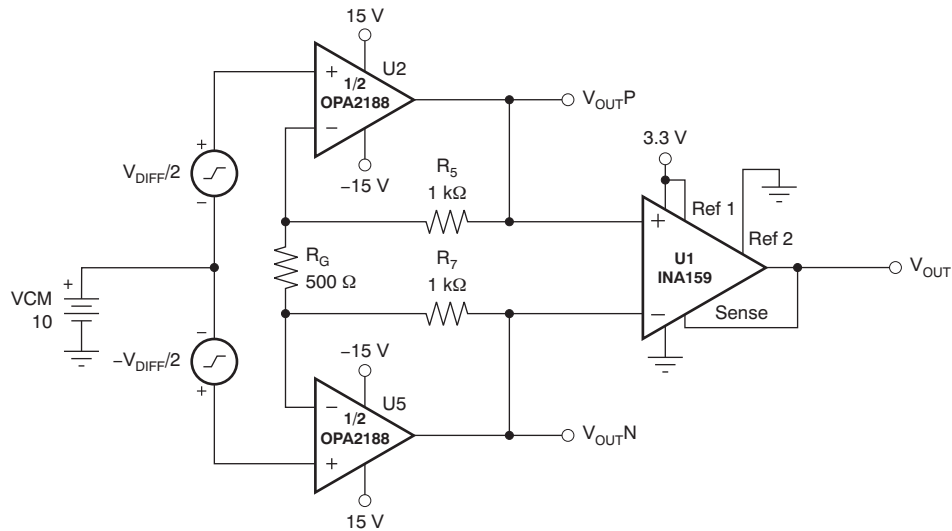
When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

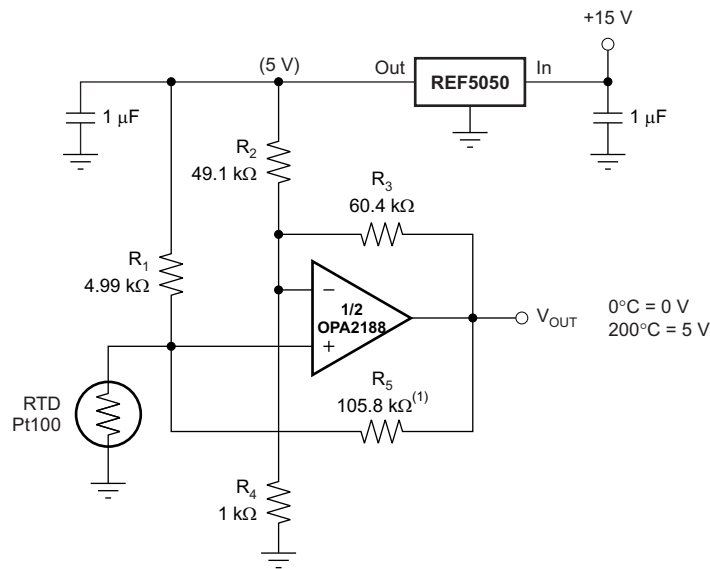
However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

**APPLICATION EXAMPLES**

The application examples of [Figure 44](#) and [Figure 45](#) highlight only a few of the circuits where the OPA2188 can be used.



**Figure 44. Discrete INA + Attenuation for ADC with 3.3-V Supply**



(1) R<sub>5</sub> provides positive-varying excitation to linearize output.

**Figure 45. RTD Amplifier with Linearization**

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**REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (June 2012) to Revision B****Page**

- 
- Changed 倒数第二个应用着重号 ..... 1
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2188AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188 ~ OPA2188)	<a href="#">Samples</a>
OPA2188AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188	<a href="#">Samples</a>
OPA2188AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	2188	<a href="#">Samples</a>
OPA2188AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188 ~ OPA2188)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2188AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2188AIDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
OPA2188AIDGKT	VSSOP	DGK	8	250	202.0	201.0	28.0
OPA2188AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2188AIDR	SOIC	D	8	2500	367.0	367.0	35.0





D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
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微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
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无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道 1568 号, 中建大厦 32 楼 邮政编码: 200122  
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