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Jameco Part Number 1357167



OPA2111

Dual Low Noise Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE:** 100% Tested, $8\text{nV}/\sqrt{\text{Hz}}$ max at 10kHz
- **LOW BIAS CURRENT:** 4pA max
- **LOW OFFSET:** 500 μV max
- **LOW DRIFT:** 2.8 $\mu\text{V}/^\circ\text{C}$
- **HIGH OPEN-LOOP GAIN:** 114dB min
- **HIGH COMMON-MODE REJECTION:** 96dB min

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

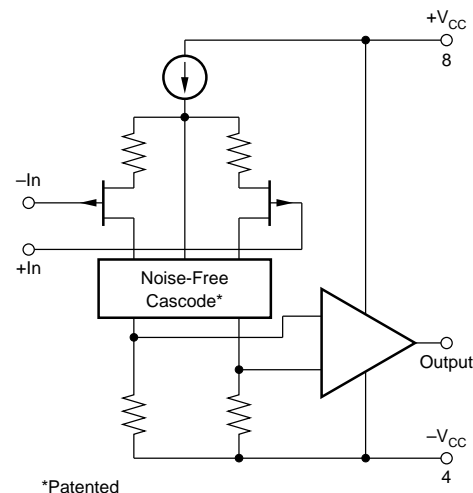
The OPA2111 is a high precision monolithic dielectrically isolated FET (*Difet*) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET[®] amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 Simplified Circuit
(Each Amplifier)

BIFET[®] National Semiconductor Corp., *Difet*[®] Burr-Brown Corp.

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
INPUT NOISE Voltage, $f_o = 10\text{Hz}$ $f_o = 100\text{Hz}$ $f_o = 1\text{kHz}$ $f_o = 10\text{kHz}$ $f_B = 10\text{Hz}$ to 10kHz $f_B = 0.1\text{Hz}$ to 10Hz Current, $f_B = 0.1\text{Hz}$ to 10Hz $f_o = 0.1\text{Hz}$ to 20kHz	100% Tested		40	80		30	60		40	80		40		$\text{nV}/\sqrt{\text{Hz}}$	
	100% Tested		15	40		11	30		15	40		15		$\text{nV}/\sqrt{\text{Hz}}$	
	100% Tested		8	15		7	12		8	15		8		$\text{nV}/\sqrt{\text{Hz}}$	
	(1)		6	8		6	8		6	8		6		$\text{nV}/\sqrt{\text{Hz}}$	
	(1)		0.7	1.2		0.6	1		0.7	1.2		0.7		μVrms	
	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		$\mu\text{Vp-p}$	
	(1)		15	24		12	19		15	24		15		fA p-p	
	(1)		0.8	1.3		0.6	1		0.8	1		0.8		$\text{fA}/\sqrt{\text{Hz}}$	
OFFSET VOLTAGE (2) Input Offset Voltage Average Drift Match Supply Rejection Channel Separation	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}		± 0.1	± 0.75		± 0.05	± 0.5		± 0.1	± 0.75		± 0.3	± 2	mV	
			± 2	± 6		± 0.5	± 2.8		± 2	± 6		± 8	± 15	$\mu\text{V}/^\circ\text{C}$	
		90	± 1		96	± 0.5		90	2		86	2		$\mu\text{V}/^\circ\text{C}$	
			110		110				110		110				dB
	100Hz, $R_L = 2\text{k}\Omega$		± 3	± 31		± 3	± 16		± 3	± 31		± 3	± 50	$\mu\text{V/V}$	
		136		136				136		136		136		dB	
BIAS CURRENT (2) Input Bias Current Match	$V_{CM} = 0\text{VDC}$		± 2	± 8		± 1.2	± 4		± 2	± 8		± 3	± 15	pA	
			± 1			± 0.5			± 1			2		pA	
OFFSET CURRENT (2) Input Offset Current	$V_{CM} = 0\text{VDC}$		± 1.2	± 6		± 0.6	± 3		± 1.2	± 6		± 3	± 12	pA	
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$		$10^{13} \parallel 1$		$10^{13} \parallel 1$		$10^{13} \parallel 1$		$10^{13} \parallel 1$		$10^{13} \parallel 1$	$\Omega \parallel \text{pF}$	
			$10^{14} \parallel 3$		$10^{14} \parallel 3$		$10^{14} \parallel 3$		$10^{14} \parallel 3$		$10^{14} \parallel 3$		$10^{14} \parallel 3$	$\Omega \parallel \text{pF}$	
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10	± 11		± 10	± 11		± 10	± 11		± 10	± 11		V	
		90	110		96	110		90	110		82	110		dB	
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Match	$R_L \geq 2\text{k}\Omega$	110	125		114	125		110	125		106	125		dB	
			3			2			3			3		dB	
FREQUENCY RESPONSE Unity Gain, Small Signal Full Power Response Slew Rate Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive(3)	20Vp-p, $R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$ Gain = -1, $R_L = 2\text{k}\Omega$ 10V Step Gain = -1		2		2		2		2		2		2	MHz	
		16	32		16	32		16	32		32		32	kHz	
		1	2		1	2		1	2		2		2	V/ μs	
			6			6			6		6		6		μs
			10			10			10		10		10		μs
			5			5			5		5		5		μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ DC, Open-Loop Gain = +1	± 10	± 11		± 10	± 11		± 10	± 11		± 10	± 11		V	
		± 5	± 10		± 5	± 10		± 5	± 10		± 5	± 10		mA	
			100			100			100			100			Ω
			1000			1000			1000			1000			pF
		10	40		10	40		10	40		10	40		40	mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0\text{mADC}$		± 15		± 15		± 15		± 15		± 15		± 15	VDC	
		± 5		± 18	± 5		± 18	± 5		± 18	± 5		± 18	VDC	
			5	7		5	7		5	7		5	9	mA	
TEMPERATURE RANGE Specification Operating "M" Package "P" Package Storage "M" Package "P" Package θ Junction-Ambient	Ambient Temp.	-25		+85	-25		+85	-55		+125	0		+70	$^\circ\text{C}$	
		-55		+125	-55		+125	-55		+125	-55		+125	$^\circ\text{C}$	
											-40			+85	$^\circ\text{C}$
		-65		+150	-65		+150	-65		+150	-65		+150	$^\circ\text{C}$	
											-40			+85	$^\circ\text{C}$
		200				200			200			200(4)			$^\circ\text{C/W}$

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical $\theta_{JA} = 150^\circ\text{C/W}$ for plastic DIP.

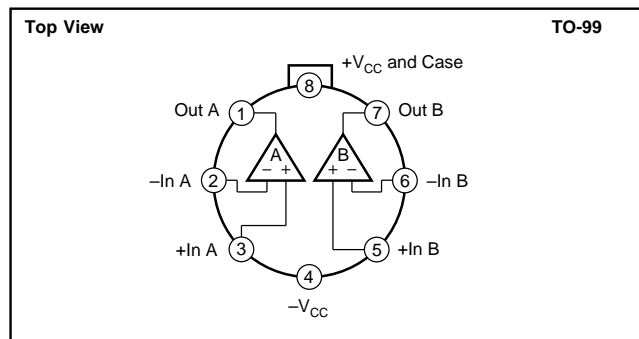
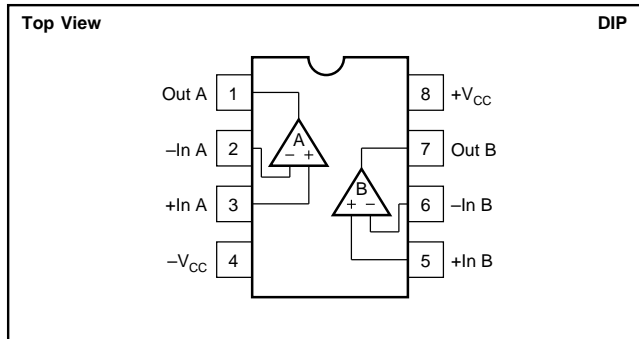
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range	Ambient Temp.	-25		+85	-25		+85	-55		+125	0		+70	°C
INPUT OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Match Supply Rejection	$V_{CM} = 0\text{VDC}$		± 0.22 ± 2 1 86	± 1.2 ± 6 1 ± 10		± 0.08 ± 0.5 0.5 90	± 0.75 ± 2.8 0.5 ± 10		± 0.3 ± 2 2 86	± 1.5 ± 6 2 ± 10		± 0.9 ± 8 2 ± 10	± 5 ± 15 2 ± 80	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V}/\text{V}$
BIAS CURRENT⁽¹⁾ Input Bias Current Match	$V_{CM} = 0\text{VDC}$		± 125 60	$\pm 1\text{nA}$		± 75 30	± 500		$\pm 2\text{nA}$ 1nA	$\pm 16.3\text{nA}$		± 125 ± 500	pA pA	
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		± 75	± 750		± 38	± 375		$\pm 1.3\text{nA}$	$\pm 12\text{nA}$		± 75 ± 375	pA	
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10 86	± 11 100		± 10 90	± 11 100		± 10 86	± 11 100		± 10 80	± 11 100	V dB	
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Match	$R_L \geq 2\text{k}\Omega$	106	120 5		110	120 3		106	120 5		100	120 5	dB dB	
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 10.5 ± 5 10	± 11 ± 10 40		± 10.5 ± 5 10	± 11 ± 10 40		± 10.5 ± 5 10	± 11 ± 10 40		± 10.5 ± 5 10	± 11 ± 10 40	V mA mA	
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		5 8		5 8	8		5 8	8		5 10	10	mA	

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18\text{VDC}$
Internal Power Dissipation ($T_J \leq +175^\circ\text{C}$)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	$\pm V_{CC}$
Storage Temperature Range: "M" Package	-65°C to $+150^\circ\text{C}$
"P" Package	-40°C to $+85^\circ\text{C}$
Operating Temperature Range: "M" Package	-55°C to $+125^\circ\text{C}$
"P" Package	-40°C to $+85^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Output Short Circuit to Ground ($+25^\circ\text{C}$)	Continuous
Junction Temperature	$+175^\circ\text{C}$

PACKAGE INFORMATION

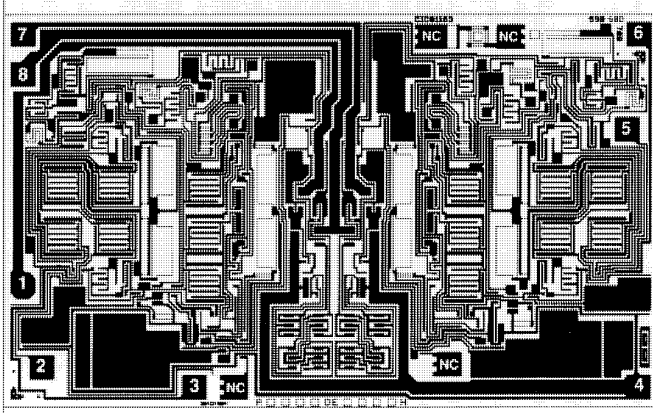
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA2111AM	TO-99	001
OPA2111BM	TO-99	001
OPA2111KM	TO-99	001
OPA2111SM	TO-99	001
OPA2111KP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, max (mV)
OPA2111AM	TO-99	-25°C to $+85^\circ\text{C}$	± 0.75
OPA2111BM	TO-99	-25°C to $+85^\circ\text{C}$	± 0.5
OPA2111KM	TO-99	0°C to $+70^\circ\text{C}$	± 2
OPA2111SM	TO-99	-55°C to $+125^\circ\text{C}$	± 0.75
OPA2111KP	8-Pin Plastic DIP	0°C to $+70^\circ\text{C}$	± 2

DICE INFORMATION



OPA2111AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Out A
2	-In A
3	+In A
4	-V _S
5	+In B
6	-In B
7	Out B
8	+V _S
NC	No Connection

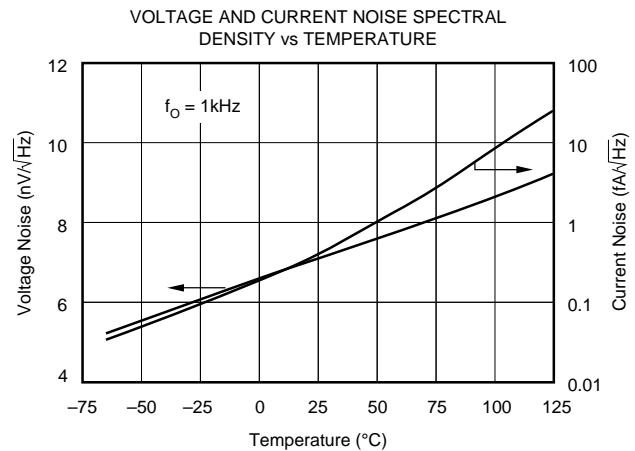
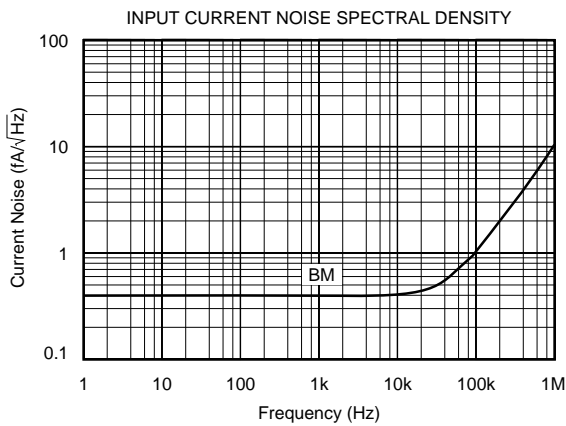
Substrate Bias: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	138 x 84 ±5	3.51 x 2.13 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		102

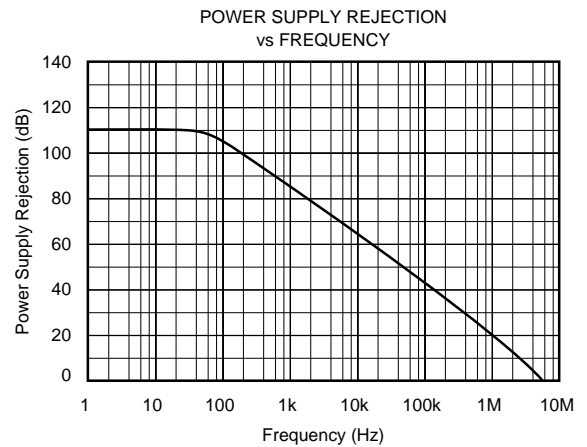
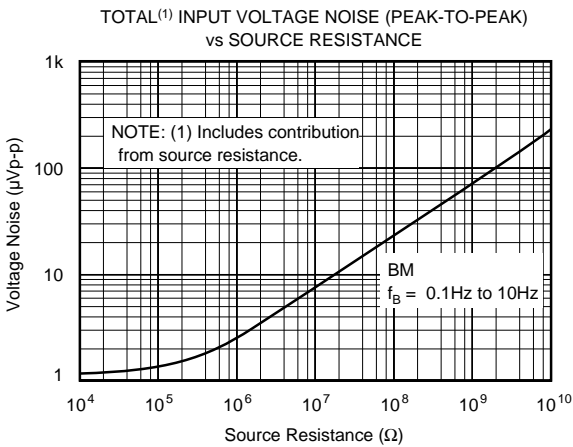
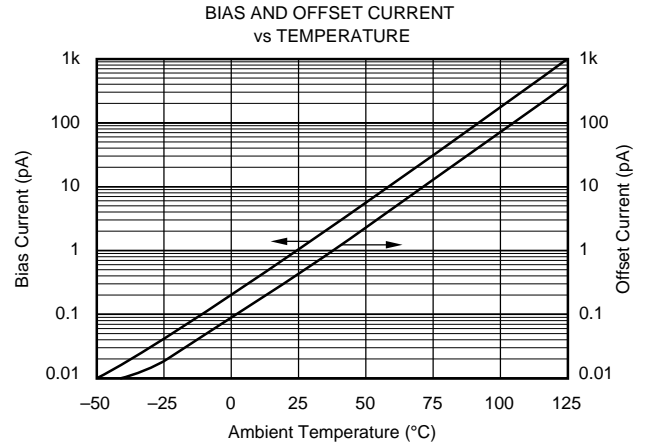
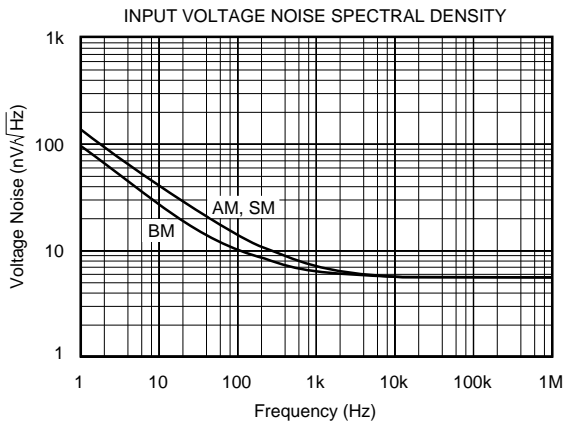
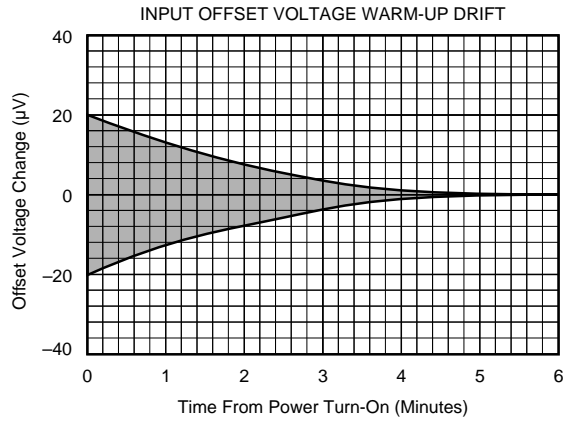
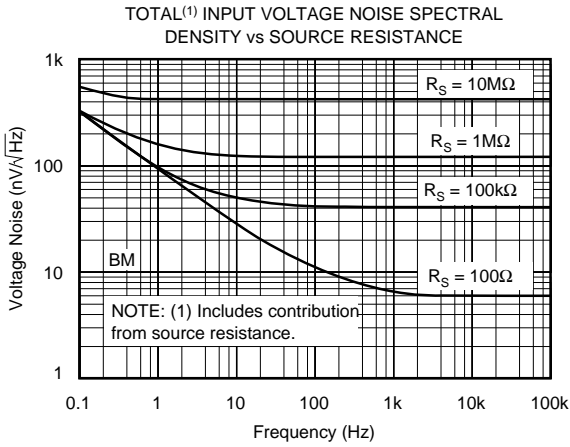
TYPICAL PERFORMANCE CURVES

T_A = +25°C, and V_{CC} = ±15VDC unless otherwise noted.



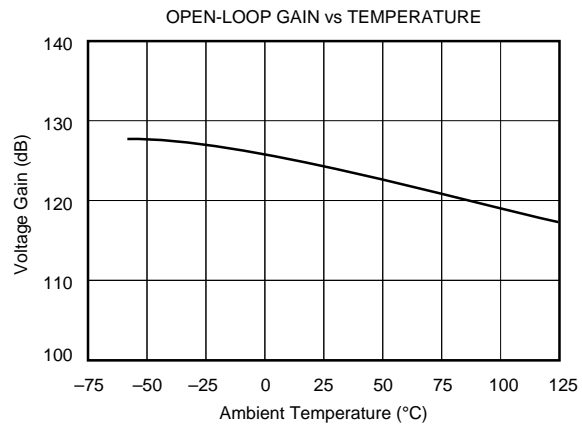
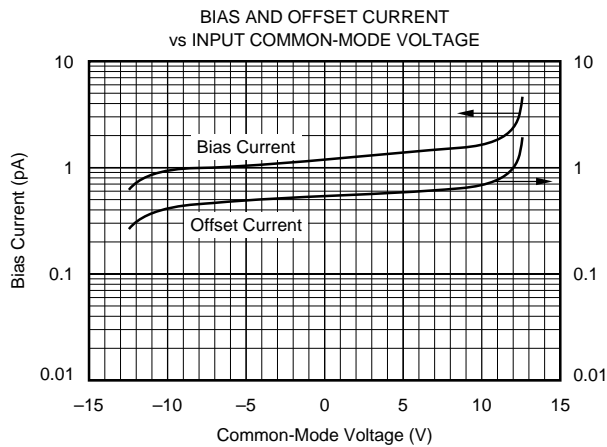
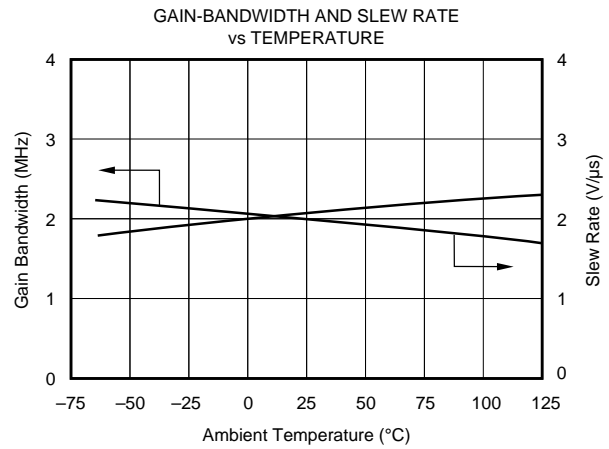
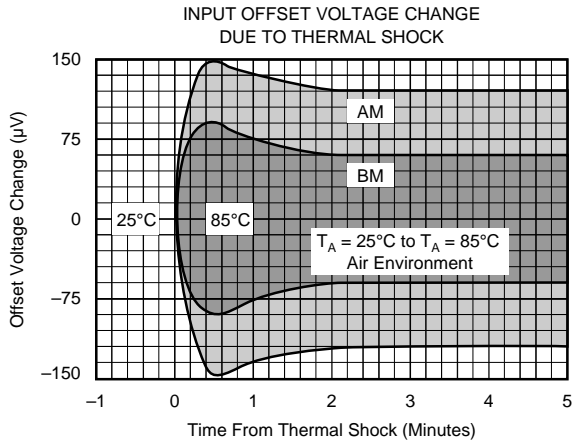
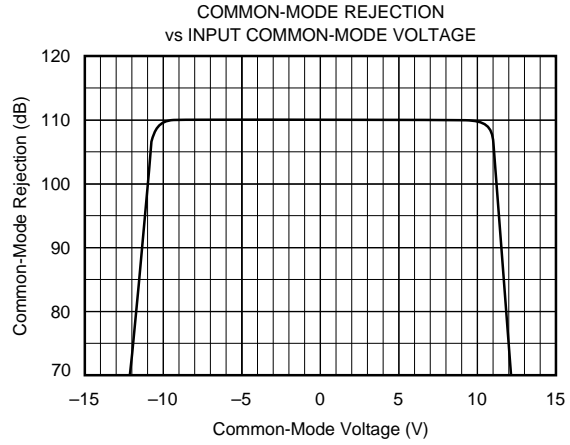
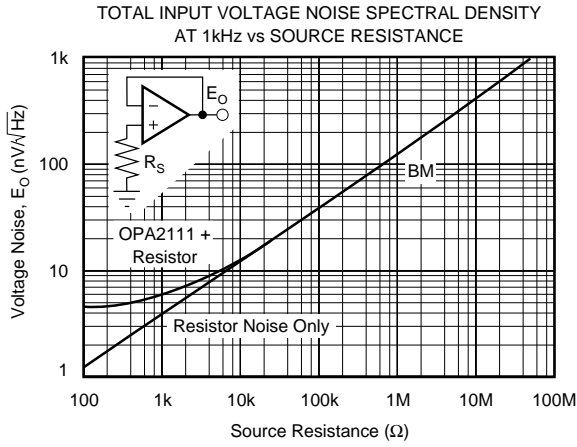
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, and $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



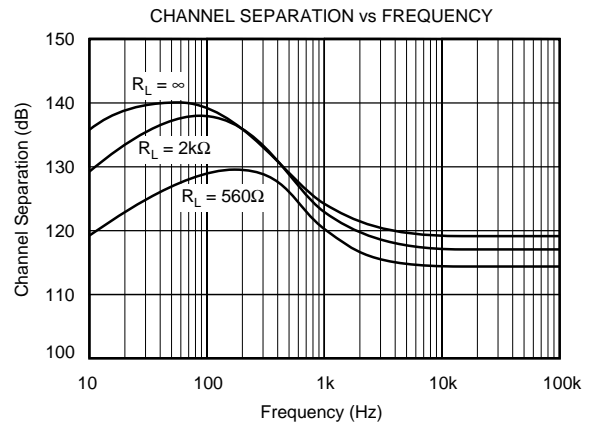
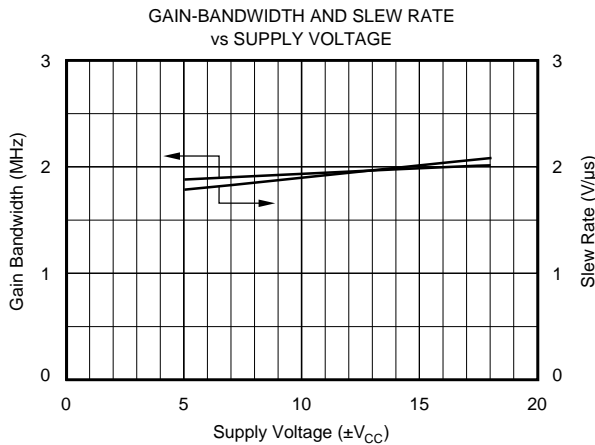
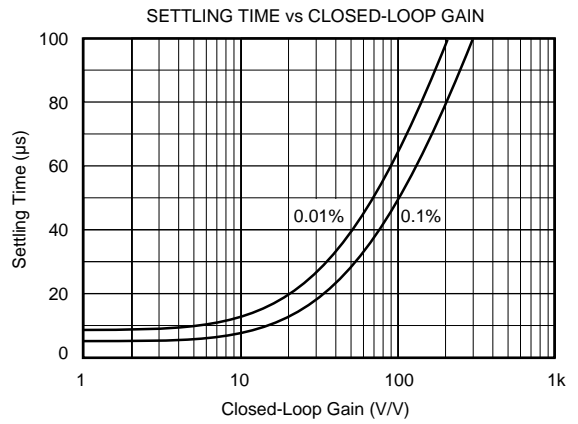
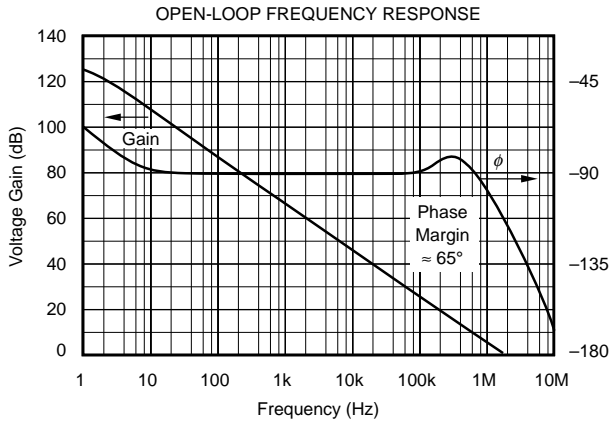
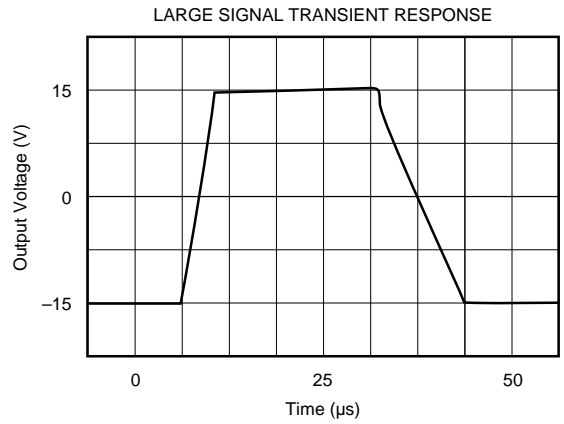
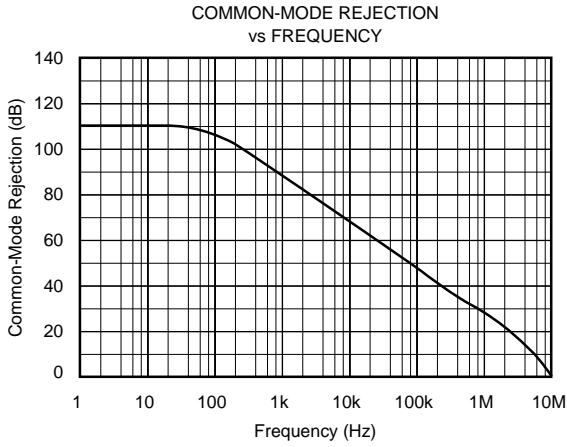
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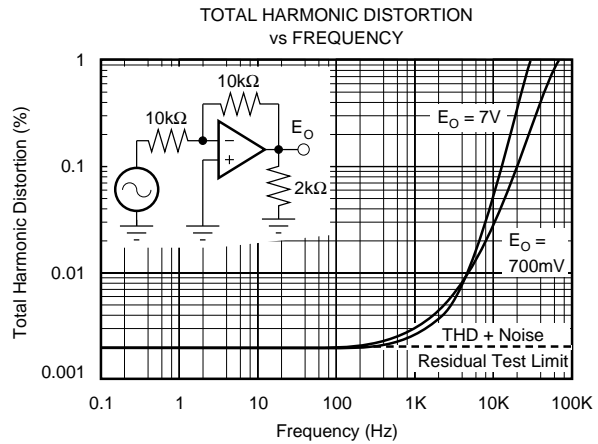
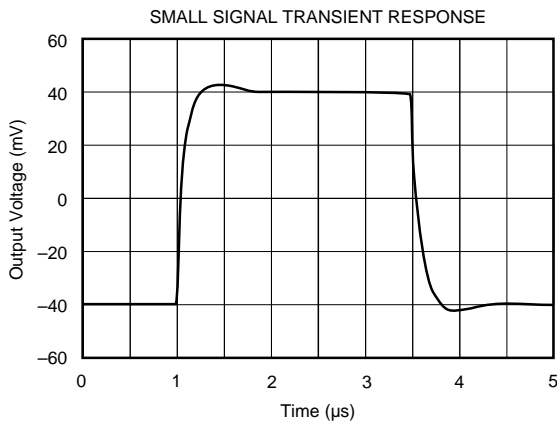
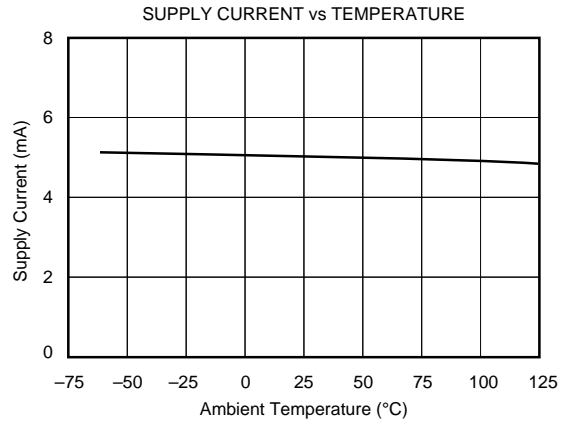
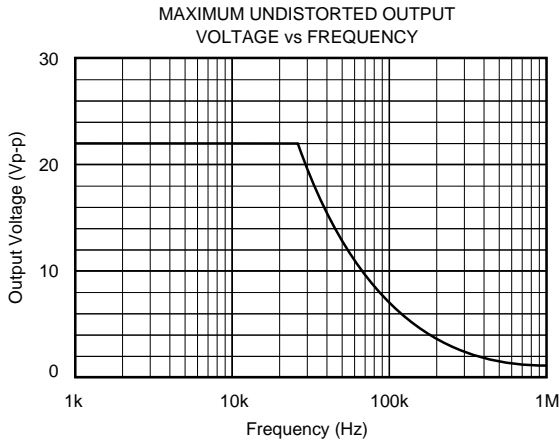
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

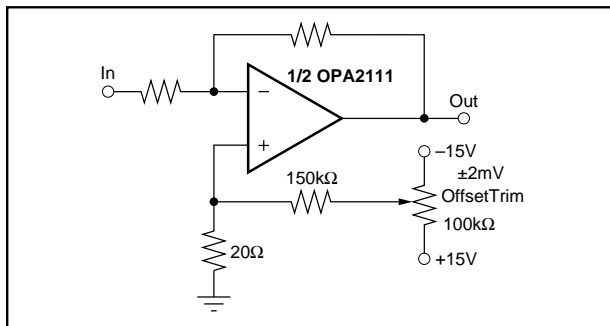


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA2111. Of course, the differential and common-mode voltage limits should be observed. Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET vs BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

BIAS CURRENT CHANGE vs COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA2111 is not compromised by common-mode voltage.

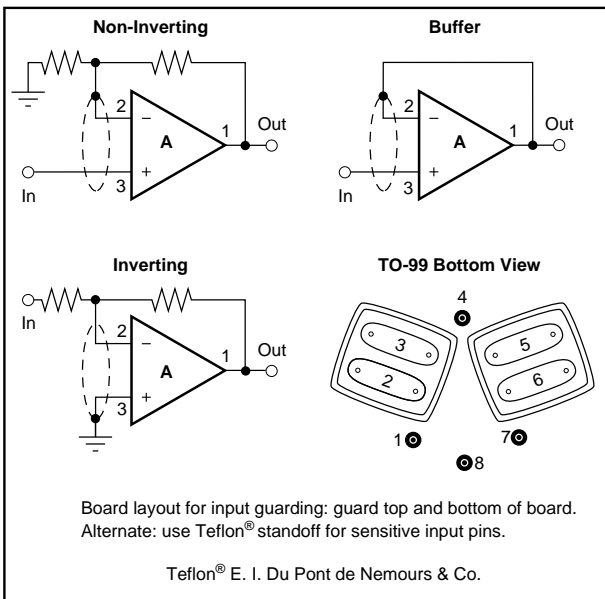


FIGURE 2. Connection of Input Guard.

APPLICATIONS CIRCUITS

Figures 5 through 13 are circuit diagrams of various applications for the OPA2111.

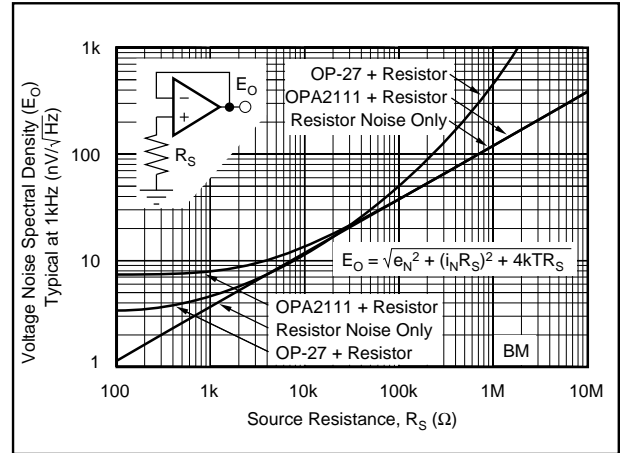


FIGURE 3. Voltage Noise Spectral Density vs Source Resistance.

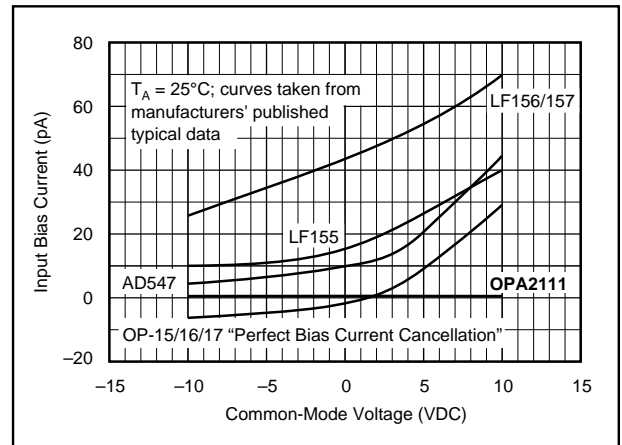


FIGURE 4. Input Bias Current vs Common-Mode Voltage.

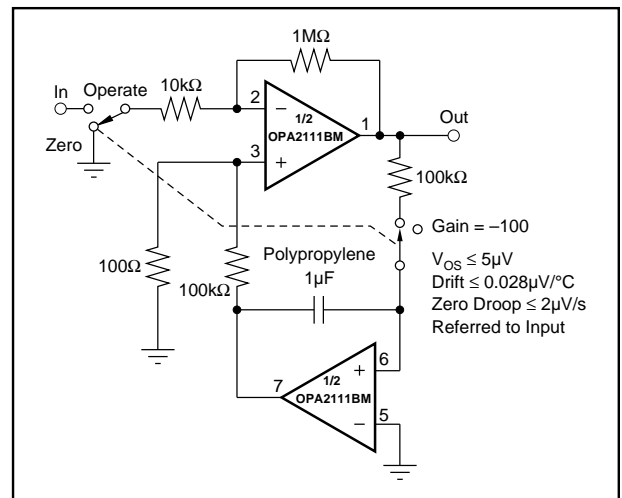


FIGURE 5. Auto-Zero Amplifier.

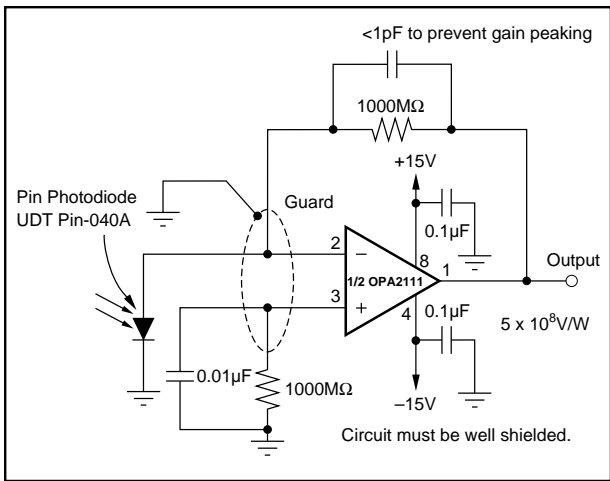


FIGURE 6. Sensitive Photodiode Amplifier.

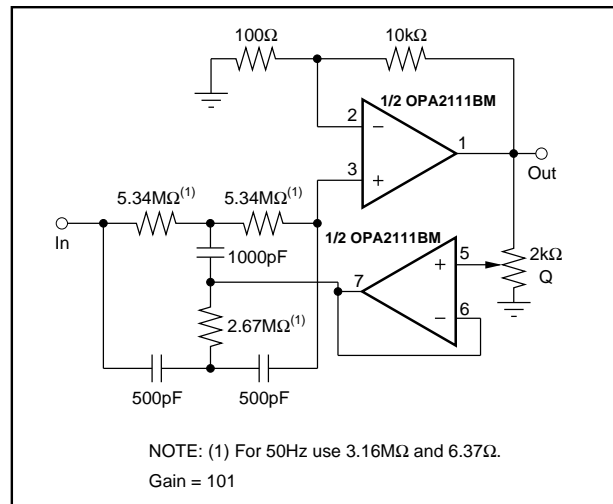


FIGURE 7. High Impedance 60Hz Reject Filter with Gain.

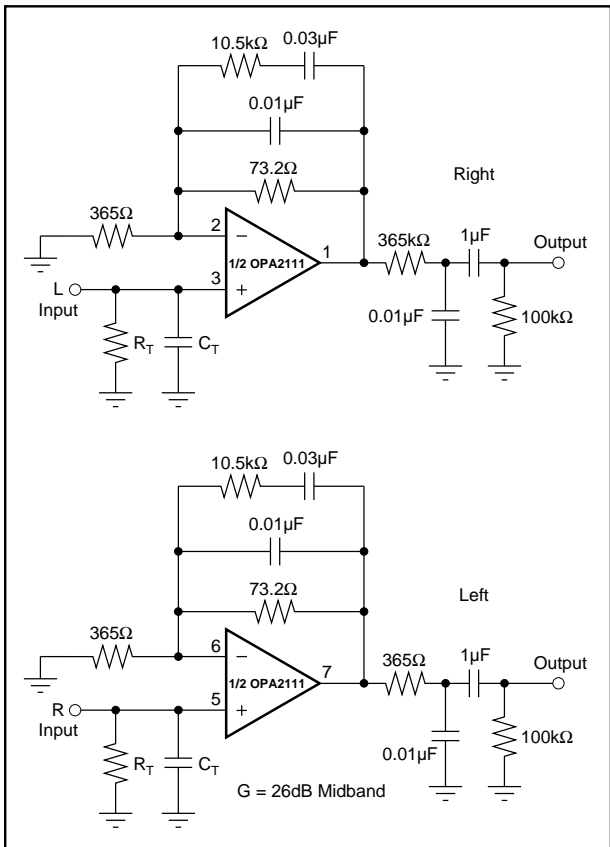


FIGURE 8. RIAA Equalized Stereo Preamplifier.

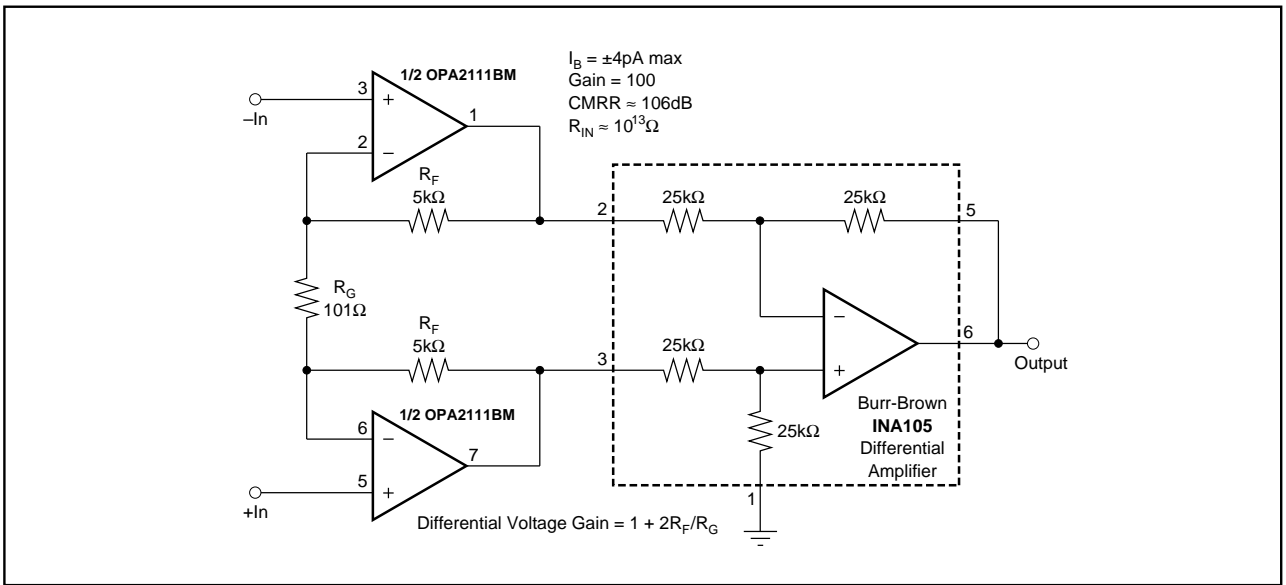


FIGURE 9. FET Input Instrumentation Amplifier.

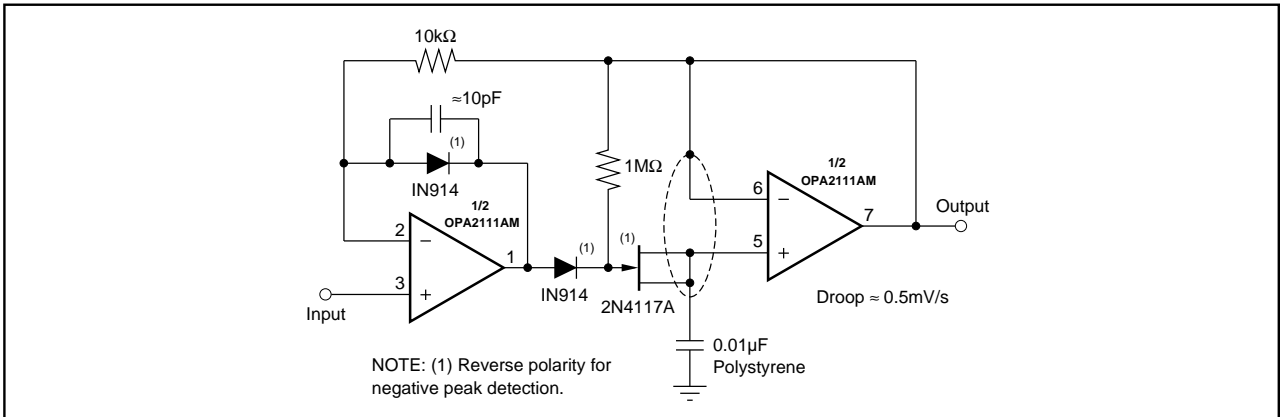


FIGURE 10. Low-Droop Positive Peak Detector.

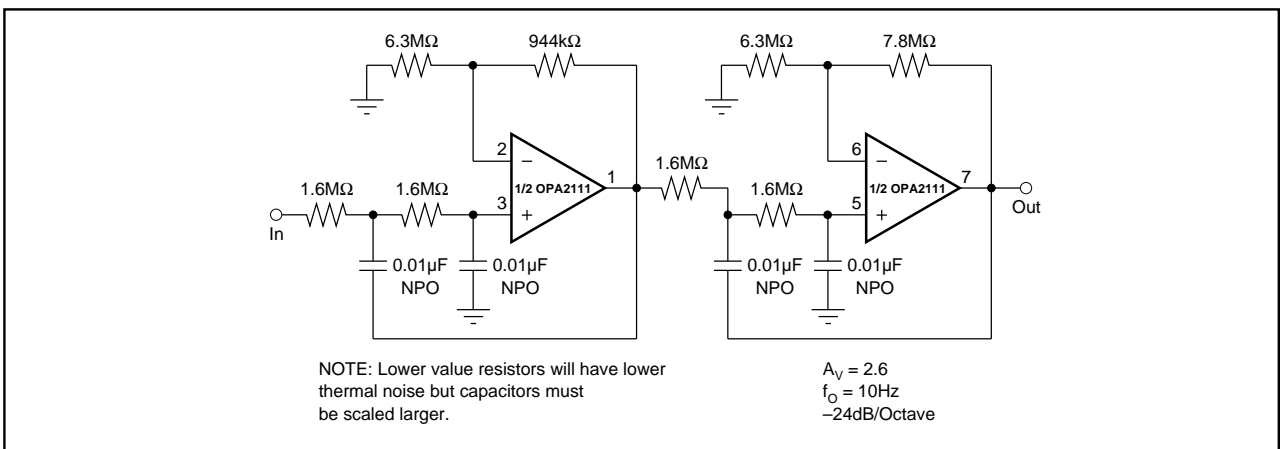


FIGURE 11. 10Hz Fourth-Order Butterworth Low-Pass Filter.

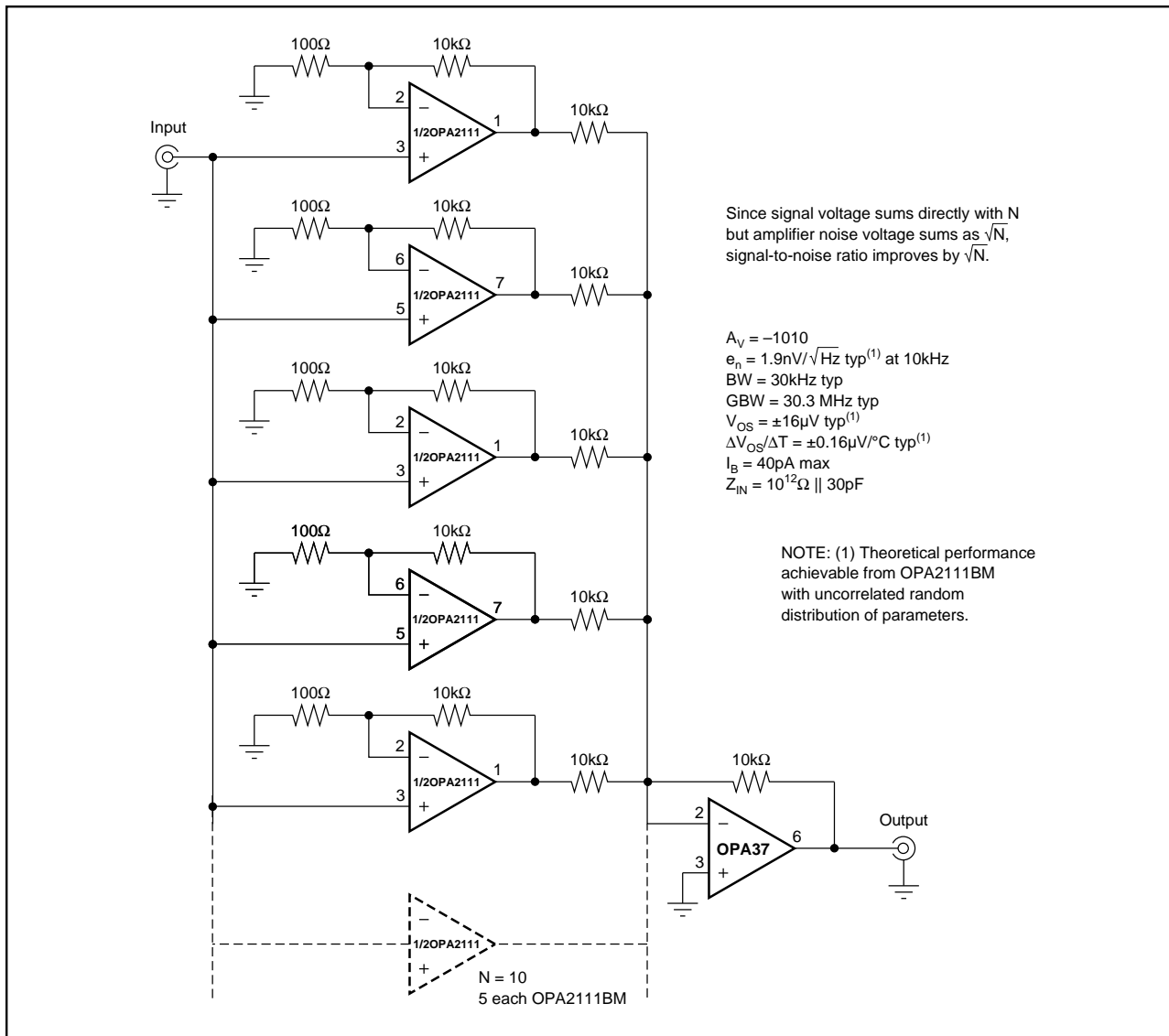


FIGURE 12. 'N' Stage Parallel-Input Amplifier.

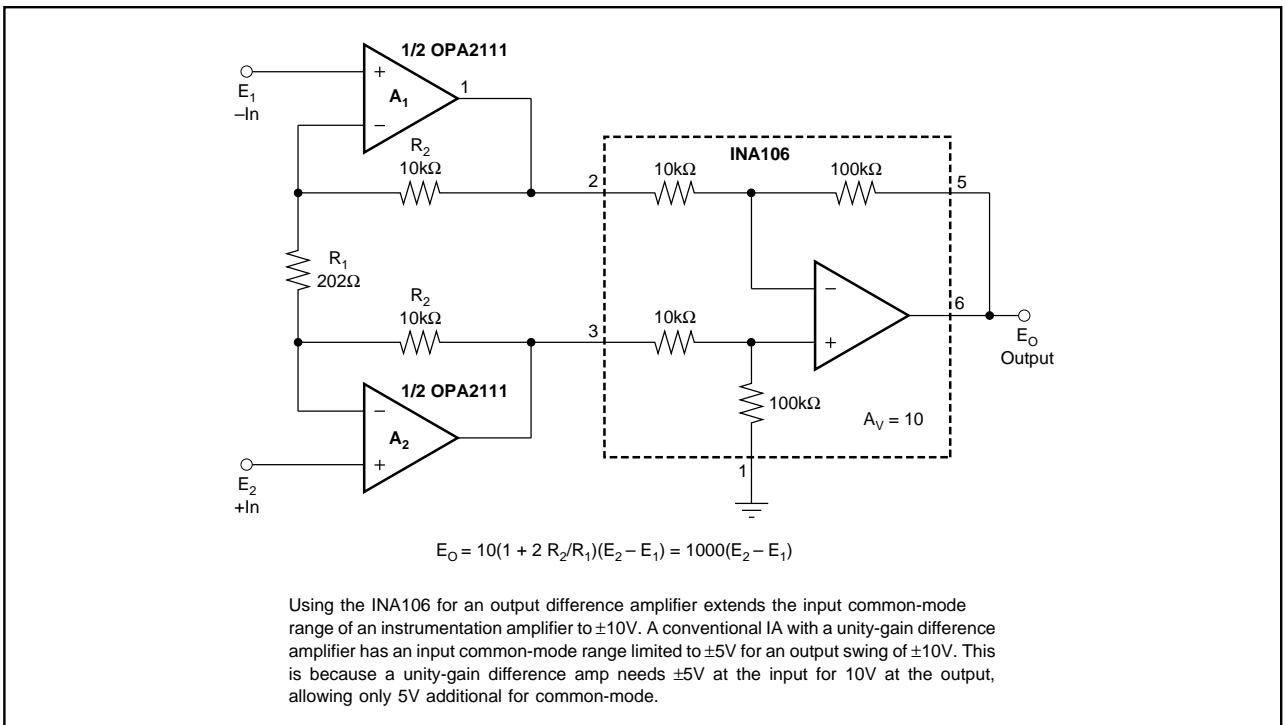


FIGURE 13. Precision Instrumentation Amplifier.

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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA2111AM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA2111BM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA2111KM	NRND	TO-99	LMC	8	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
OPA2111KP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2111KPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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