OPA188 高精度、低噪声、轨到轨输出、36V、零漂移运算放大器

1 特性

- 低偏移电压：25μV（最大值）
- 零漂移：0.03μV/°C
- 低噪声：8.8 nV/√Hz
  - 0.1Hz 至 10Hz 噪声：0.25μV_{PP}
- 出色的 DC 精度：
  - 电源抑制比 (PSRR)：142dB
  - 共模抑制比 (CMRR)：146dB
  - 开环路增益：136dB
- 增益带宽：2MHz
- 静态电流：510μA（最大值）
- 宽电源电压：±2V 至 ±18V
- 轨至轨输出
- 输入包括负电源轨
- 已过滤射频干扰 (RFI) 的输入
- *Micro*SIZE 封装

2 应用范围

- 桥式放大器
- 应力计
- 传感器 应用
- 温度测量
- 电子称
- 医疗仪表
- 电阻温度检测器

3 说明

OPA188 运算放大器使用德州仪器 (TI) 拥有自主知识产权的自动归零技术来提供低偏移电压（25μV，最大值），以及时间和温度范围的接近零漂移。这个微型、高精度、低静态电流放大器提供高输入阻抗和摆幅为电源轨 15mV 之内的轨到轨输出。输入共模范围包括负电源轨。单电源或者双电源可在 +4V 至 +36V（±2V 至 ±18V）的范围内使用。

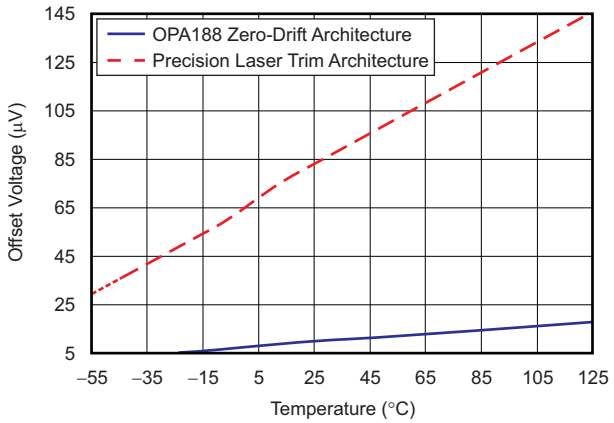
单通道版本采用微型尺寸小外形晶体管 (SOT)23-5，微型小外形尺寸 (MSOP)-8 和小外形尺寸 (SO)-8 封装。所有器件版本的额定工作温度范围均为 -40°C 至 +125°C。

器件信息(1)

产品型号	封装	封装尺寸（标称值）
OPA188	SOIC (8)	4.90mm x 3.91mm
	SOT-23 (5)	2.90mm x 1.60mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

采用自动调零技术实现超低温度漂移



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2013) to Revision B **Page**

- Deleted Package Information table; all information now available in the package option addendum at the end of the data sheet ... 3
- Changed *input bias current* maximum value for over-temperature test condition in Electrical Characteristics ... 5
- Changed *input offset current* maximum value for over-temperature test condition in Electrical Characteristics ... 5
- Changed *quiescent current* values in Electrical Characteristics ... 5
- Changed *input bias current* maximum value for over-temperature test condition in Electrical Characteristics ... 6
- Changed *input offset current* maximum value for over-temperature test condition in Electrical Characteristics ... 6
- Changed *quiescent current* maximum values in Electrical Characteristics ... 6

Changes from Original (March 2013) to Revision A **Page**

- 已添加器件信息，器件比较，ESD 额定值和建议运行条件表，*详细 说明*, *应用 和实施*，*电源相关建议*，*布局*，*器件和文档支持*以及*机械、封装和可订购信息*部分 ... 1
- 已将文档状态更改为量产数据 ... 1

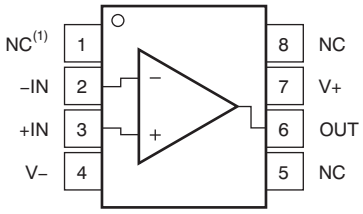
5 Device Comparison Table

Zero-Drift Amplifier Portfolio

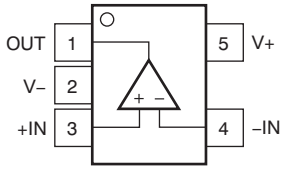
VERSION	PRODUCT	OFFSET VOLTAGE (μV, max)	OFFSET VOLTAGE DRIFT (μV/°C, max)	BANDWIDTH (MHz)	INPUT VOLTAGE NOISE (μV_{PP}, f = 0.1 Hz to 10 Hz)
Single	OPA188 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA333 (5 V)	±10	±0.05	0.35	1.1
	OPA378 (5 V)	±50	±0.25	0.9	0.4
	OPA735 (12 V)	±5	±0.05	1.6	2.5
Dual	OPA2188 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA2333 (5 V)	±10	±0.05	0.35	1.1
	OPA2378 (5 V)	±50	±0.25	0.9	0.4
	OPA2735 (12 V)	±5	±0.05	1.6	2.5
Quad	OPA4188 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA4330 (5 V)	±50	±0.25	0.35	1.1

6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



DBV Package
5-Pin SOT-23
Top View



(1) NC = no connection.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D, DGK	DBV		
+IN	3	3	I	Noninverting input
–IN	2	4	I	Inverting input
OUT	6	1	O	Output
NC	1, 5, 8	—	—	No internal connection (can be left floating)
V+	7	5	—	Positive (highest) power supply
V–	4	2	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply	Split supply		±20	V
		Single supply		40	
	Signal input pins(2)		(V–) – 0.5	(V+) + 0.5	
		Differential		±0.7	
Current	Signal input pins(2)			±10	mA
	Output short-circuit(3)		Continuous		
Temperature	Operating(4), T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, V-, or V+.
(4) Provided device does not exceed maximum junction temperature (T_J) at any time.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Operating voltage range	Split supply	±2		±18	V
		Single supply	4		36	
T_A	Specified temperature range		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA188			UNIT
		D (SO)	DBV (SOT23)	DGK (MSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.0	158.8	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.5	60.7	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	44.8	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.7	1.6	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.8	44.2	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: High-Voltage Operation

at T_A = +25°C, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V), R_L = 10 kΩ connected to V_S / 2[1], and V_{CM} = V_{OUT} = V_S / 2[1] (unless otherwise noted)

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±6	±25	µV
			T_A = –40°C to +125°C		±0.03	±0.085	µV/°C
PSRR	Power-supply rejection ratio		V_S = 4 V to 36 V, T_A = –40°C to +125°C		±0.075	±0.3	µV/V
	Long-term stability[2]				4		µV
INPUT BIAS CURRENT							
I_B	Input bias current		V_{CM} = V_S / 2		±160	±1400	pA
			T_A = –40°C to +125°C			±18	nA
I_{OS}	Input offset current				±320	±2800	pA
			T_A = –40°C to +125°C			±6	nA
NOISE							
e_n	Input voltage noise		f = 0.1 Hz to 10 Hz		250		nV_{PP}
			f = 0.1 Hz to 10 Hz		40		nVrms
	Input voltage noise density		f = 1 kHz		8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density		f = 1 kHz		7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to +125°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio		(V–) < V_{CM} < (V+) – 1.5 V	120	134		dB
			(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V	130	146		dB
			(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V, T_A = –40°C to +125°C	120	126		dB
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 6		MΩ || pF
Z_{IC}	Common-mode				6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		(V–) + 0.5 V < V_O < (V+) – 0.5 V	130	136		dB
			(V–) + 0.5 V < V_O < (V+) – 0.5 V, T_A = –40°C to +125°C	120	126		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				2		MHz
SR	Slew rate		G = +1		0.8		V/µs
t_S	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		20		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		27		µs
t_{OR}	Overload recovery time		V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise		1 kHz, G = 1, V_{OUT} = 1 Vrms		0.0001%		
OUTPUT							
	Voltage output swing from rail		No load		6	15	mV
			R_L = 10 kΩ		220	250	mV
			T_A = –40°C to +125°C		310	350	mV
I_{SC}	Short-circuit current		Sinking		–18		mA
			Sourcing		16		mA
R_O	Open-loop output resistance		f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive				1		nF
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)		V_S = ±4 V to V_S = ±18 V		450	510	µA
			I_O = 0 mA, T_A = –40°C to +125°C			600	µA

(1) V_S / 2 = midsupply.
(2) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

7.6 Electrical Characteristics: Low-Voltage Operation

at T_A = 25°C, V_S = ±2 V to < ±4 V (V_S = 4 V to < 8 V), R_L = 10 kΩ connected to V_S / 2 (1), and V_{CM} = V_{OUT} = V_S / 2 (1) (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±6	±25	μV
		T_A = –40°C to +125°C		±0.03	±0.085	μV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, T_A = –40°C to +125°C		0.075	0.3	μV/V
	Long-term stability (2)			4		μV
INPUT BIAS CURRENT						
I_B	Input bias current			±160	±1400	pA
		T_A = –40°C to +125°C			±18	nA
I_{OS}	Input offset current			±320	±2800	pA
		T_A = –40°C to +125°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		250		nV_{PP}
		f = 0.1 Hz to 10 Hz		40		nVrms
	Input voltage noise density	f = 1 kHz		8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V	114	120		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V, T_A = –40°C to +125°C	110	120		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			100 || 6		MΩ || pF
Z_{IC}	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 5 kΩ	110	120		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V	120	130		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, T_A = –40°C to +125°C	110	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/μs
t_{OR}	Overload recovery time	V_{IN} × G = V_S		1		μs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 Vrms		0.0001%		
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		T_A = –40°C to +125°C		310	350	mV
I_{SC}	Short-circuit current	Sinking		–18		mA
		Sourcing		16		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		425	485	μA
		I_O = 0 mA, T_A = –40°C to +125°C			575	μA

(1) V_S / 2 = midsupply.
(2) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 μV.

7.7 Typical Characteristics

表 1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3
Offset Voltage vs Common-Mode Voltage	图 4, 图 5
Offset Voltage vs Power Supply	图 6
Open-Loop Gain and Phase vs Frequency	图 7
Closed-Loop Gain vs Frequency	图 8
I_B and I_{OS} vs Common-Mode Voltage	图 9
Input Bias Current vs Temperature	图 10
Output Voltage Swing vs Output Current (Maximum Supply)	图 11
CMRR and PSRR vs Frequency (Referred-to-Input)	图 12
CMRR vs Temperature	图 13, 图 14
PSRR vs Temperature	图 15
0.1-Hz to 10-Hz Noise	图 16
Input Voltage Noise Spectral Density vs Frequency	图 17
THD+N Ratio vs Frequency	图 18
THD+N vs Output Amplitude	图 19
Quiescent Current vs Supply Voltage	图 20
Quiescent Current vs Temperature	图 21
Open-Loop Gain vs Temperature	图 22
Open-Loop Output Impedance vs Frequency	图 23
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 24, 图 25
No Phase Reversal	图 26
Positive Overload Recovery	图 27
Negative Overload Recovery	图 28
Small-Signal Step Response (100 mV)	图 29, 图 30
Large-Signal Step Response	图 31, 图 32
Large-Signal Settling Time (10-V Positive Step)	图 33
Large-Signal Settling Time (10-V Negative Step)	图 34
Short-Circuit Current vs Temperature	图 35
Maximum Output Voltage vs Frequency	图 36
EMIRR IN+ vs Frequency	图 37

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

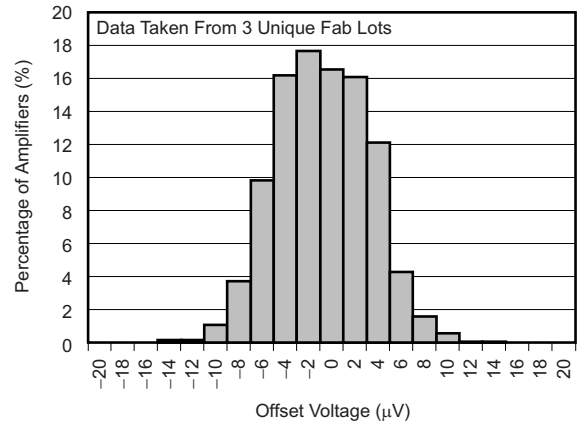


图 1. Offset Voltage Production Distribution

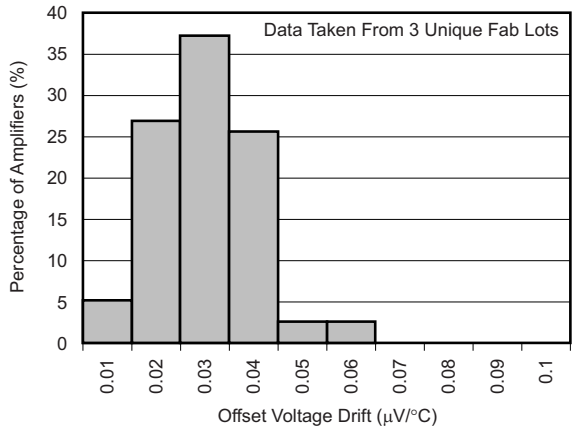


图 2. Offset Voltage Drift Distribution

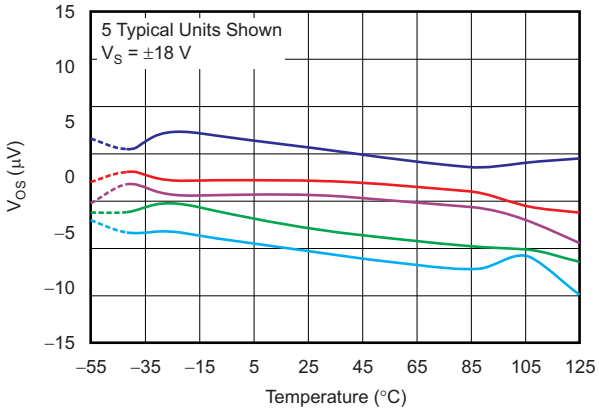


图 3. Offset Voltage vs Temperature

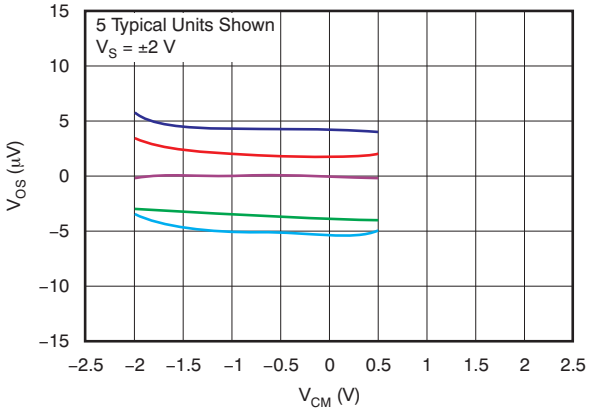


图 4. Offset Voltage vs Common-Mode Voltage

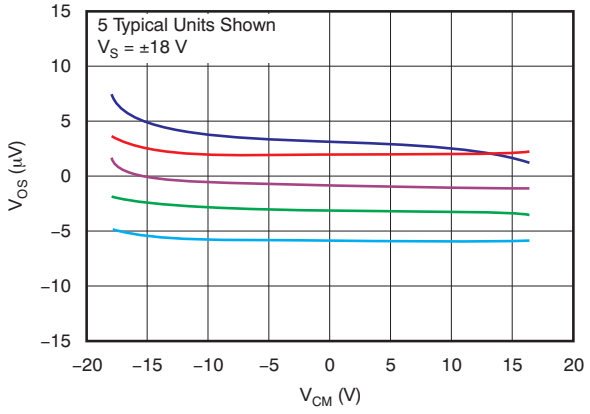


图 5. Offset Voltage vs Common-Mode Voltage

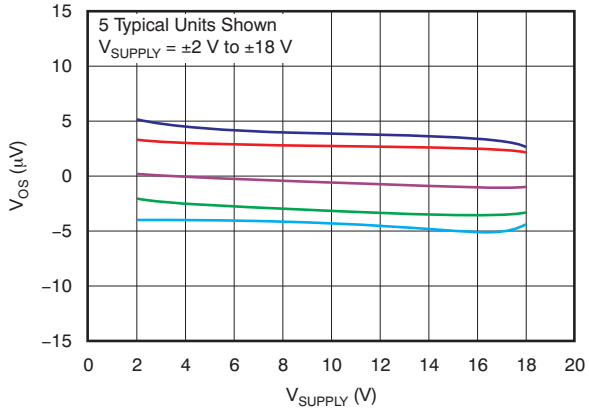


图 6. Offset Voltage vs Power Supply

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

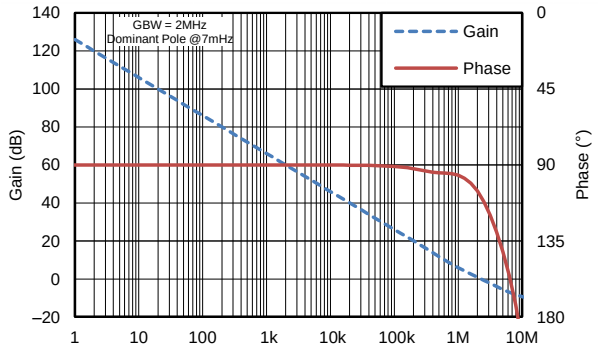


图 7. Open-Loop Gain and Phase vs Frequency

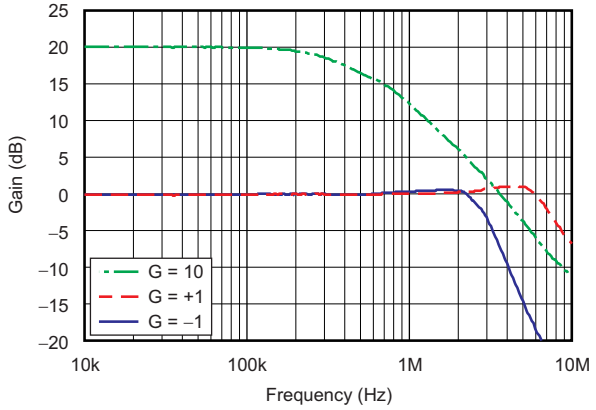


图 8. Closed-Loop Gain vs Frequency

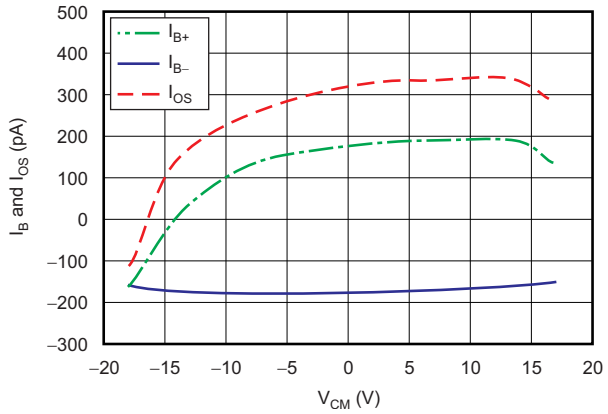


图 9. I_B and I_{OS} vs Common-Mode Voltage

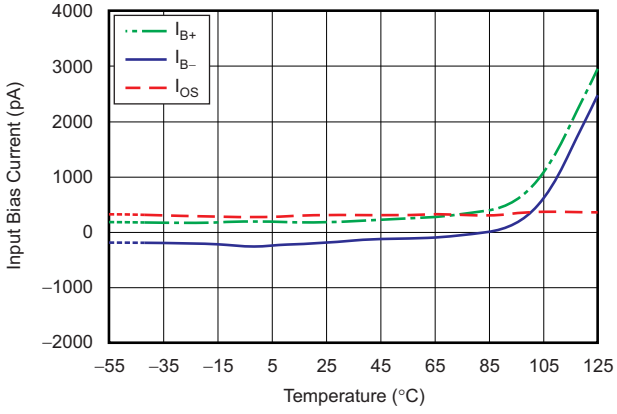


图 10. Input Bias Current vs Temperature

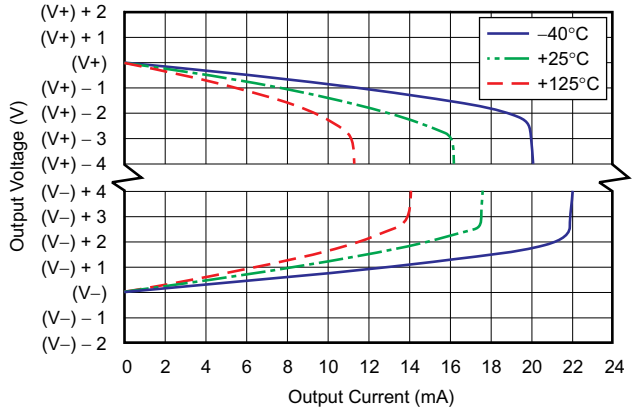


图 11. Output Voltage Swing vs Output Current (Maximum Supply)

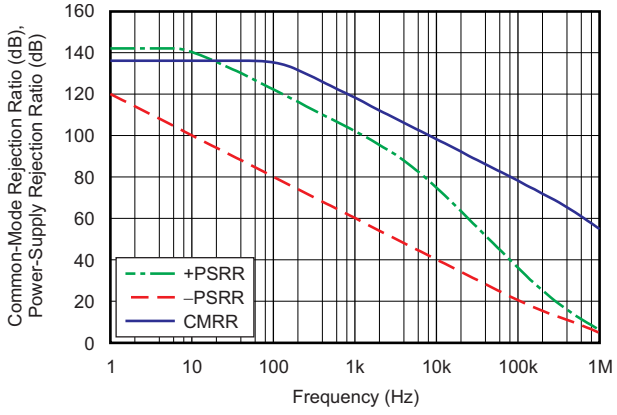


图 12. CMRR and PSRR vs Frequency (Referred-to-Input)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

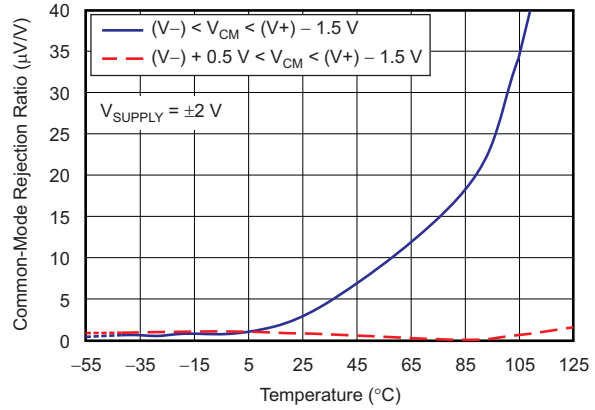


图 13. CMRR vs Temperature

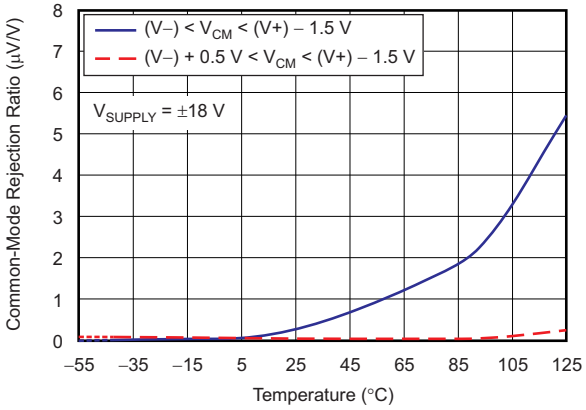


图 14. CMRR vs Temperature

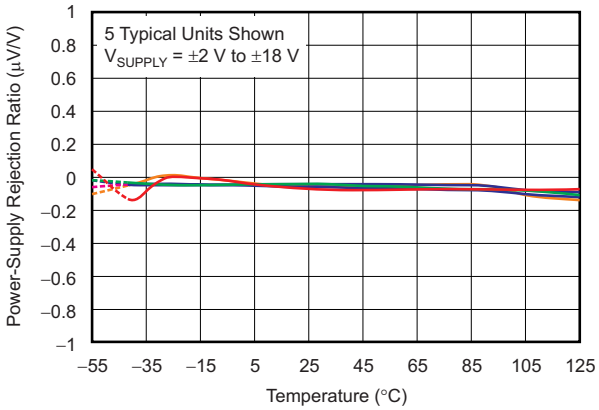


图 15. PSRR vs Temperature

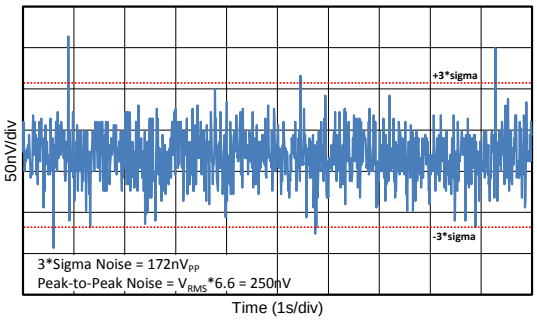


图 16. 0.1-Hz to 10-Hz Noise

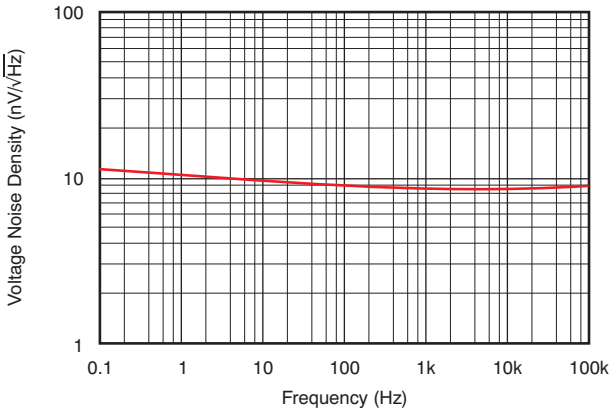


图 17. Input Voltage Noise Spectral Density vs Frequency

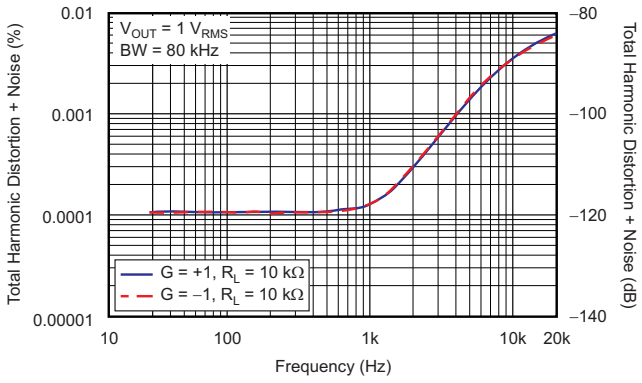


图 18. THD+N Ratio vs Frequency

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

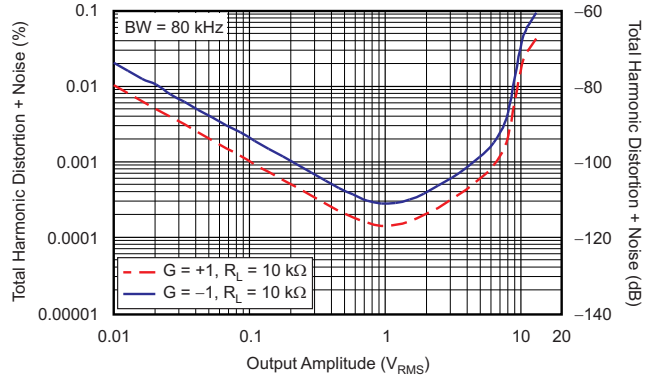


图 19. THD+N vs Output Amplitude

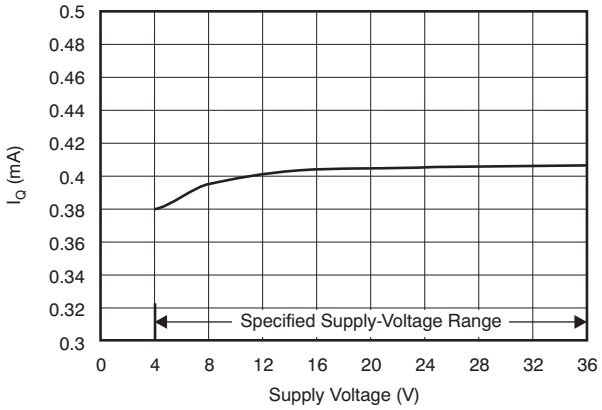


图 20. Quiescent Current vs Supply Voltage

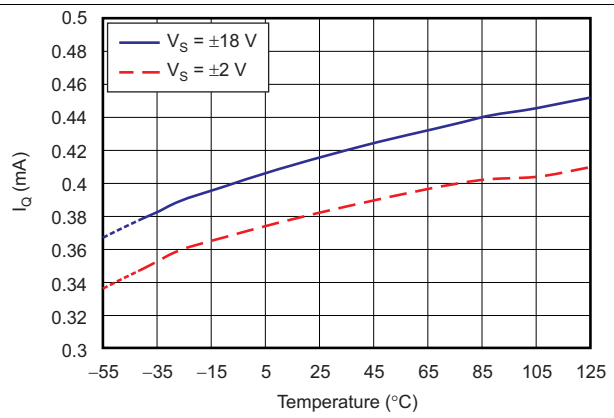


图 21. Quiescent Current vs Temperature

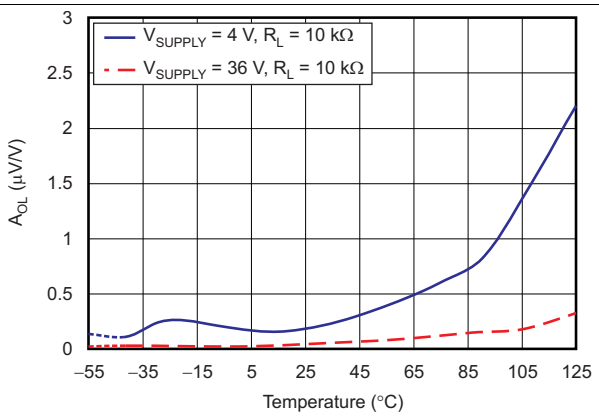


图 22. Open-Loop Gain vs Temperature

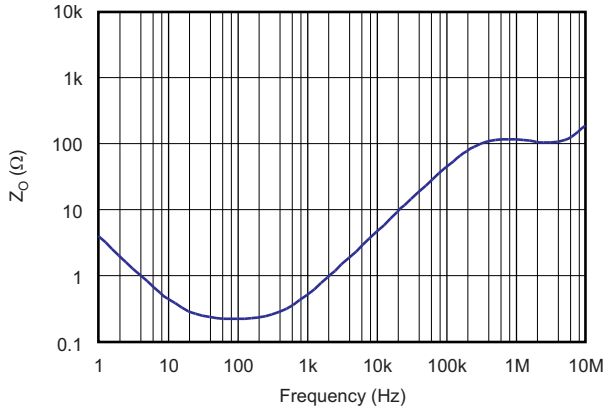


图 23. Open-Loop Output Impedance vs Frequency

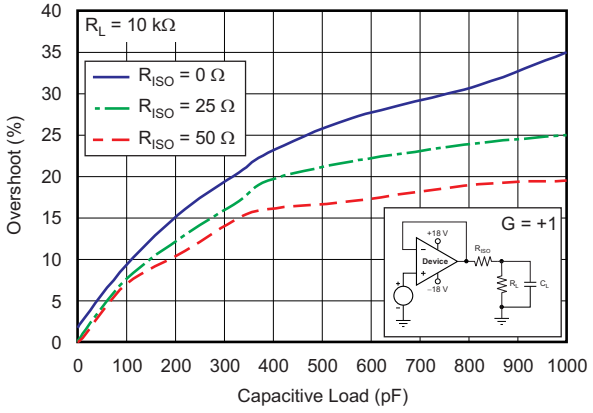


图 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

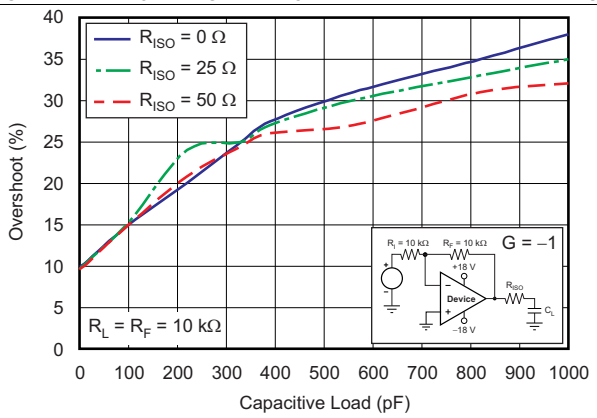


图 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

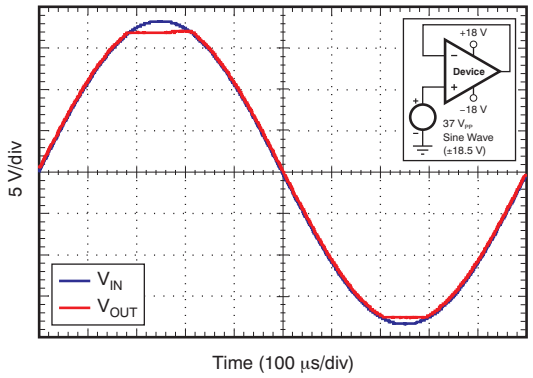


图 26. No Phase Reversal

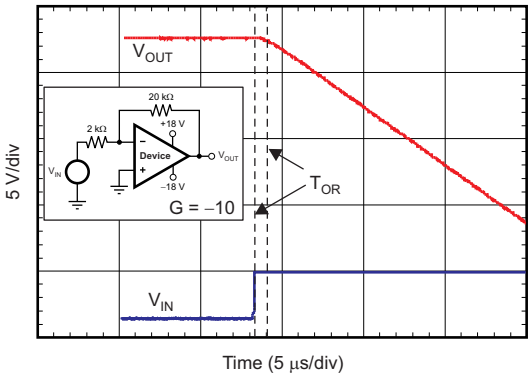


图 27. Positive Overload Recovery

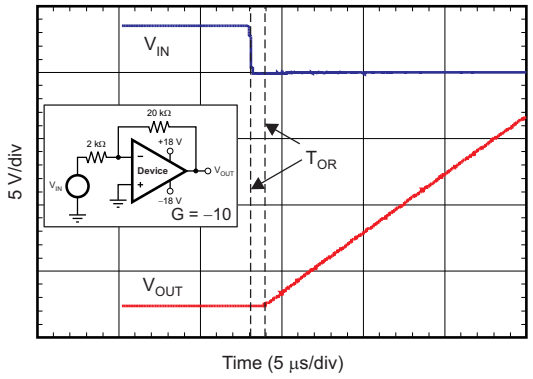


图 28. Negative Overload Recovery

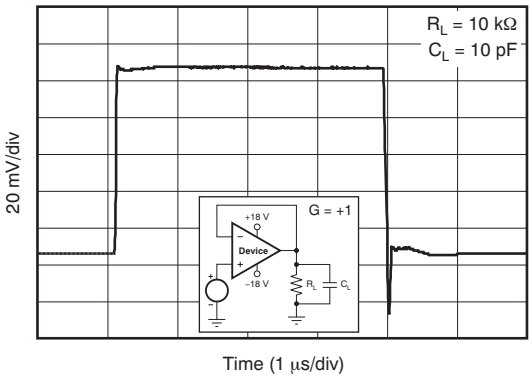


图 29. Small-Signal Step Response (100 mV)

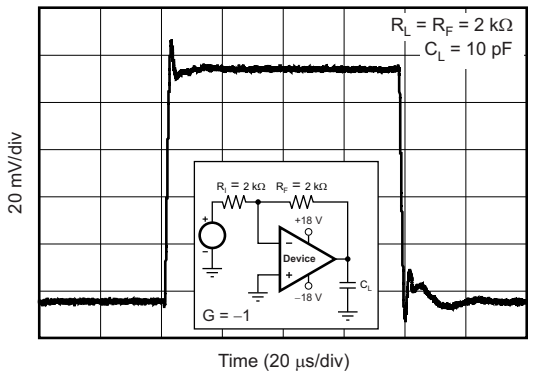


图 30. Small-Signal Step Response (100 mV)

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

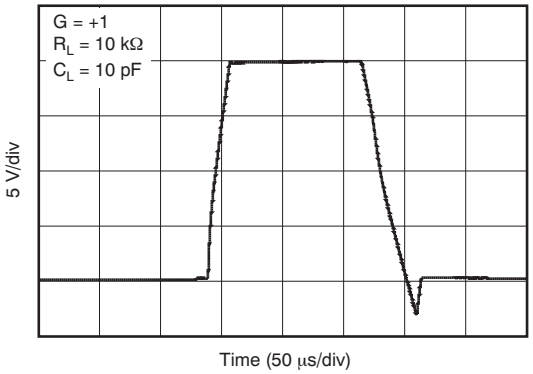


图 31. Large-Signal Step Response

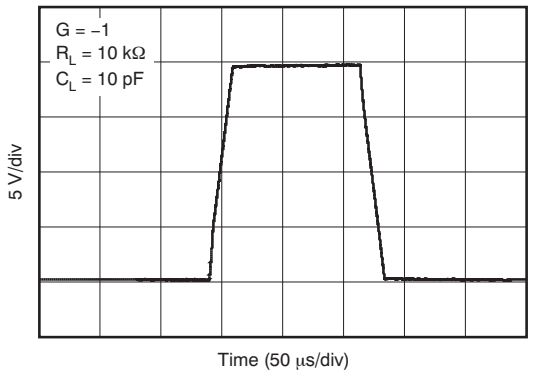


图 32. Large-Signal Step Response

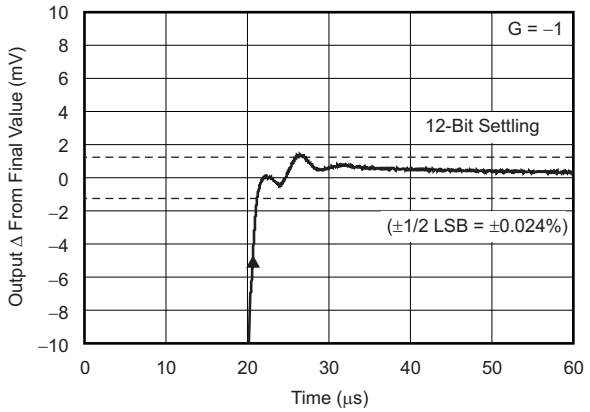


图 33. Large-Signal Settling Time (10-V Positive Step)

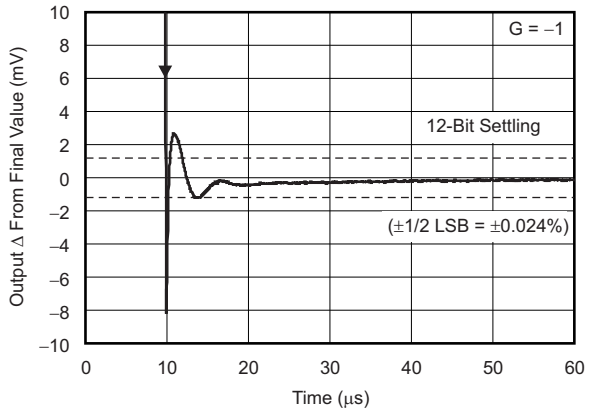


图 34. Large-Signal Settling Time (10-V Negative Step)

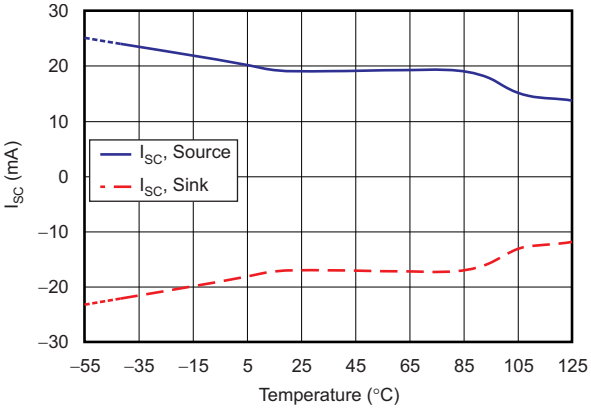


图 35. Short-Circuit Current vs Temperature

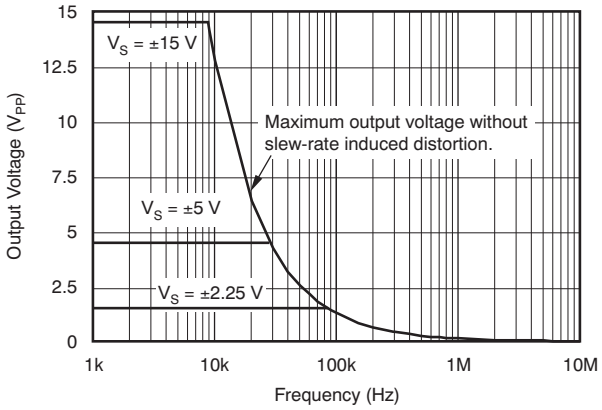


图 36. Maximum Output Voltage vs Frequency

at V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

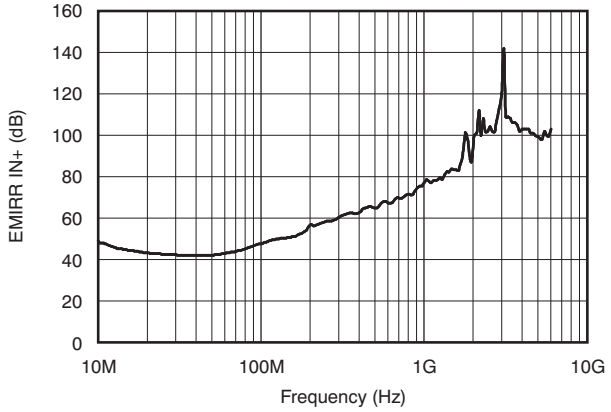


图 37. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPA188 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, this device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The OPA188 is part of a family of zero-drift, low-power, rail-to-rail output operational amplifiers. These devices operate from 4 V to 36 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The zero-drift architecture provides ultralow input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultralow broadband noise and zero flicker noise.

8.2 Functional Block Diagram

图 38 shows a representation of the proprietary OPA188 architecture. 表 2 contains both the active and passive component count for this device. The component count allows for accurate reliability calculations.

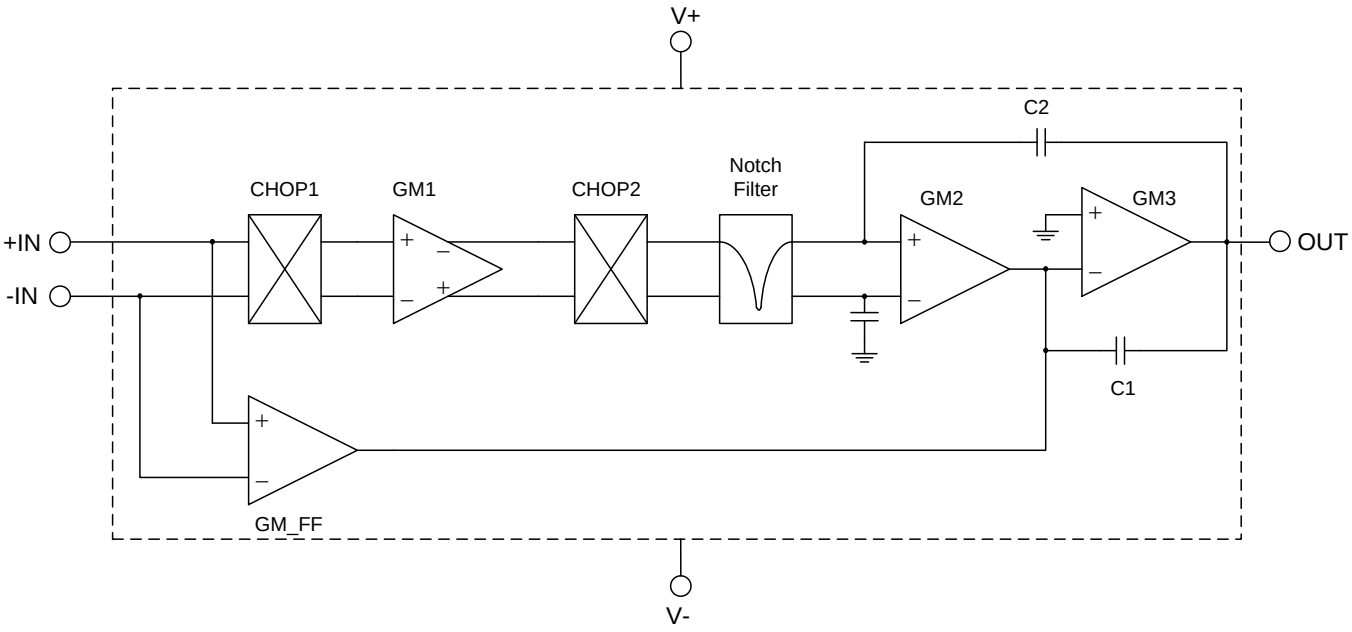


图 38. Functional Block Diagram

表 2. Component Count

COMPONENT	COUNT
Transistors	636
Diodes	5
Resistors	41
Capacitors	72

8.3 Feature Description

The OPA188 is unity-gain stable and free from unexpected output phase reversal. This device uses a proprietary, periodic autocalibration technique to provide low input offset voltage and very low input offset voltage drift over temp and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by making sure they are equal on both input pins. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines in order to reduce the likelihood of junctions being at different temperatures, which may cause thermoelectric voltages of 0.1 µV/°C or higher, depending on the materials used.

8.3.1 Operating Characteristics

The OPA188 is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics section.

8.3.2 Phase-Reversal Protection

The OPA188 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 图 39.

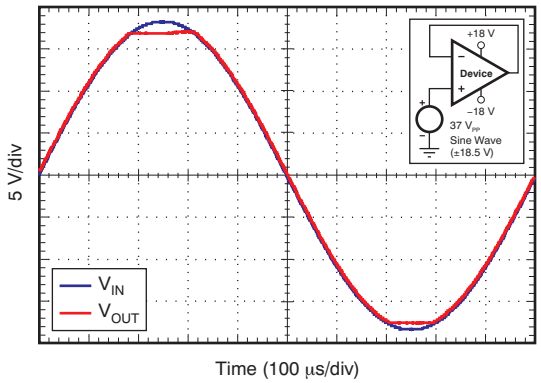


图 39. No Phase Reversal

8.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers, such as the OPA188, use switching on their inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents them from being amplified, however they may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.4 Internal Offset Correction

The OPA188 op amp uses an auto-calibration technique with a time-continuous 750-kHz op amp in the signal path. This amplifier is zero-corrected every 3 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

Feature Description (接下页)

8.3.5 EMI Rejection

The OPA188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 40 shows the results of this testing on the OPA188. 表 3 shows the EMIRR IN+ values for the OPA188 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 3 may be centered on or operated near the particular frequency shown. Detailed information can also be found in *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

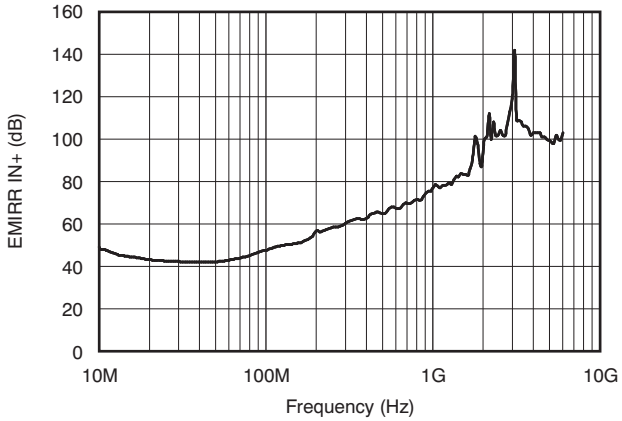


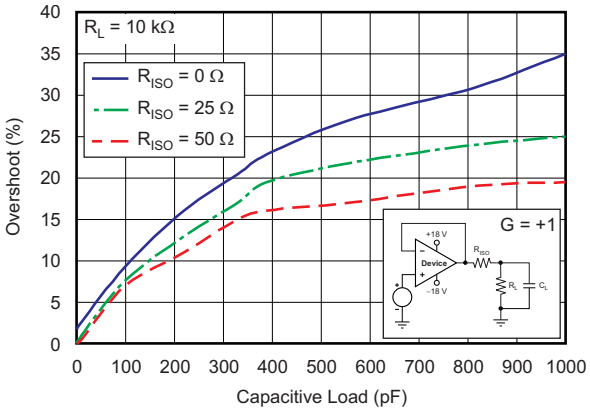
图 40. EMIRR Testing

表 3. OPA188 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	62.2 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	74.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	100.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	102.4 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	104.8 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100.3 dB

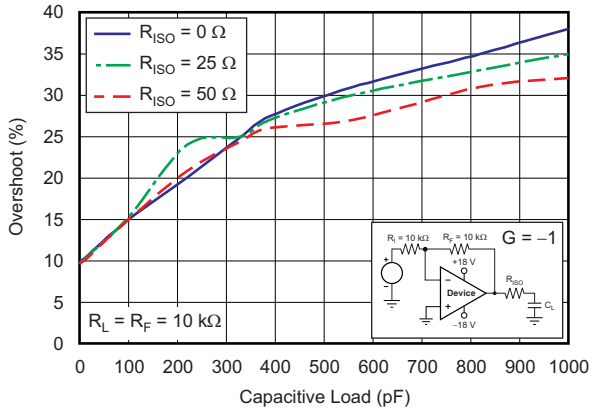
8.3.6 Capacitive Load and Stability

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 图 41 and 图 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, for details of analysis techniques and application circuits, refer to *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from www.ti.com,



G = 1, R_L = 10 kΩ, , 100-mV Output Step

图 41. Small-Signal Overshoot Versus Capacitive Load



G = –1, R_L = R_F = 10 kΩ, 100-mV Output Step

图 42. Small-Signal Overshoot Versus Capacitive Load

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See 图 43 for an illustration of the ESD circuits contained in the OPA188 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA188 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

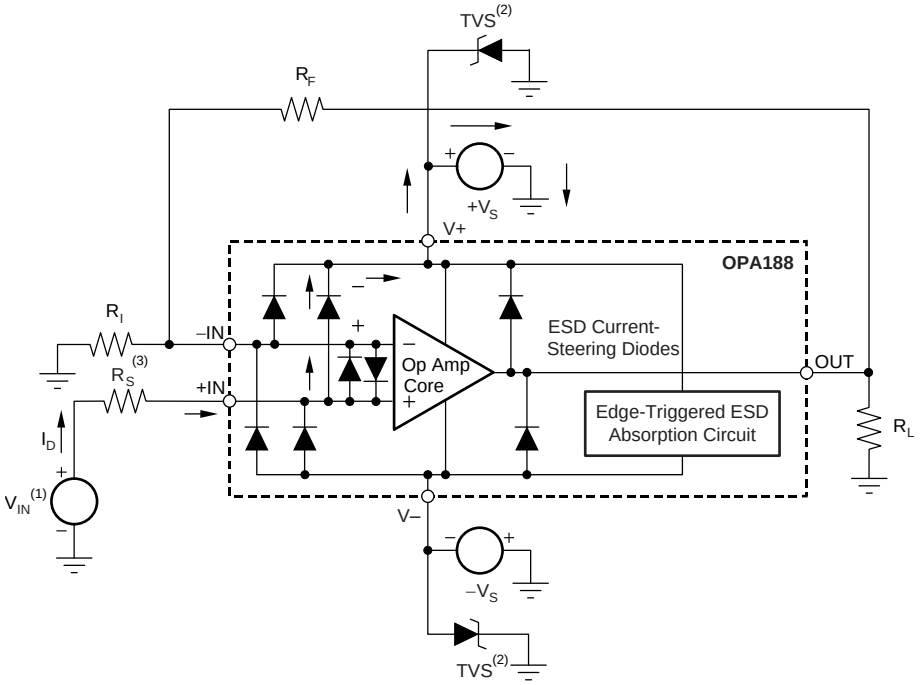
When the operational amplifier connects into a circuit (such as the one 图 43 depicts), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 43 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current-steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins, as shown in 图 43. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500$ mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (min)} > +V_S$.

(3) Suggested value is approximately 1 kΩ.

图 43. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

The OPA188 input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in 图 43. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA188. 图 43 shows an example configuration that implements a current-limiting feedback resistor.

8.4 Device Functional Modes

The OPA188 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPA188 is 36 V (±18 V).

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA188 operational amplifier combines precision offset and drift with excellent overall performance, making it ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPA188 can be used.

9.2 Typical Applications

9.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in 图 44 is a high-side voltage-to-current (V-I) converter. The converter translates an input voltage of 0 V to 2 V into an output current of 0 mA to 100 mA. 图 45 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2188 facilitate excellent dc accuracy for the circuit.

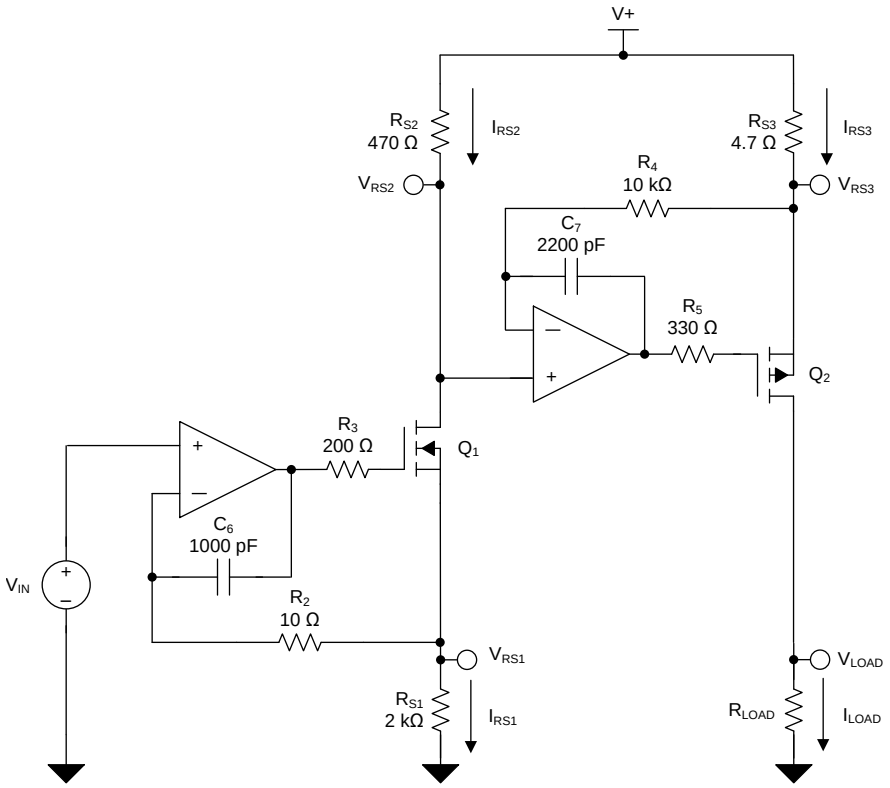


图 44. High-Side Voltage-to-Current (V-I) Converter

9.2.1.1 Design Requirements

The design requirements are:

Typical Applications (接下页)

- Supply voltage: 5 V dc
- Input: 0 V to 2 V dc
- Output: 0 mA to 100 mA dc

9.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA188 CMOS operational amplifier is a high-precision, ultralow offset, ultralow drift amplifier, optimized for low-voltage, single-supply operation, with an output swing to within 15 mV of the positive rail. The OPA188 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making this device appropriate for precise dc control. The rail-to-rail output stage of the OPA188 makes sure that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in reference design TIPD102, a step-by-step process to design a *High-Side Voltage-to-Current (V-I) Converter*.

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD102, *High-Side Voltage-to-Current (V-I) Converter* (SLAU502).

9.2.1.3 Application Curves

图 45 shows the measured transfer function for the high-side voltage-to-current converter shown in 图 44 .

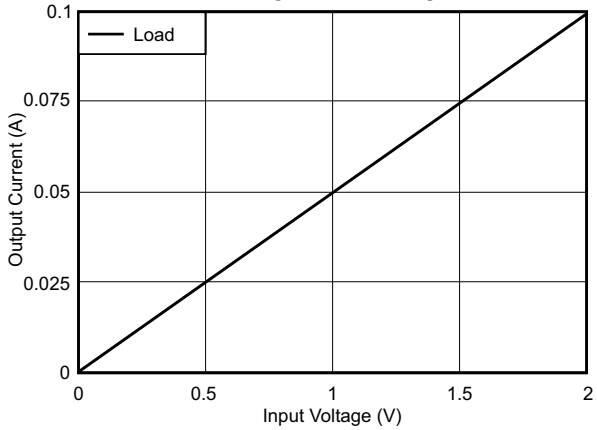


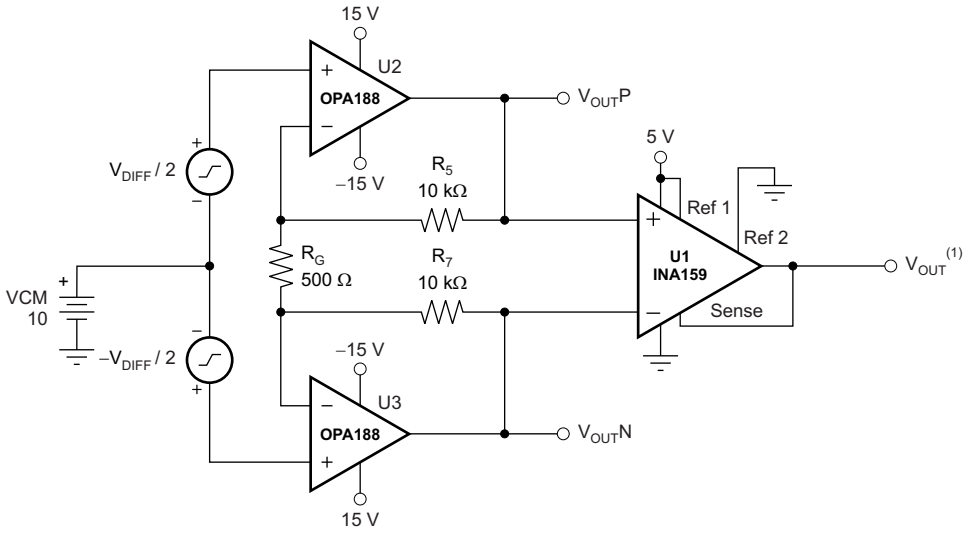
图 45. Measured Transfer Function for High-Side V-I Converter

9.2.2 Discrete INA + Attenuation for ADC With 3.3-V Supply

注

The TINA-TI files shown in the following sections require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

图 46 shows an example of how the OPA188 is used as a high-voltage, high-impedance front-end for a precision, discreet instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link download the TINA-TI file: Discrete INA.



(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref 1) / 2$.

图 46. Discrete INA + Attenuation for ADC With 3.3-V Supply

9.2.3 Bridge Amplifier

图 47 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: Bridge Amplifier Circuit.

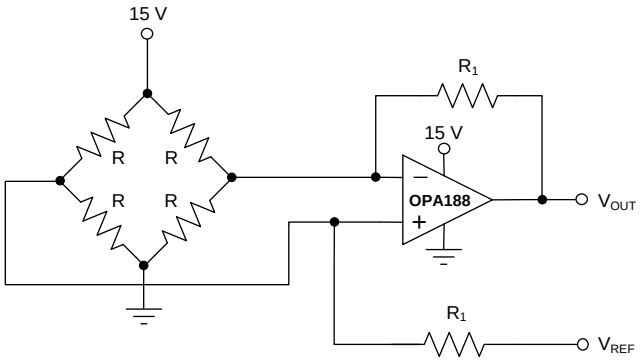


图 47. Bridge Amplifier

9.2.4 Low-Side Current Monitor

图 48 shows the OPA188 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPA188, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: Current-Sensing Circuit.

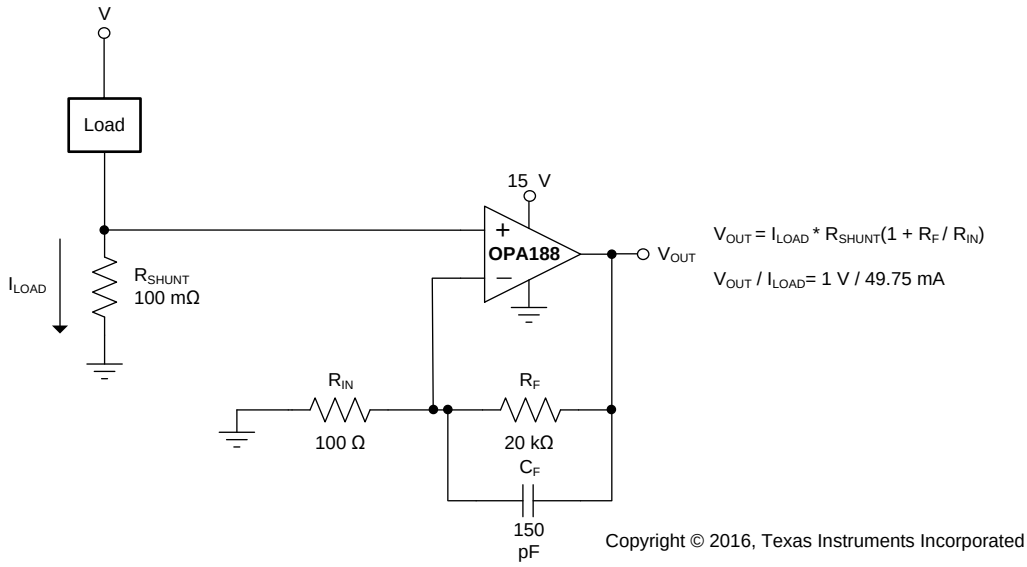


图 48. Low-Side Current Monitor

9.2.5 Programmable Power Supply

图 49 shows the OPA188 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five, and handles a large variety of capacitive and current loads. The OPA188 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: Programmable Power-Supply Circuit.

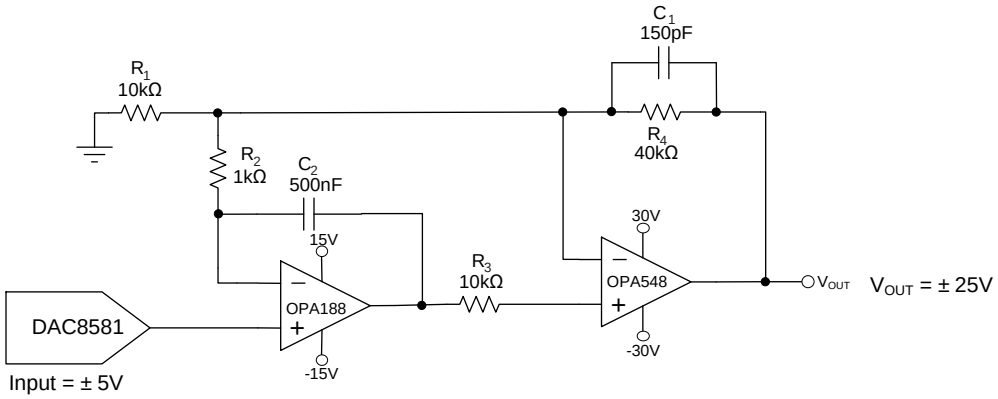
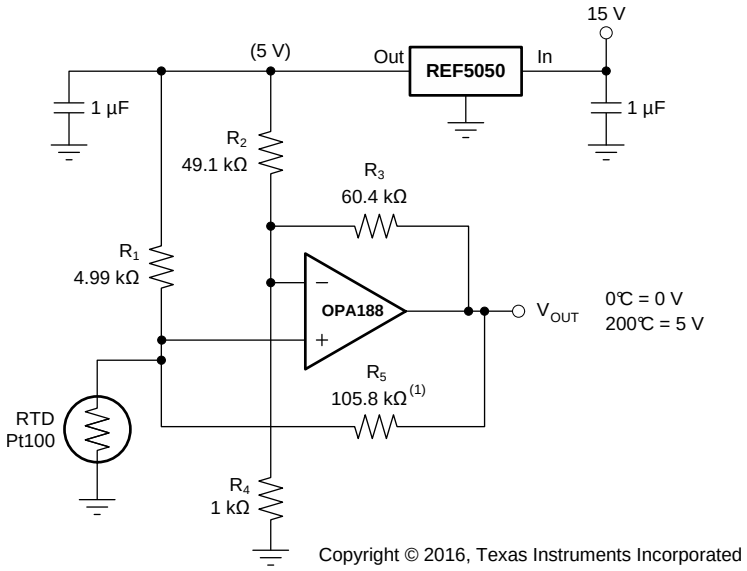


图 49. Programmable Power Supply

9.2.6 RTD Amplifier With Linearization

See *Analog Linearization Of Resistance Temperature Detectors* (SLYT442), for an in-depth analysis of 图 50. Click the following link to download the TINA-TI file: RTD Amplifier with Linearization.



(1) R_5 provides positive-varying excitation to linearize output.

图 50. RTD Amplifier With Linearization

10 Power Supply Recommendations

The OPA188 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

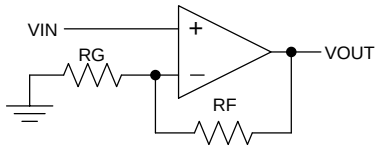
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Low-ESR, 0.1-µF ceramic bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- In order to reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



(Schematic Representation)

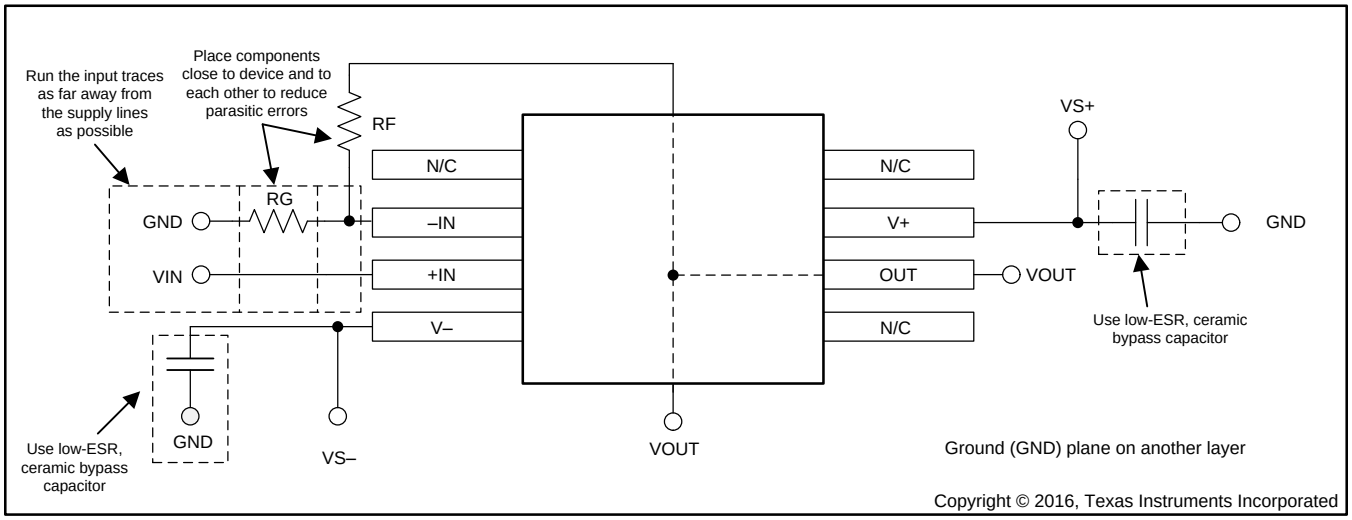


图 51. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™（免费下载软件）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器为用户提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *《运算放大器的 EMI 抑制比》*（文献编号：SBOA128）
- *《反馈曲线图定义运算放大器交流性能》*（文献编号：SBOA015）
- *《电阻式温度检测器的模拟线性化》*（文献编号：SLYT442），
- *《高侧电压电流 (V-I) 转换器》*（文献编号：SLAU502）

12.3 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA188AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA188	Samples
OPA188AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXZ	Samples
OPA188AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXZ	Samples
OPA188AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXX	Samples
OPA188AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXX	Samples
OPA188AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

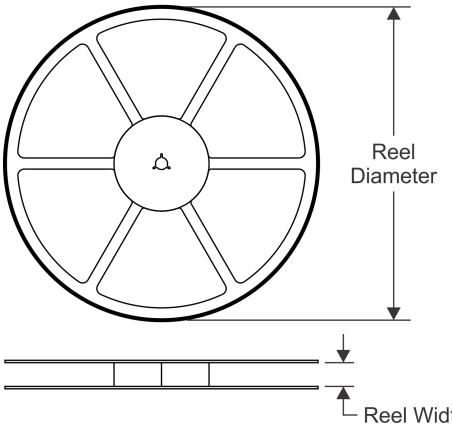
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

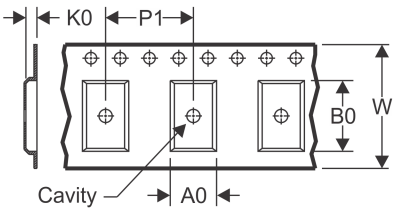
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

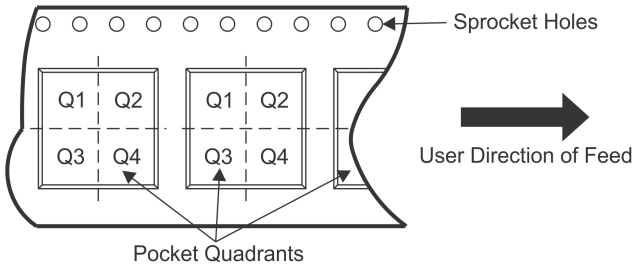


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

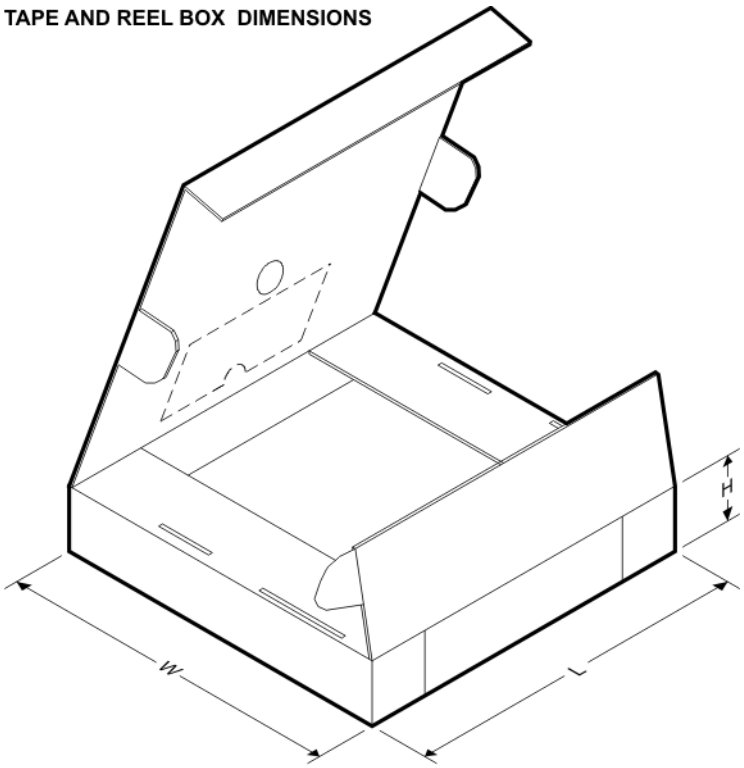
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA188AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA188AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA188AIDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA188AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

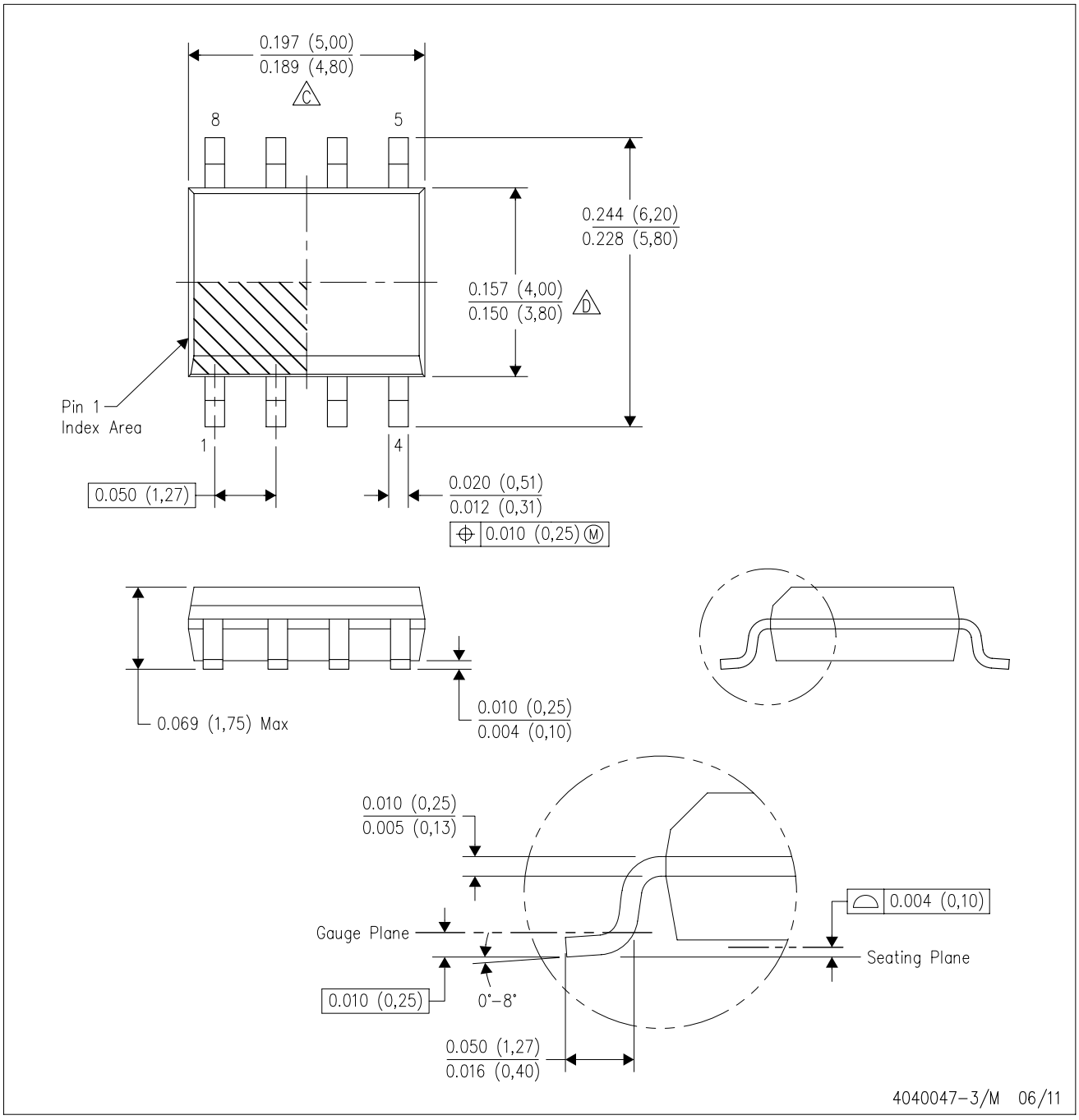
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

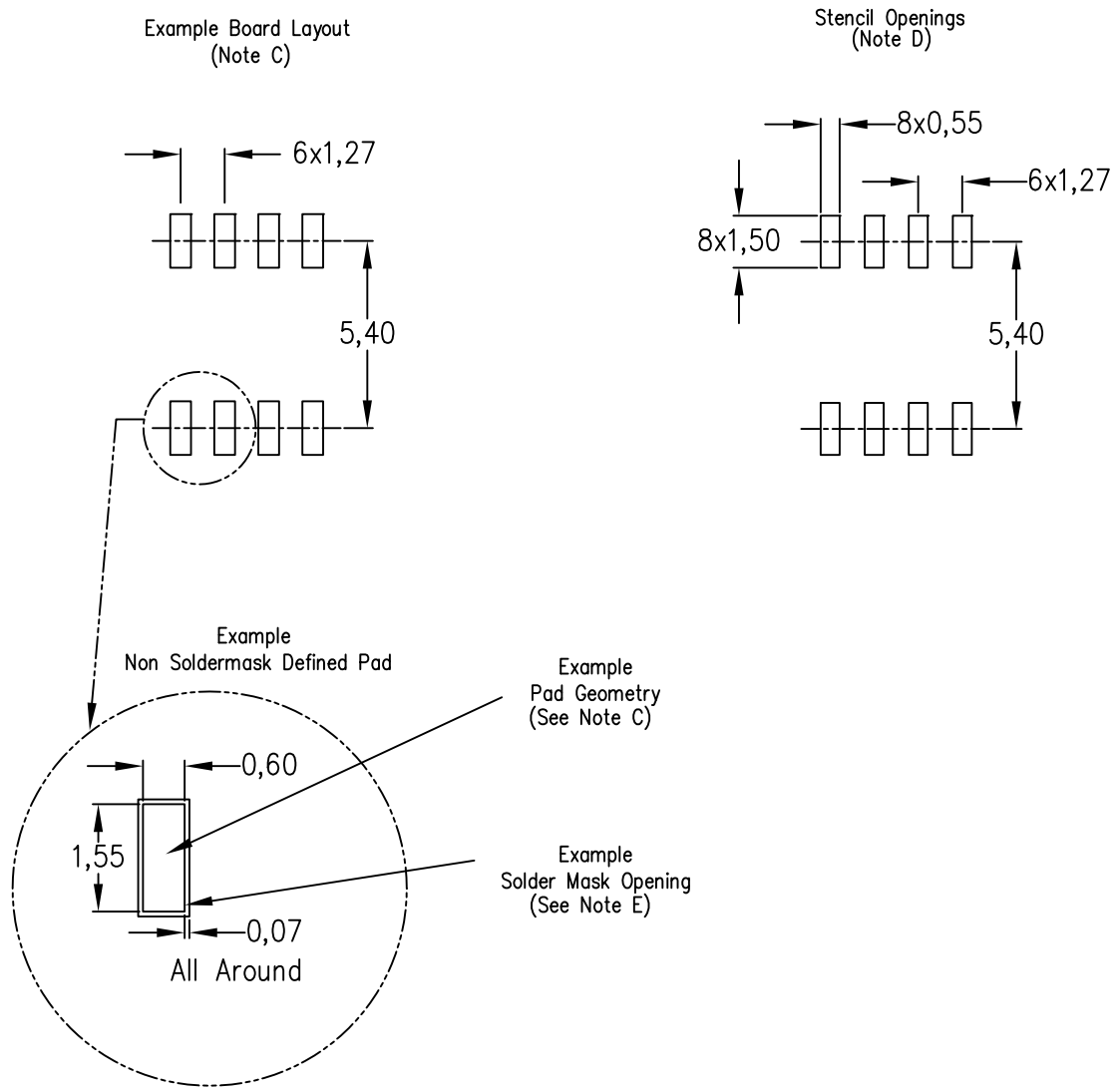
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA188AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA188AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA188AIDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
OPA188AIDGKT	VSSOP	DGK	8	250	202.0	201.0	28.0
OPA188AIDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



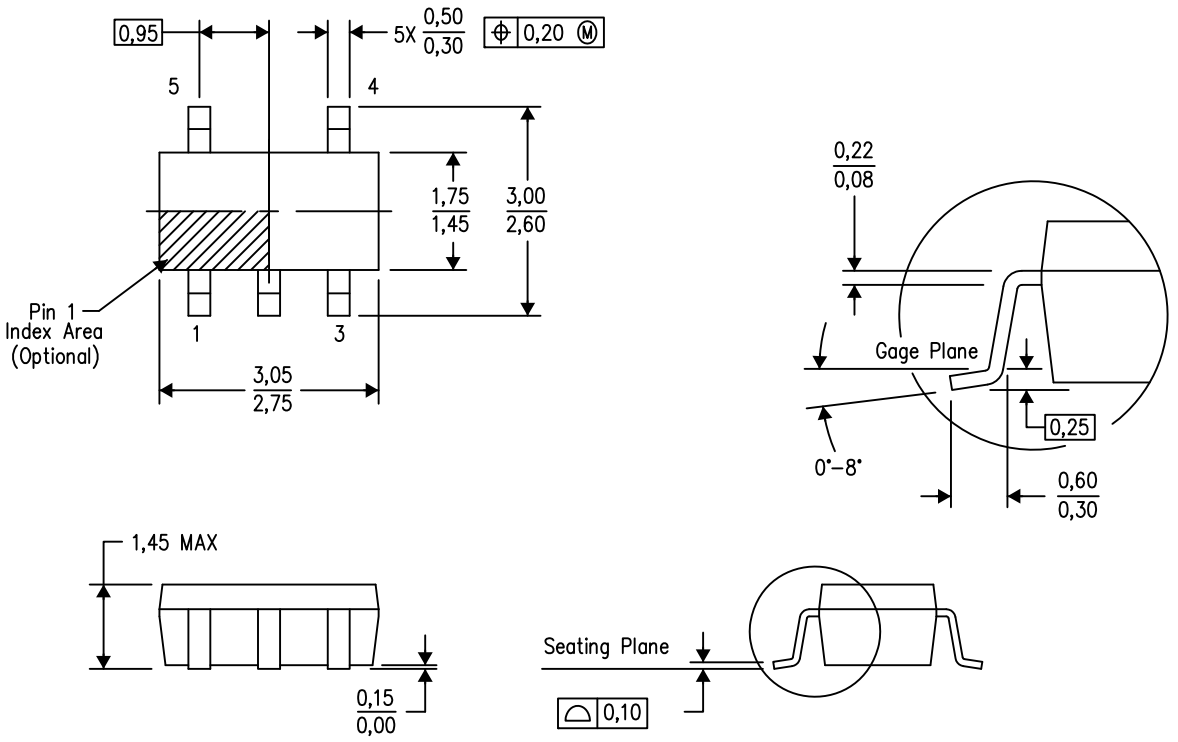
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

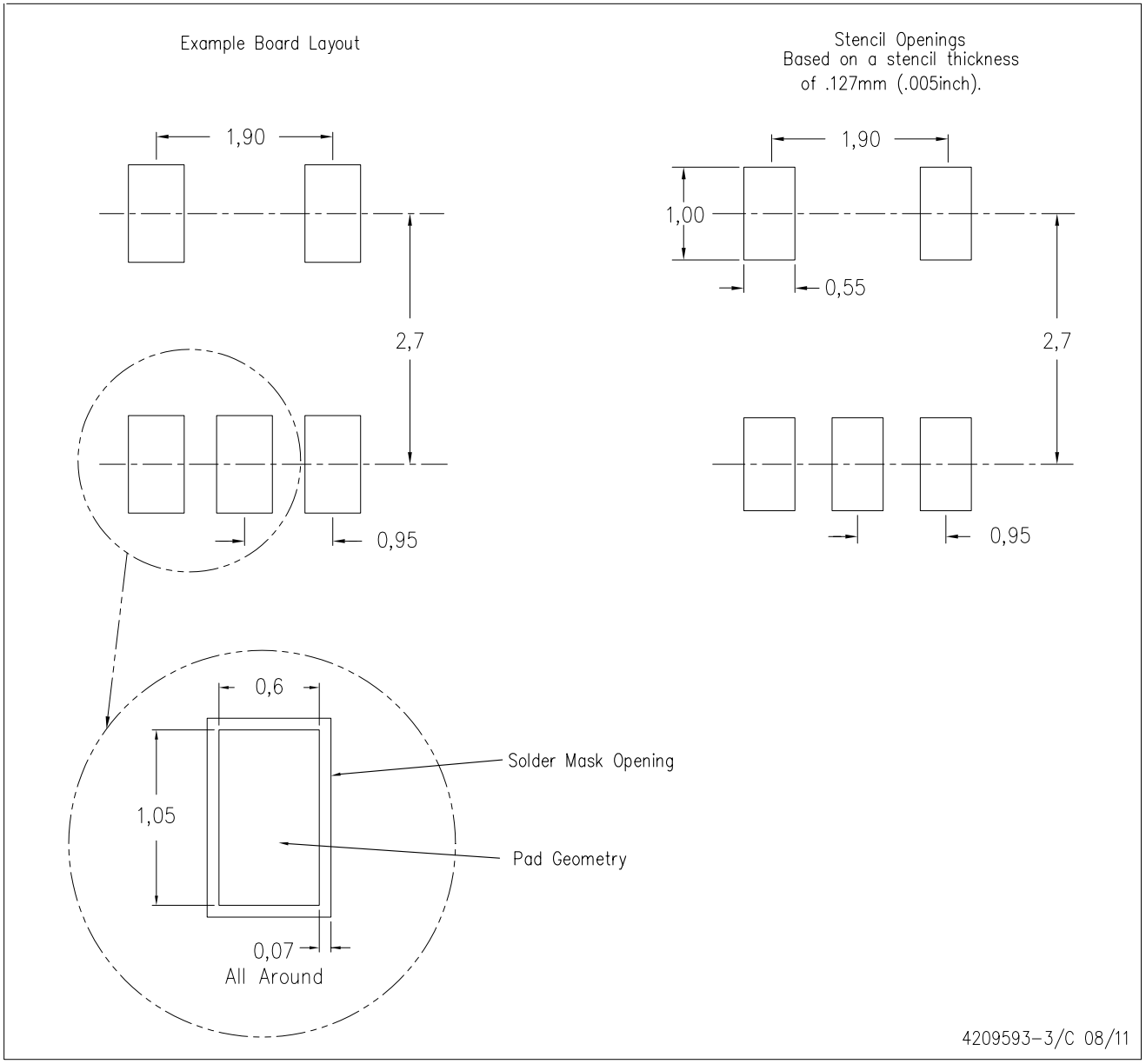
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

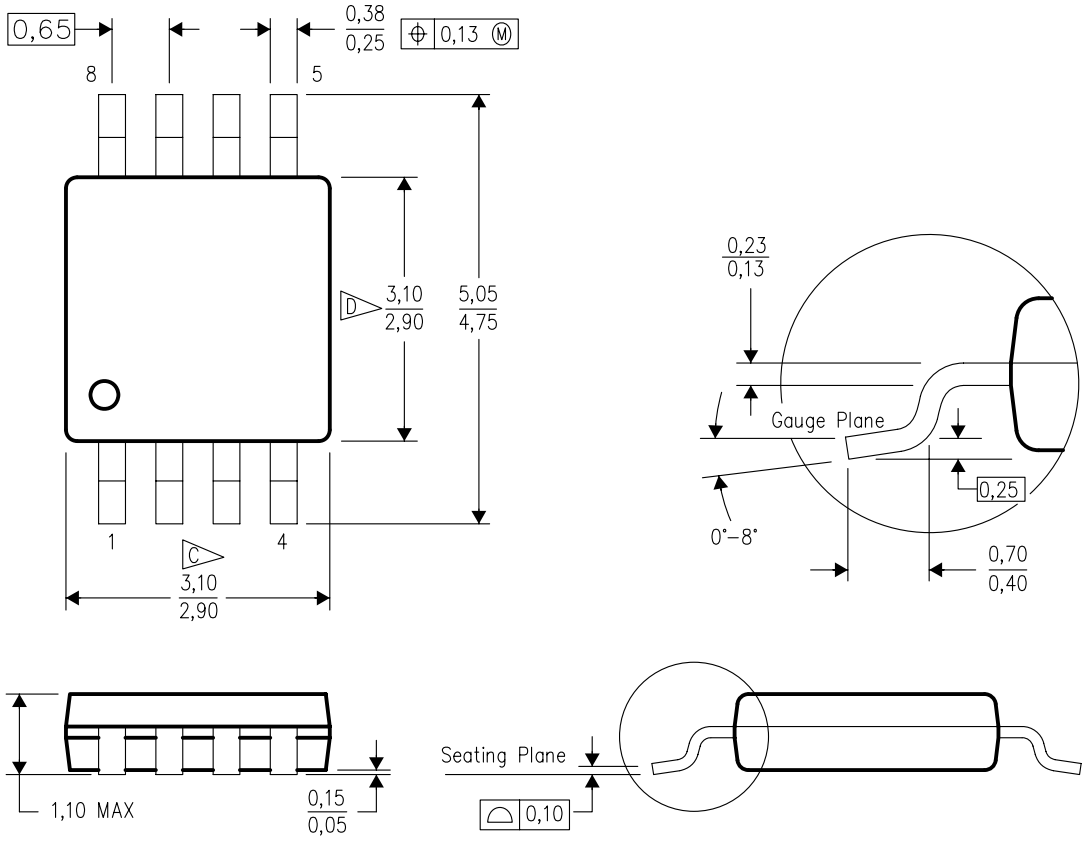
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

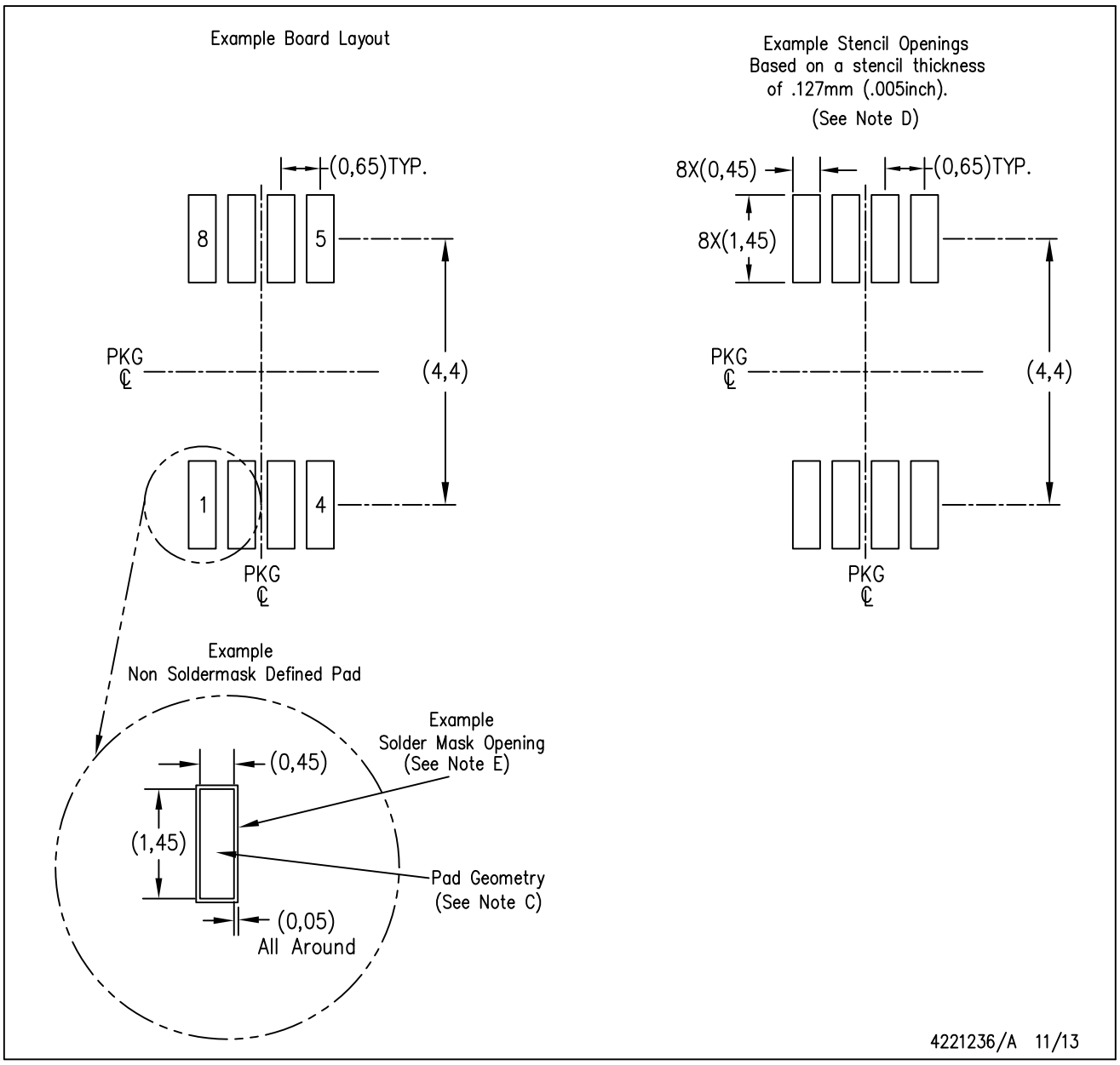
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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