# OPAx171 36-V, Single-Supply, SOT553, General-Purpose Operational Amplifiers

## 1 Features

- Supply Range: 2.7 to 36 V, ±1.35 V to ±18 V
- Low Noise: 14 nV/√Hz
- Low Offset Drift: ±0.3 µV/°C (Typical)
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 3 MHz
- Low Quiescent Current: 475 µA per Amplifier
- High Common-Mode Rejection: 120 dB (Typical)
- Low-Input Bias Current: 8 pA
- Industry-Standard Packages:
  - 8-Pin SOIC
  - 8-Pin MSOP
  - 14-Pin TSSOP
- *micro*Packages:
  - Single in SOT553
  - Dual in VSSOP-8

## 2 Applications

- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

## 3 Description

The OPA171, OPA2171, and OPA4171 (OPAx171) are a family of 36-V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most operational amplifiers, which are specified at only one supply voltage, the OPAx171 family is specified from 2.7 to 36 V. Input signals beyond the supply rails do not cause phase reversal. The OPAx171 family is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. These devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

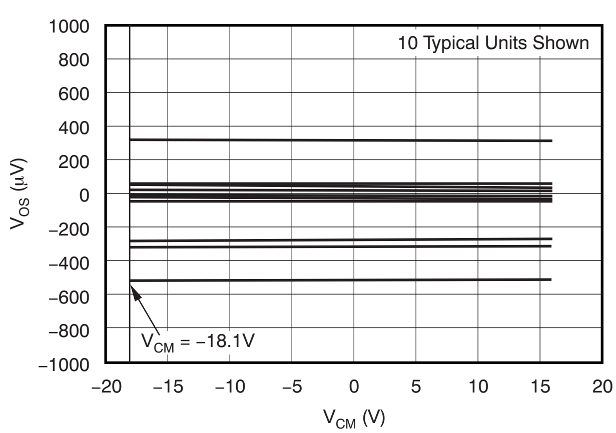
The OPAx171 series of operational amplifiers are specified from –40°C to 125°C.

**Device Information(1)**

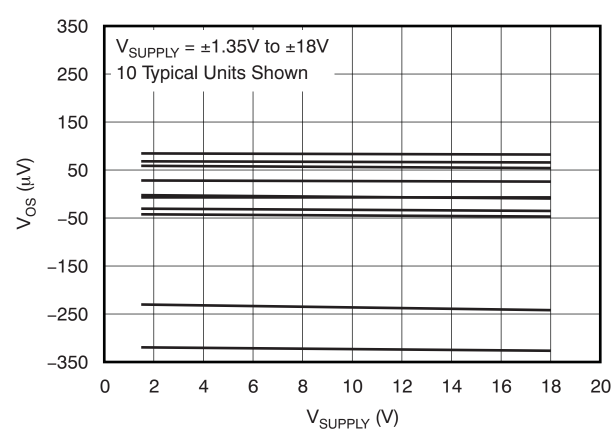
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA171 | SOT23 (5) | 1.60 mm × 2.90 mm |
| OPA2171 | SOIC (8) | 3.90 mm × 4.90 mm |
| OPA4171 | TSSOP (14) | 4.40 mm × 5.00 mm |
| | SOIC (14) | 3.90 mm × 8.65 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Offset Voltage vs Common-Mode Voltage**




**Offset Voltage vs Power Supply**



# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision D (September 2012) to Revision E** — **Page**

- Changed device title (removed "Value Line Series") ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision C (June 2011) to Revision D** — **Page**

- Added "Value Line Series" to title ... 1

**Changes from Revision B (November 2010) to Revision C** — **Page**

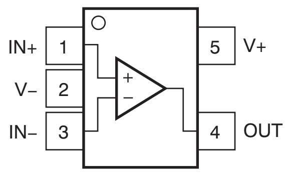
- Added MSOP-8 package to device graphic ... 1
- Added MSOP-8 package to Features bullets ... 1
- Added MSOP-8 package to Product Family table ... 1
- Updated pinout configurations for OPA2171 and OPA4171 ... 3
- Updated format of thermal information tables ... 6
- Added MSOP-8 package to OPA2171 Thermal Information table ... 6
- Added new row for Voltage Output Swing from Rail parameter to *Output* subsection of *Electrical Characteristics* ... 7
- Changed Voltage Output Swing from Rail parameter to over temperature in *Output* subsection of *Electrical Characteristics* ... 7
- Changed Figure 9 ... 10

**Changes from Revision A (November, 2010) to Revision B** — **Page**

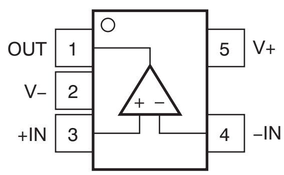
- Changed input offset voltage specification ... 7
- Changed input offset voltage, over temperature specification ... 7
- Changed quiescent current per amplifier, over temperature specification ... 8

## 5 Pin Configuration and Functions

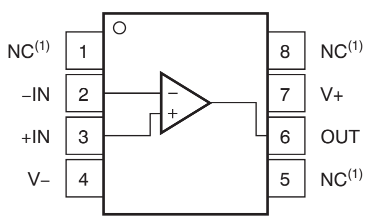
**DRL Package: OPA171**
**SOT-553**
**Top View**




**DBV Package: OPA171**
**SOT23-5**
**Top View**

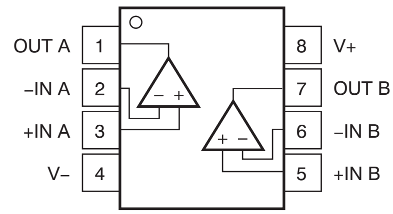



**D PACKAGE: OPA171**
**SO-8**
**Top View**

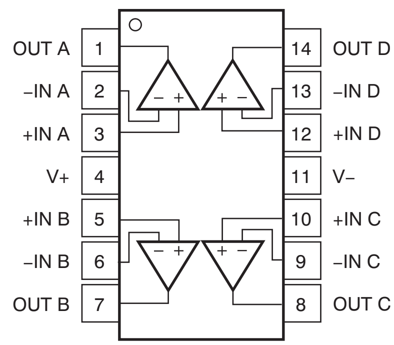



(1) No internal connection.

**D, DCU, and DGK Packages: OPA2171**
**SO-8, VSSOP-8, and MSOP-8**
**Top View**




**D and PW Packages: OPA4171**
**SO-14 and TSSOP-14**
**Top View**




### Pin Functions: OPA171

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DRL | DBV | D | | |
| +IN | 1 | 3 | 3 | I | Noninverting input |
| –IN | 3 | 4 | 2 | I | Inverting input |
| OUT | 4 | 1 | 6 | O | Output |
| V+ | 5 | 5 | 7 | — | Positive (highest) supply |
| V– | 2 | 2 | 4 | — | Negative (lowest) supply |
| NC | — | — | 1, 5, 8 | — | No internal connection (can be left floating) |

### Pin Functions: OPA2171

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DCU | DGK | D | | |
| +IN A | 3 | 3 | 3 | I | Noninverting input |
| +IN B | 5 | 5 | 5 | I | Noinverting input |
| –IN A | 2 | 2 | 2 | I | Inverting input |
| –IN B | 6 | 6 | 6 | O | Inverting input |
| OUT A | 1 | 1 | 1 | O | Output |
| OUT B | 7 | 7 | 7 | — | Output |

### Pin Functions: OPA2171 (continued)

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DCU | DGK | D | | |
| V+ | 8 | 8 | 8 | — | Positive (highest) supply |
| V– | 4 | 4 | 4 | — | Negative (lowest) supply |

### Pin Functions: OPA4171

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DCU | DGK | | |
| +IN A | 3 | 3 | I | Noninverting input |
| +IN B | 5 | 5 | I | Noninverting input |
| +IN C | 10 | 10 | I | Noninverting input |
| +IN D | 12 | 12 | I | Noninverting input |
| –IN A | 2 | 2 | I | Inverting input |
| –IN B | 6 | 6 | I | Inverting input |
| –IN C | 9 | 9 | I | Inverting input |
| –IN D | 13 | 13 | I | Inverting input |
| OUT A | 1 | 1 | O | Output |
| OUT B | 7 | 7 | O | Output |
| OUT C | 8 | 8 | O | Output |
| OUT D | 14 | 14 | O | Output |
| V+ | 4 | 4 | — | Positive (highest) supply |
| V– | 11 | 11 | — | Negative (lowest) supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | | ±20 | | V |
| Signal input terminals | Voltage | (V–) – 0.5 | (V+) + 0.5 | V |
| | Current | –10 | 10 | mA |
| Output short circuit[2] | | Continuous | | |
| Operating temperature | | –55 | 150 | °C |
| Junction temperature | | | 150 | °C |
| Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage (V+ – V–) | 4.5 (±2.25) | | 36 (±18) | V |
| Specified temperature | –40 | | 125 | °C |

## 6.4 Thermal Information: OPA171

| THERMAL METRIC(1) | | OPA171 D (SO) 8 PINS | OPA171 DBV (SOT23) 5 PINS | OPA171 DRL (SOT553) 5 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 149.5 | 245.8 | 208.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 97.9 | 133.9 | 0.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 87.7 | 83.6 | 42.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 35.5 | 18.2 | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 89.5 | 83.1 | 42.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Thermal Information: OPA2171

| THERMAL METRIC(1) | | OPA2171 D (SO) 8 PINS | OPA2171 DGK (MSOP) 8 PINS | OPA2171 DCU (VSSOP) 8 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 134.3 | 175.2 | 195.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 72.1 | 74.9 | 59.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 60.6 | 22.2 | 115.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.2 | 1.6 | 4.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 53.8 | 22.8 | 114.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.6 Thermal Information: OPA4171

| THERMAL METRIC(1) | | OPA4171 D (SOIC) 14 PINS | OPA4171 PW (TSSOP) 14 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 93.2 | 106.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 51.8 | 24.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.4 | 59.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 13.5 | 0.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 42.2 | 54.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.7 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = 2.7 to 36 V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| Input offset voltage | $V_{OS}$ | | | 0.25 | ±1.8 | mV |
| Over temperature | | $T_A$ = –40°C to 125°C | | 0.3 | ±2 | mV |
| Drift | $dV_{OS}/dT$ | $T_A$ = –40°C to 125°C | | 0.3 | ±2 | µV/°C |
| vs power supply | PSRR | $V_S$ = 4 to 36 V, $T_A$ = –40°C to 125°C | | 1 | ±3 | µV/V |
| Channel separation, dc | | DC | | 5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input bias current | $I_B$ | | | ±8 | ±15 | pA |
| Over temperature | | $T_A$ = –40°C to 125°C | | | ±3.5 | nA |
| Input offset current | $I_{OS}$ | | | ±4 | | pA |
| Over temperature | | $T_A$ = –40°C to 125°C | | | ±3.5 | nA |
| **NOISE** | | | | | | |
| Input voltage noise | | f = 0.1 Hz to 10 Hz | | 3 | | $\mu V_{PP}$ |
| Input voltage noise density | $e_n$ | f = 100 Hz | | 25 | | $nV/\sqrt{Hz}$ |
| | | f = 1 kHz | | 14 | | $nV/\sqrt{Hz}$ |
| **INPUT VOLTAGE** | | | | | | |
| Common-mode voltage range(1) | $V_{CM}$ | | (V–) – 0.1 V | | (V+) – 2 V | V |
| Common-mode rejection ratio | CMRR | $V_S$ = ±2 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V, $T_A$ = –40°C to 125°C | 90 | 104 | | dB |
| | | $V_S$ = ±18V, (V–) – 0.1V < $V_{CM}$ < (V+) – 2 V, $T_A$ = –40°C to 125°C | 104 | 120 | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | 100 \|\| 3 | | MΩ \|\| pF |
| Common-mode | | | | 6 \|\| 3 | | $10^{12}$Ω \|\| pF |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-loop voltage gain | $A_{OL}$ | $V_S$ = 4 V to 36 V, (V–) + 0.35 V < $V_O$ < (V+) – 0.35 V, $T_A$ = –40°C to 125°C | 110 | 130 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain bandwidth product | GBP | | | 3.0 | | MHz |
| Slew rate | SR | G = +1 | | 1.5 | | V/µs |
| Settling time | $t_S$ | To 0.1%, $V_S$ = ±18 V, G = +1, 10-V step | | 6 | | µs |
| | | To 0.01% (12 bit), $V_S$ = ±18V, G = +1, 10V step | | 10 | | µs |
| Overload recovery time | | $V_{IN}$ × Gain > $V_S$ | | 2 | | µs |
| Total harmonic distortion + noise | THD+N | G = +1, f = 1kHz, $V_O$ = $3V_{RMS}$ | | 0.0002% | | |
| **OUTPUT** | | | | | | |
| Voltage output swing from rail | $V_O$ | $V_S$ = 5V, $R_L$ = 10kΩ | | 30 | | mV |
| Over temperature | | $R_L$ = 10 kΩ, $A_{OL}$ ≥ 110 dB, $T_A$ = –40°C to 125°C | (V–) + 0.35 | | (V+) – 0.35 | V |
| Short-circuit current | $I_{SC}$ | | | +25/–35 | | mA |
| Capacitive load drive | $C_{LOAD}$ | | | See *Typical Characteristics* | | pF |
| Open-loop output resistance | $R_O$ | f = 1MHz, $I_O$ = 0A | | 150 | | Ω |

(1) The input range can be extended beyond (V+) – 2V up to V+. See *Typical Characteristics* and *Application and Implementation* for additional information.

## Electrical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 2.7 to 36 V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Specified voltage range | $V_S$ | | 2.7 | | 36 | V |
| Quiescent current per amplifier | $I_Q$ | $I_O$ = 0A | | 475 | 595 | µA |
| Over temperature | | $I_O$ = 0 A, $T_A$ = –40°C to 125°C | | | 650 | µA |
| **TEMPERATURE** | | | | | | |
| Specified range | | | –40 | | 125 | °C |
| Operating range | | | –55 | | 150 | °C |

## 6.8 Typical Characteristics

### Table 1. Characteristic Performance Measurements

| DESCRIPTION | FIGURE |
|---|---|
| Offset Voltage Production Distribution | Figure 1 |
| Offset Voltage Drift Distribution | Figure 2 |
| Offset Voltage vs Temperature | Figure 3 |
| Offset Voltage vs Common-Mode Voltage | Figure 4 |
| Offset Voltage vs Common-Mode Voltage (Upper Stage) | Figure 5 |
| Offset Voltage vs Power Supply | Figure 6 |
| $I_B$ and $I_{OS}$ vs Common-Mode Voltage | Figure 7 |
| Input Bias Current vs Temperature | Figure 8 |
| Output Voltage Swing vs Output Current (Maximum Supply) | Figure 9 |
| CMRR and PSRR vs Frequency (Referred-to Input) | Figure 10 |
| CMRR vs Temperature | Figure 11 |
| PSRR vs Temperature | Figure 12 |
| 0.1-Hz to 10-Hz Noise | Figure 13 |
| Input Voltage Noise Spectral Density vs Frequency | Figure 14 |
| THD+N Ratio vs Frequency | Figure 15 |
| THD+N vs Output Amplitude | Figure 16 |
| Quiescent Current vs Temperature | Figure 17 |
| Quiescent Current vs Supply Voltage | Figure 18 |
| Open-Loop Gain and Phase vs Frequency | Figure 19 |
| Closed-Loop Gain vs Frequency | Figure 20 |
| Open-Loop Gain vs Temperature | Figure 21 |
| Open-Loop Output Impedance vs Frequency | Figure 22 |
| Small-Signal Overshoot vs Capacitive Load (100-mV Output Step) | Figure 23, Figure 24 |
| No Phase Reversal | Figure 25 |
| Positive Overload Recovery | Figure 26 |
| Negative Overload Recovery | Figure 27 |
| Small-Signal Step Response (100 mV) | Figure 28, Figure 29 |
| Large-Signal Step Response | Figure 30, Figure 31 |
| Large-Signal Settling Time (10-V Positive Step) | Figure 32 |
| Large-Signal Settling Time (10-V Negative Step) | Figure 33 |
| Short-Circuit Current vs Temperature | Figure 34 |
| Maximum Output Voltage vs Frequency | Figure 35 |
| Channel Separation vs Frequency | Figure 36 |

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

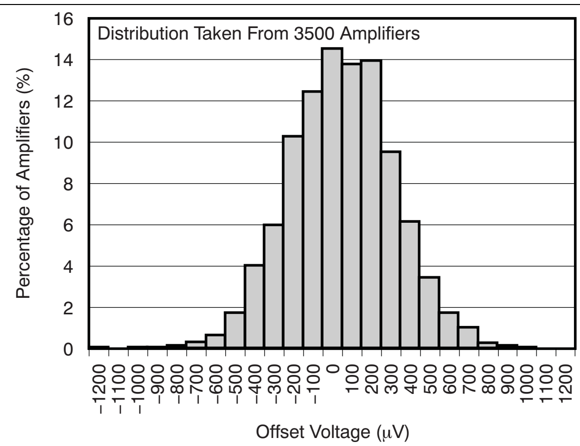



**Figure 1. Offset Voltage Production Distribution**

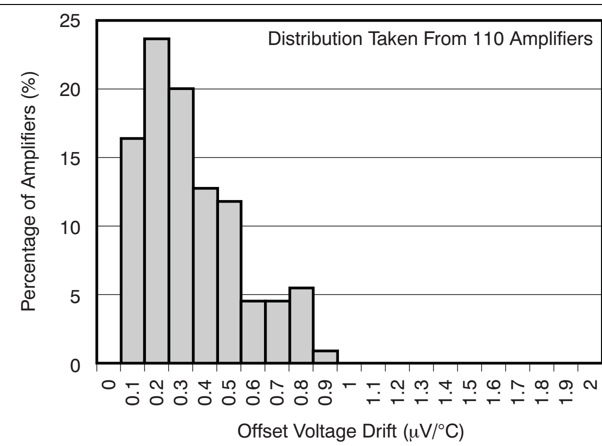



**Figure 2. Offset Voltage Drift Distribution**

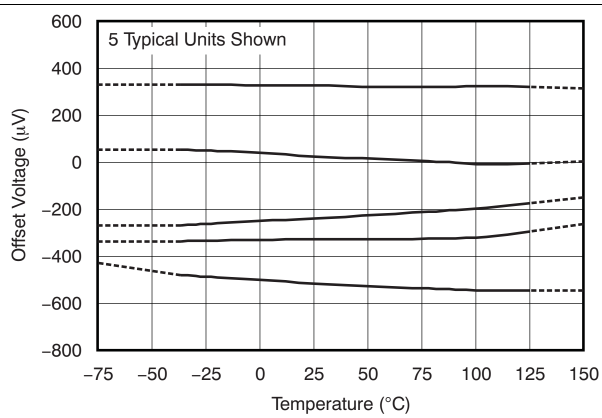



**Figure 3. Offset Voltage vs Temperature**

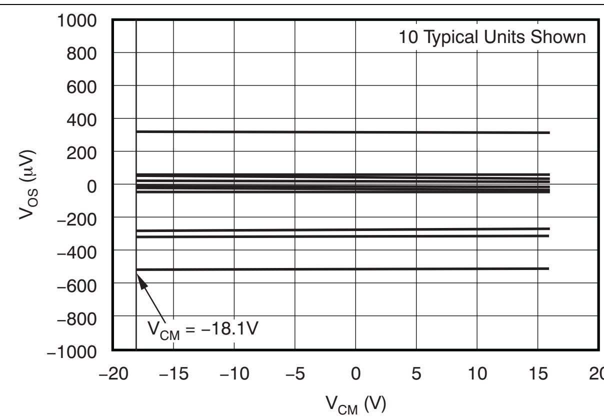



**Figure 4. Offset Voltage vs Common-Mode Voltage**

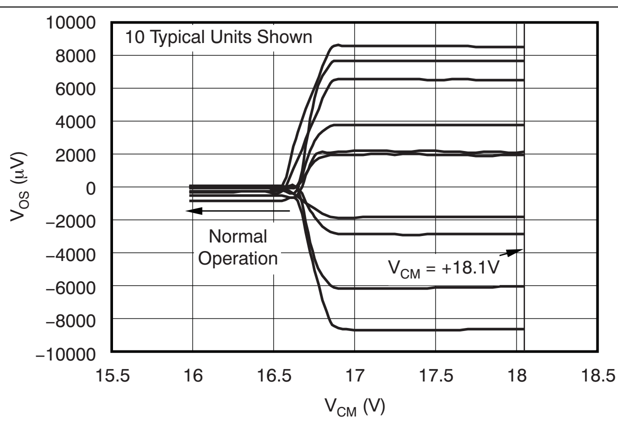



**Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)**

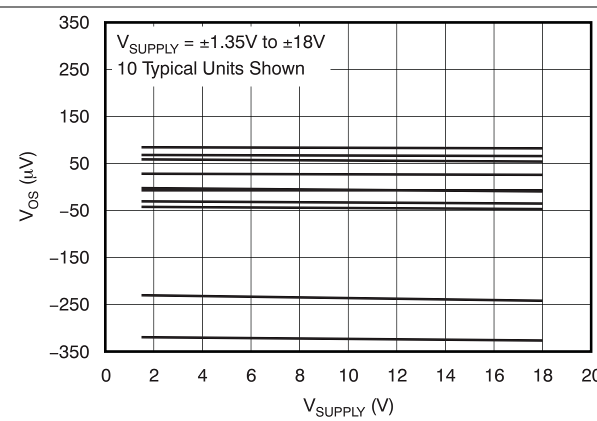



**Figure 6. Offset Voltage vs Power Supply**

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

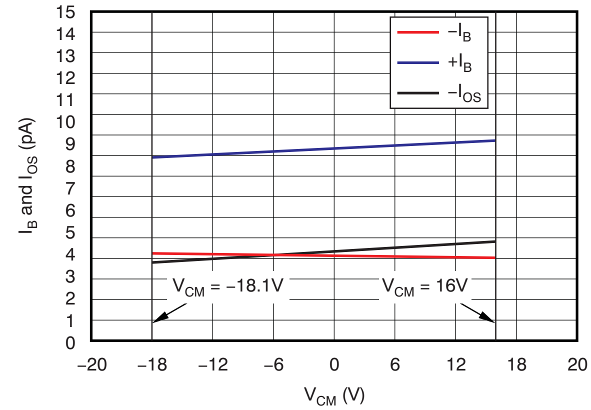



Figure 7. $I_B$ and $I_{OS}$ vs Common-Mode Voltage

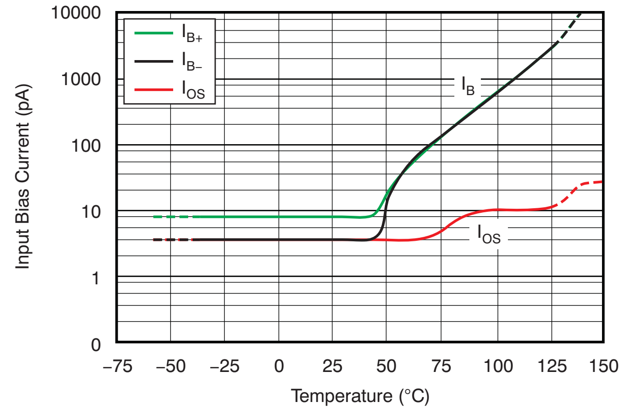



Figure 8. Input Bias Current vs Temperature

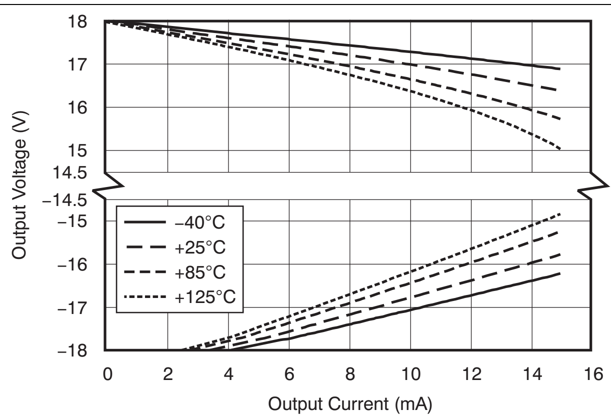



Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

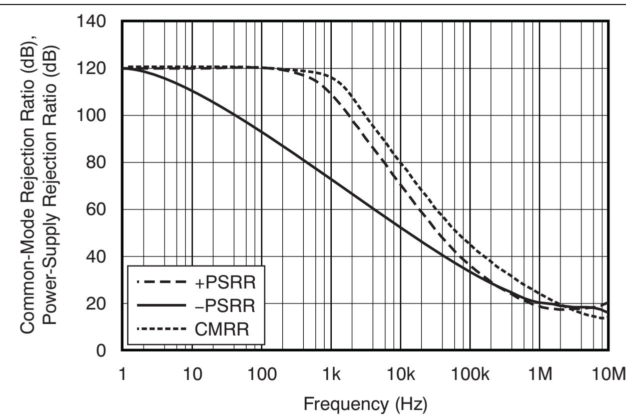



Figure 10. CMRR and PSRR vs Frequency (Referred-to Input)

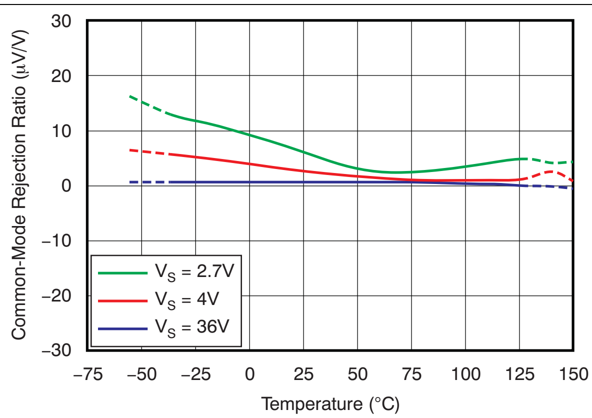



Figure 11. CMRR vs Temperature

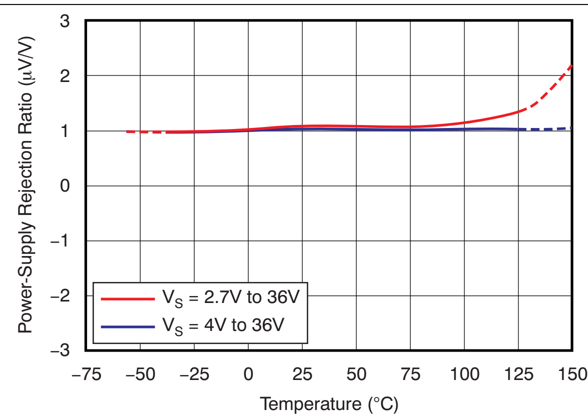



Figure 12. PSRR vs Temperature

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

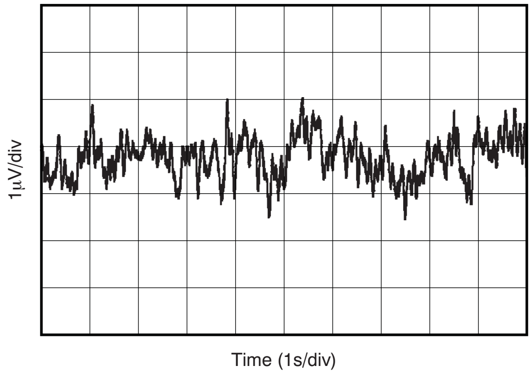



**Figure 13. 0.1-Hz to 10-Hz Noise**

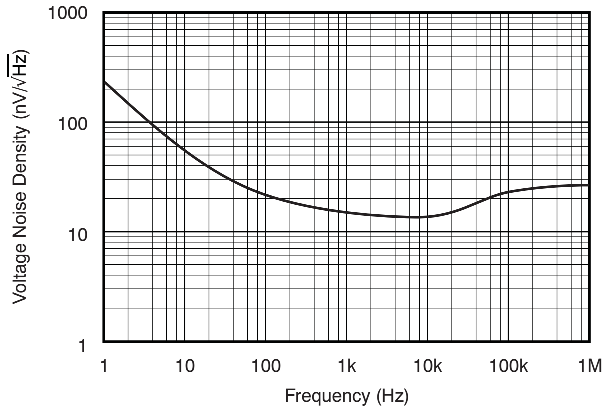



**Figure 14. Input Voltage Noise Spectral Density vs Frequency**

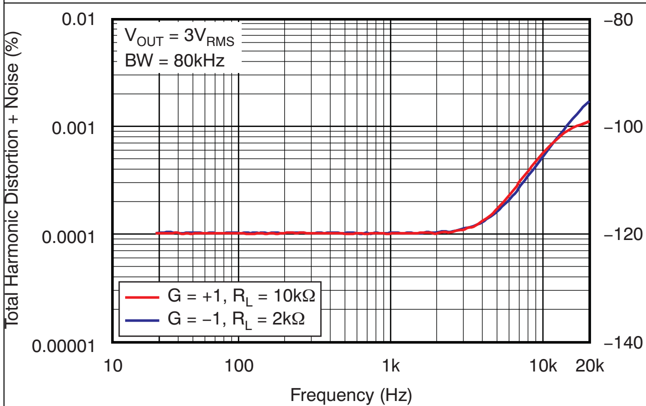



**Figure 15. THD+N Ratio vs Frequency**

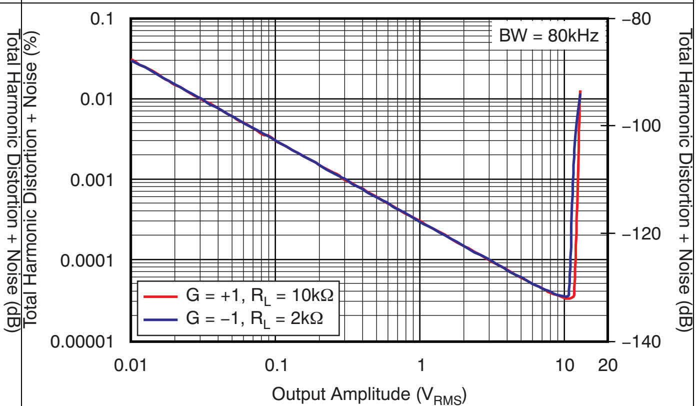



**Figure 16. THD+N vs Output Amplitude**

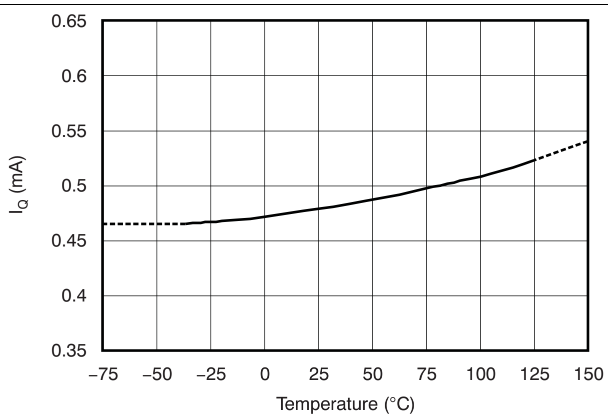



**Figure 17. Quiescent Current vs Temperature**

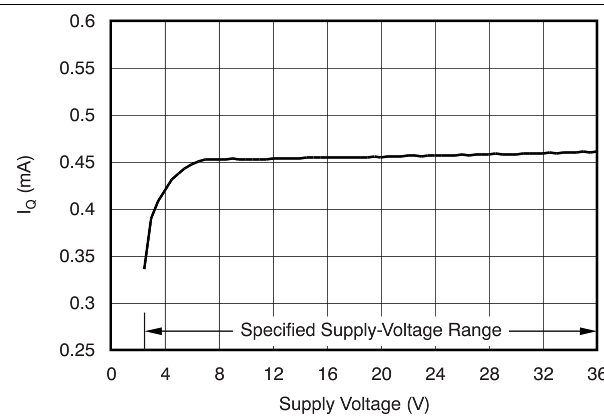



**Figure 18. Quiescent Current vs Supply Voltage**

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

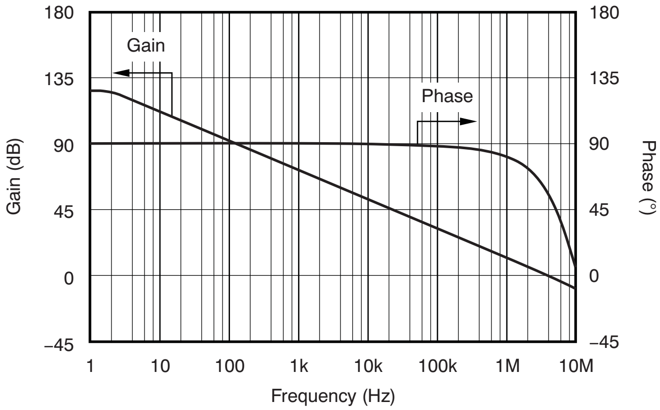



**Figure 19. Open-Loop Gain and Phase vs Frequency**

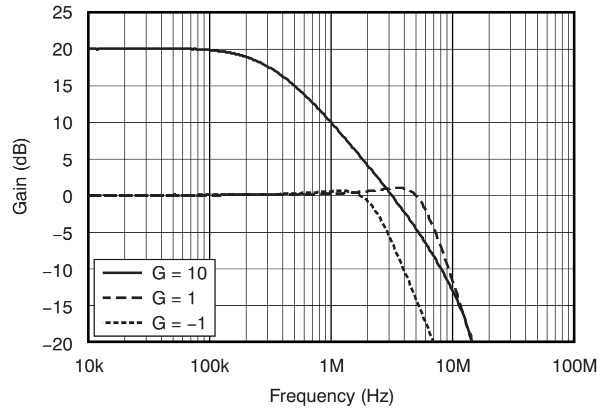



**Figure 20. Closed-Loop Gain vs Frequency**

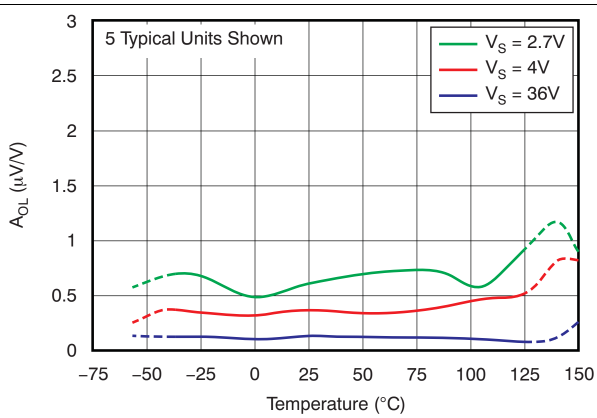



**Figure 21. Open-Loop Gain vs Temperature**

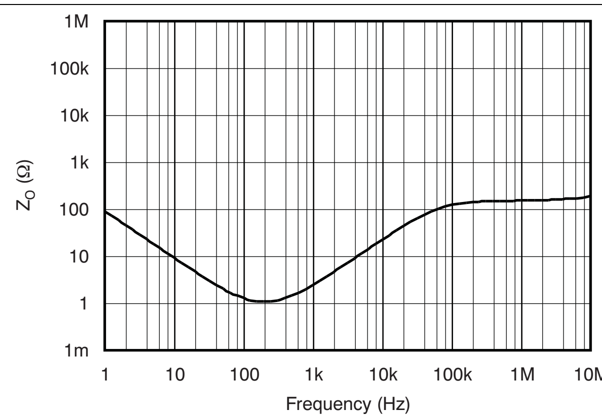



**Figure 22. Open-Loop Output Impedance vs Frequency**

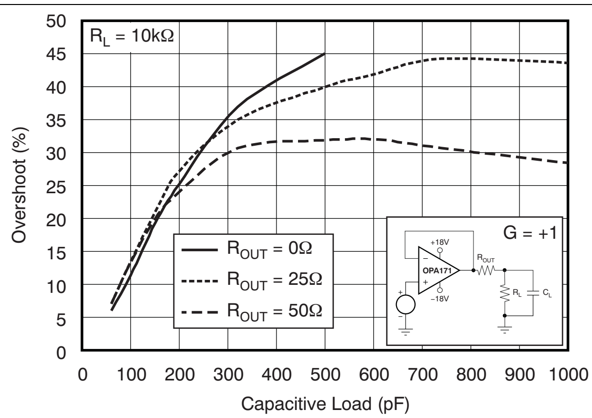



**Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

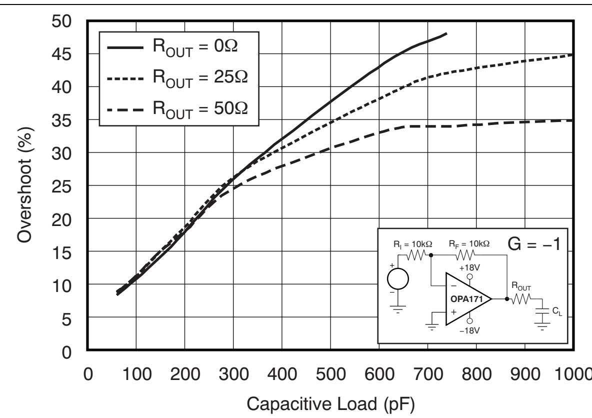



**Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

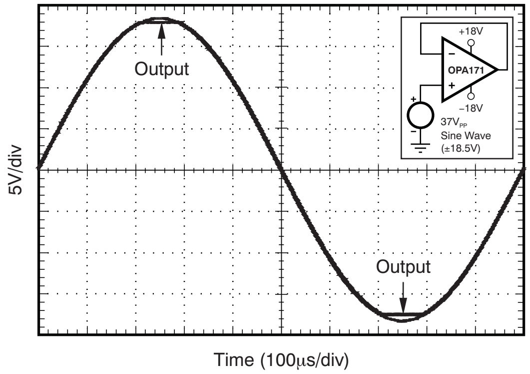



**Figure 25. No Phase Reversal**

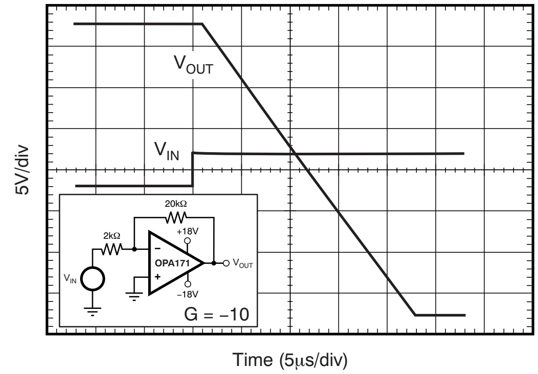



**Figure 26. Positive Overload Recovery**

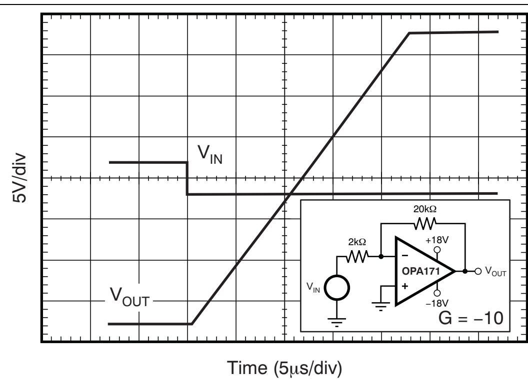



**Figure 27. Negative Overload Recovery**

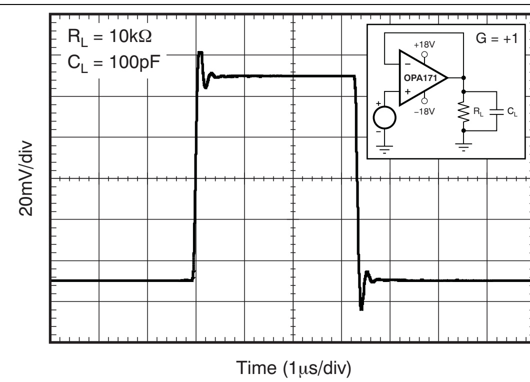



**Figure 28. Small-Signal Step Response (100 mV)**

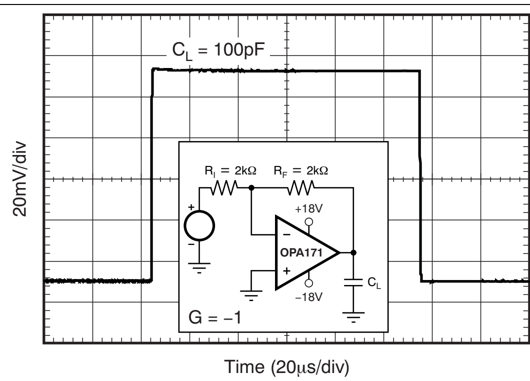



**Figure 29. Small-Signal Step Response (100 mV)**

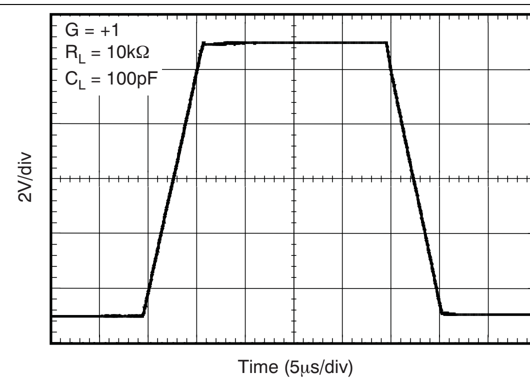



**Figure 30. Large-Signal Step Response**

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

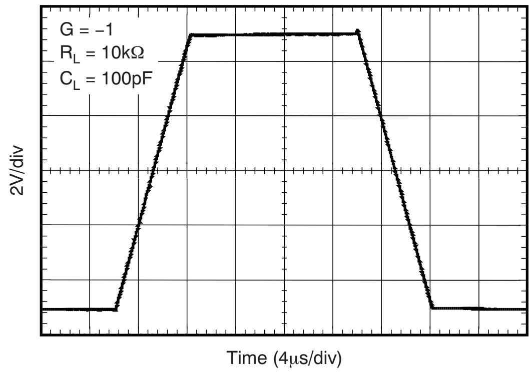



**Figure 31. Large-Signal Step Response**

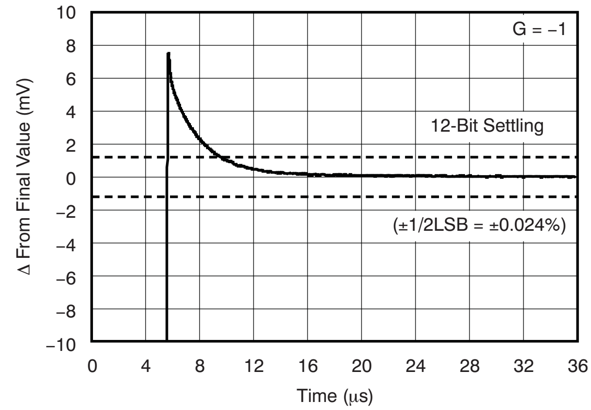



**Figure 32. Large-Signal Settling Time (10-V Positive Step)**

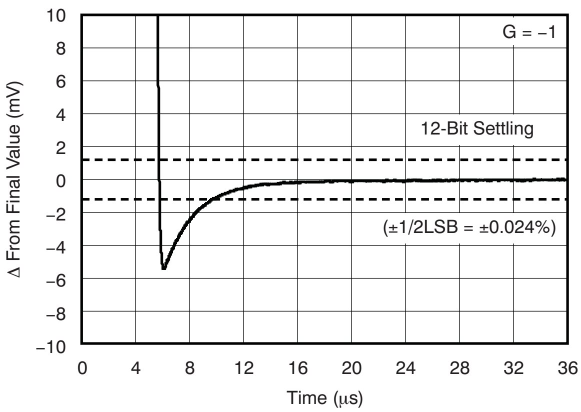



**Figure 33. Large-Signal Settling Time (10-V Negative Step)**

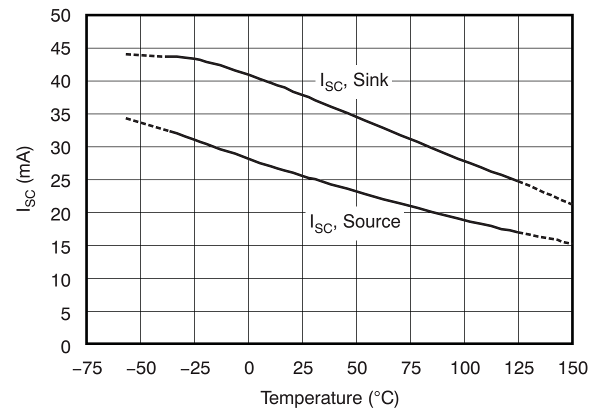



**Figure 34. Short-Circuit Current vs Temperature**

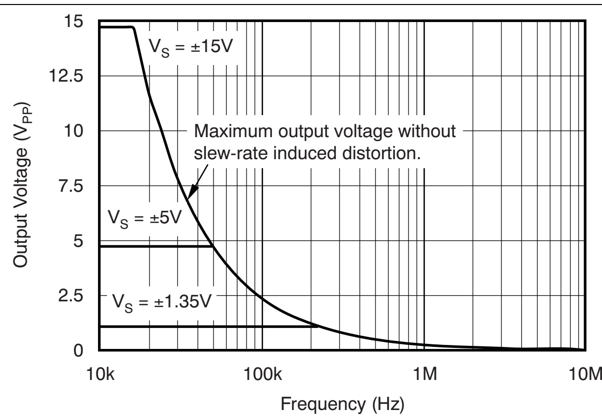



**Figure 35. Maximum Output Voltage vs Frequency**

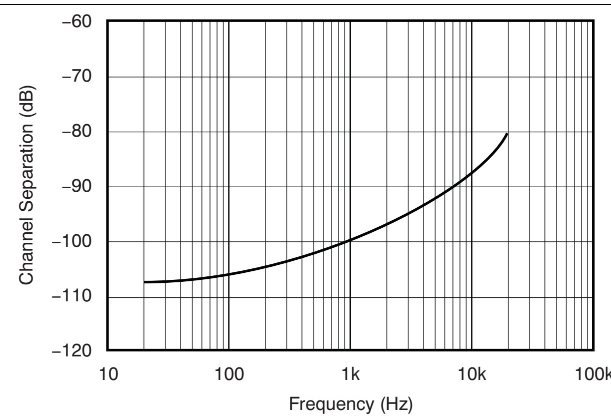


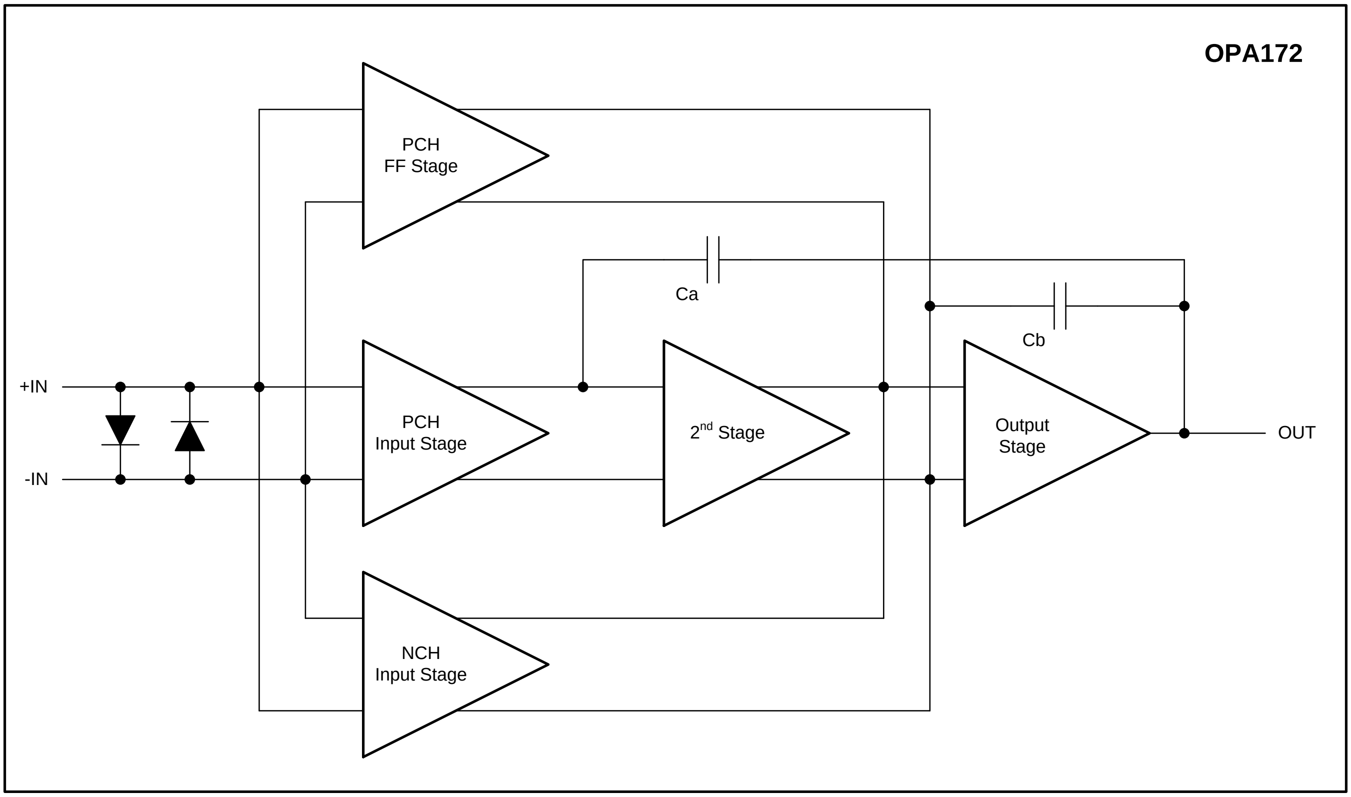

**Figure 36. Channel Separation vs Frequency**

# 7 Detailed Description

## 7.1 Overview

The OPAx171 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and $A_{OL}$. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Operating Characteristics

The OPAx171 family of amplifiers is specified for operation from 2.7 to 36 V (±1.35 to ±18 V). Many of the specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

### 7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 2.

## Feature Description (continued)

### 7.3.3 Phase-Reversal Protection

The OPAx171 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 37.

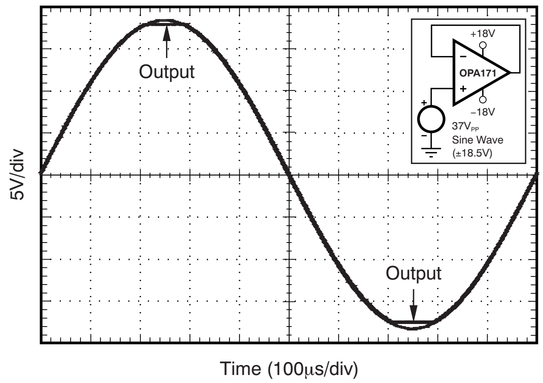



**Figure 37. No Phase Reversal**

**Table 2. Typical Performance Range**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| **Input Common-Mode Voltage** | **(V+) – 2** | | **(V+) + 0.1** | **V** |
| Offset voltage | | 7 | | mV |
| **vs Temperature** | | **12** | | **µV/°C** |
| Common-mode rejection | | 65 | | dB |
| Open-loop gain | | 60 | | dB |
| GBW | | 0.7 | | MHz |
| Slew rate | | 0.7 | | V/µs |
| Noise at f = 1kHz | | 30 | | nV/√Hz |

### 7.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx171-Q1 family of devices have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ equal to 50 Ω) in series with the output. Figure 38 and Figure 39 show small-signal overshoot versus capacitive load for several values of $R_{OUT}$. Also, for details of analysis techniques and application circuits, refer to the *Applications Bulletin AB-028* (SBOA015), available for download from TI.com.

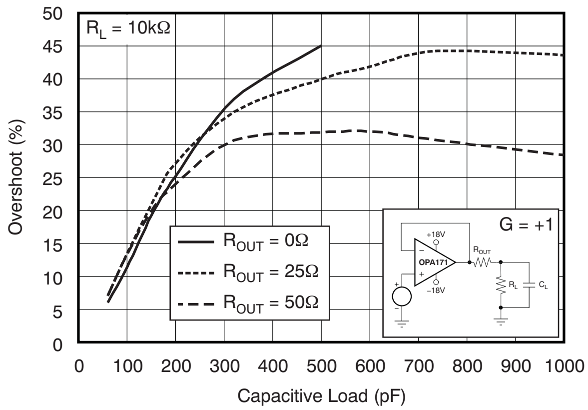



**Figure 38. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

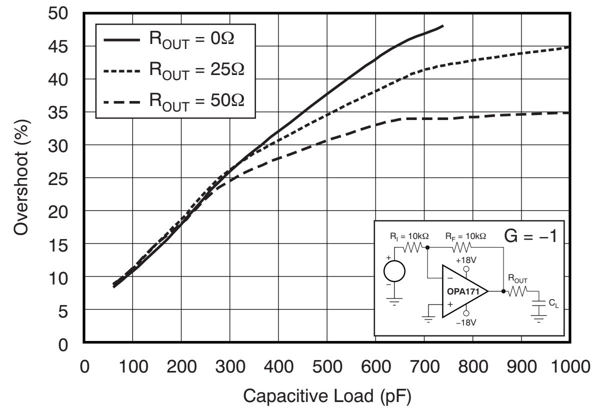



**Figure 39. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

## 7.4 Device Functional Modes

### 7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171 family of devices extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 2.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The OPAx171 operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very-good overall performance with high CMRR, PSRR, and $A_{OL}$. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

### 8.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins

or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the *Absolute Maximum Ratings*. Figure 40 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

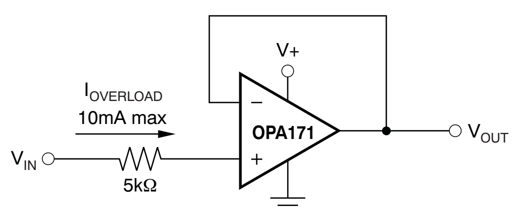



**Figure 40. Input Current Protection**

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The Zener voltage must be selected such that the diode does not turn on during normal operation.

However, its Zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

## 8.2 Typical Application

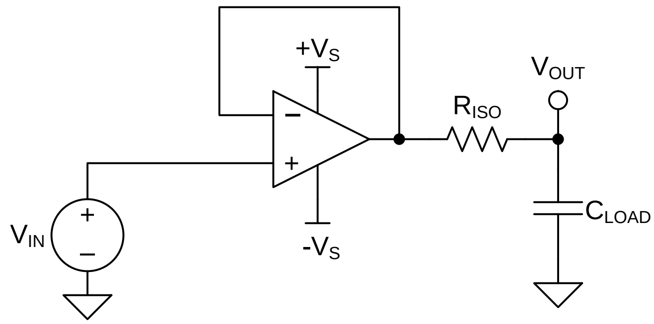



**Figure 41. Unity-Gain Buffer With $R_{ISO}$ Stability Compensation**

### 8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

### 8.2.2 Detailed Design Procedure

Figure 42 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 42. Not shown in Figure 42 is the open-loop output resistance of the operational amplifier, $R_o$.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole ($f_p$) is determined by ($R_o$ + $R_{ISO}$) and $C_{LOAD}$. Components $R_{ISO}$ and $C_{LOAD}$ determine the frequency of the zero ($f_z$). A stable system is obtained by selecting $R_{ISO}$ such that the rate of closure (ROC) between the open-loop gain ($A_{OL}$) and 1/β is 20 dB/decade. Figure 42 depicts the concept. The 1/β curve for a unity-gain buffer is 0 dB.

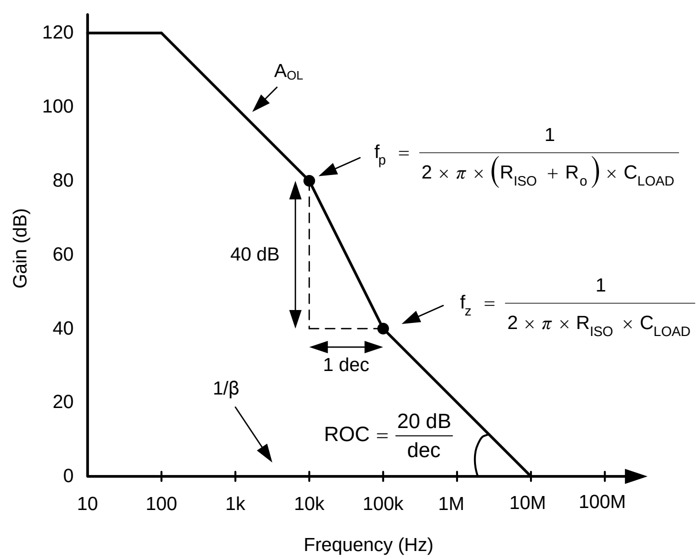



**Figure 42. Unity-Gain Amplifier With $R_{ISO}$ Compensation**

## Typical Application (continued)

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of $R_o$. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA171, refer to the Precision Design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

**Table 3. Phase Margin versus Overshoot and AC Gain Peaking**

| PHASE MARGIN | OVERSHOOT | AC GAIN PEAKING |
|---|---|---|
| 45° | 23.3% | 2.35 dB |
| 60° | 8.8% | 0.28 dB |

#### *8.2.2.1 Capacitive Load and Stability*

The dynamic characteristics of the OPAx171 have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ equal to 50 Ω) in series with the output. Figure 38 and Figure 39 illustrate graphs of small-signal overshoot versus capacitive load for several values of $R_{OUT}$. Also, refer to *Applications Bulletin AB-028* (SBOA015), available for download from the TI website for details of analysis techniques and application circuits.

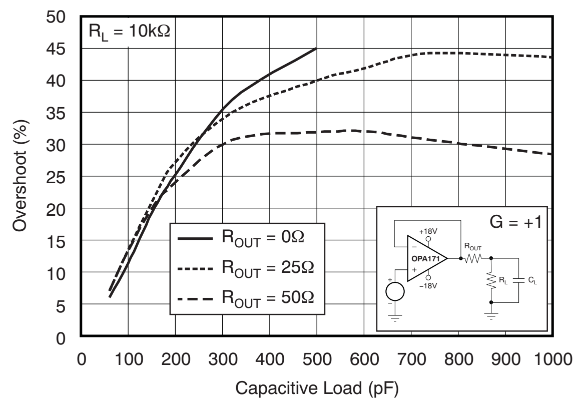



**Figure 43. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

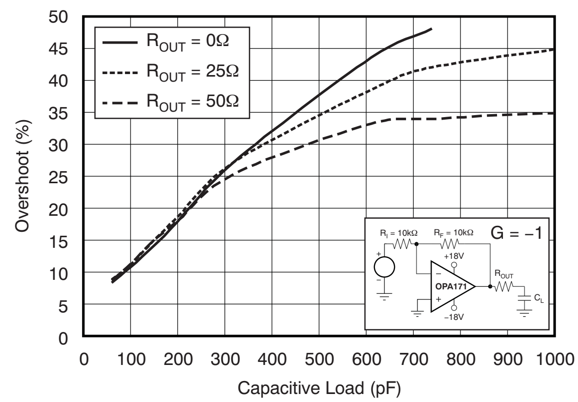



**Figure 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

### 8.2.3 Application Curve

The OPA171 meets the supply voltage requirements of 30 V. The OPA171 is tested for various capacitive loads and RISO is adjusted to get an overshoot corresponding to Table 3. The results of the these tests are summarized in Figure 45.

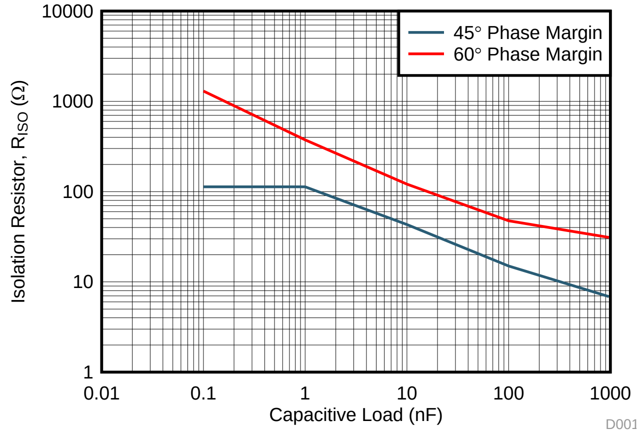



**Figure 45. $R_{ISO}$ vs $C_{LOAD}$**

# 9 Power Supply Recommendations

The OPAx171 family of devices is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Specifications* section.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, good printed--circuit board (PCB) layout practices are recommended. Low-loss, 0.1-µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

## 10.2 Layout Example

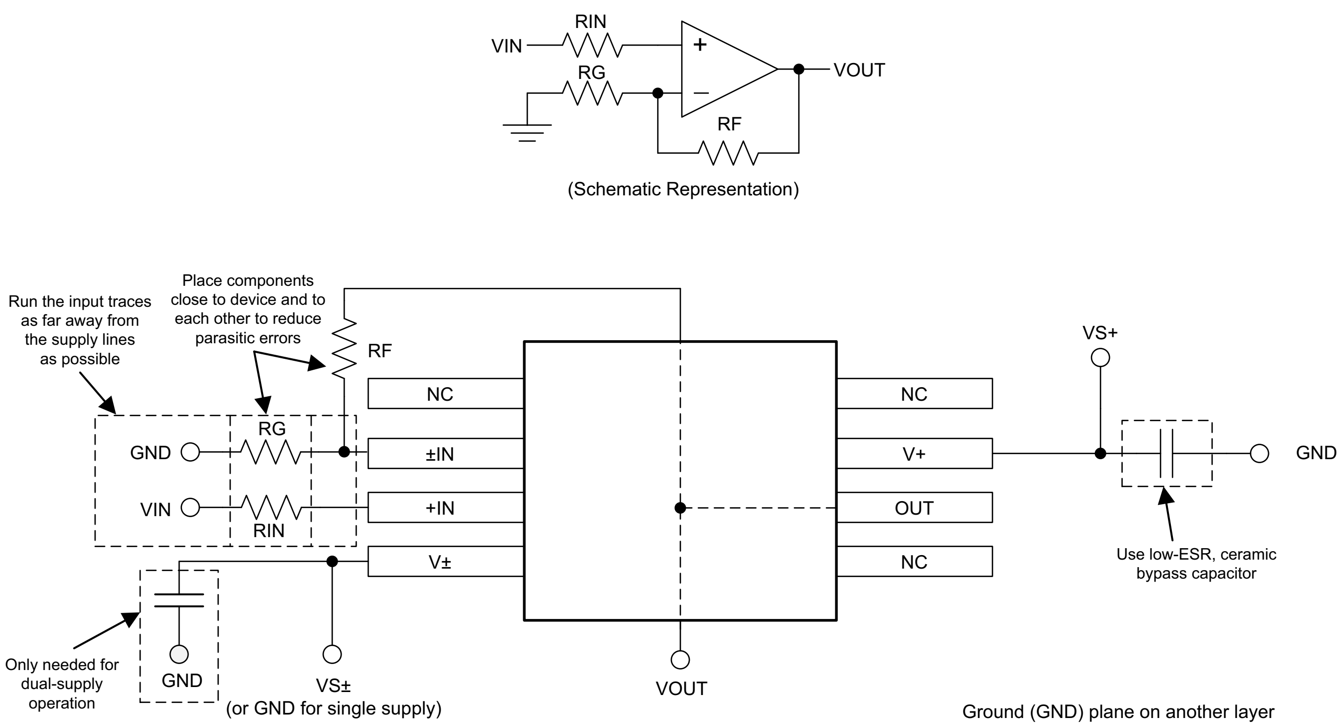



**Figure 46. Operational Amplifier Board Layout for Noninverting Configuration**

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| OPA171 | Click here | Click here | Click here | Click here | Click here |
| OPA2171 | Click here | Click here | Click here | Click here | Click here |
| OPA4171 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA171AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | O171A | Samples |
| OPA171AIDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OSUI | Samples |
| OPA171AIDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OSUI | Samples |
| OPA171AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | O171A | Samples |
| OPA171AIDRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DAP | Samples |
| OPA171AIDRLT | ACTIVE | SOT | DRL | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DAP | Samples |
| OPA2171AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2171A | Samples |
| OPA2171AIDCUR | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OPOC | Samples |
| OPA2171AIDCUT | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OPOC | Samples |
| OPA2171AIDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | OPMI | Samples |
| OPA2171AIDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | OPMI | Samples |
| OPA2171AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2171A | Samples |
| OPA4171AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | OPA4171 | Samples |
| OPA4171AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | OPA4171 | Samples |
| OPA4171AIPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA4171 | Samples |
| OPA4171AIPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPA4171 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA171, OPA2171, OPA4171 :**

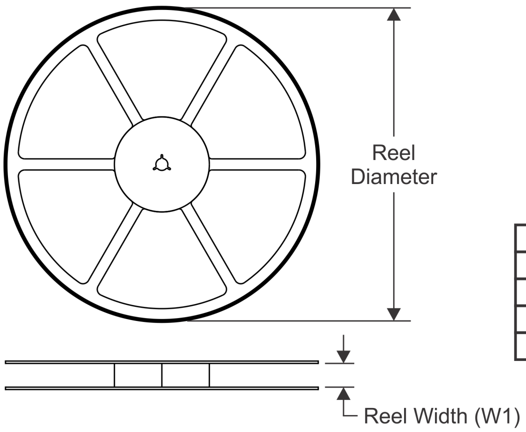
- Automotive: OPA171-Q1, OPA2171-Q1, OPA4171-Q1

NOTE: Qualified Version Definitions:

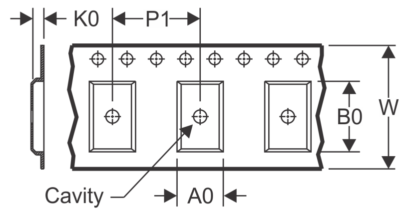
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

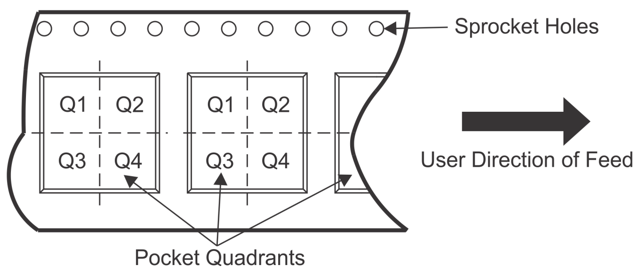



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

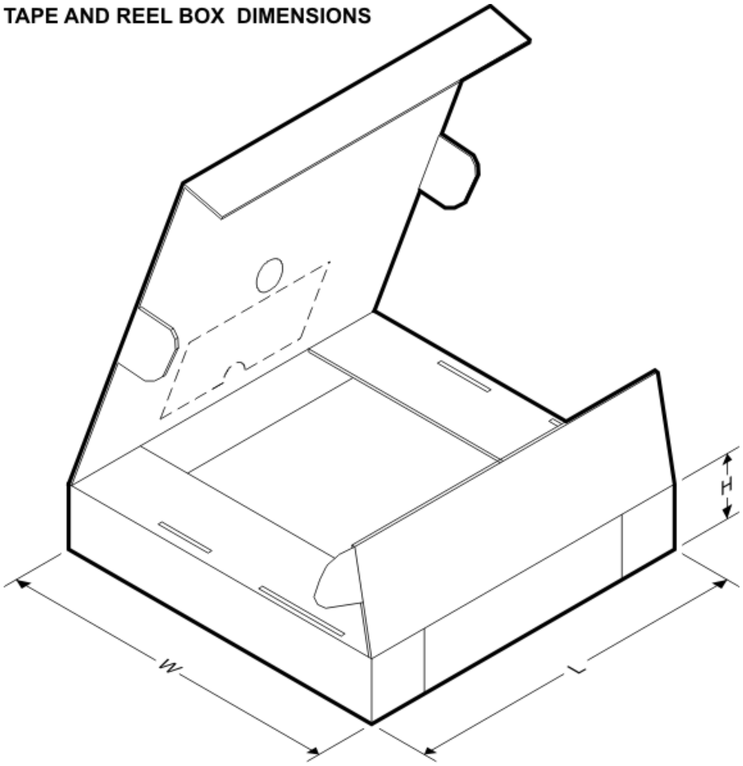
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA171AIDBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA171AIDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA171AIDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| OPA171AIDBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA171AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA171AIDRLR | SOT | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| OPA171AIDRLT | SOT | DRL | 5 | 250 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| OPA2171AIDCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| OPA2171AIDCUT | VSSOP | DCU | 8 | 250 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| OPA2171AIDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2171AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA4171AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4171AIPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

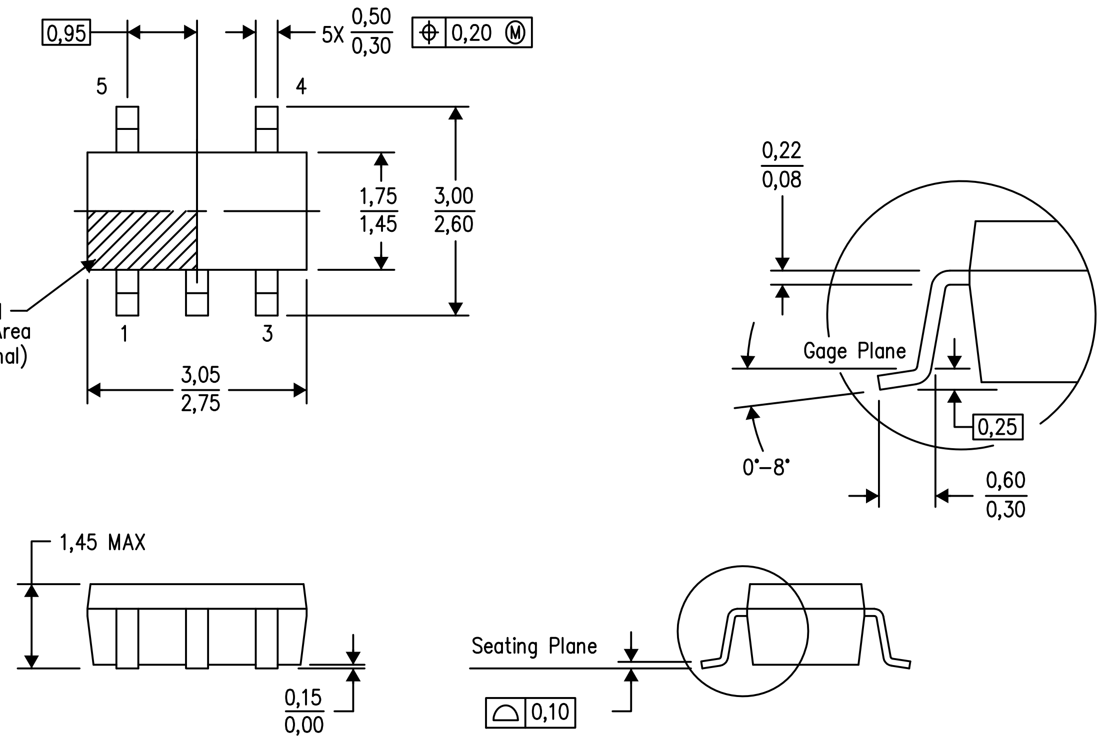
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA171AIDBVR | SOT-23 | DBV | 5 | 3000 | 195.0 | 200.0 | 45.0 |
| OPA171AIDBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| OPA171AIDBVT | SOT-23 | DBV | 5 | 250 | 223.0 | 270.0 | 35.0 |
| OPA171AIDBVT | SOT-23 | DBV | 5 | 250 | 195.0 | 200.0 | 45.0 |
| OPA171AIDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA171AIDRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| OPA171AIDRLT | SOT | DRL | 5 | 250 | 202.0 | 201.0 | 28.0 |
| OPA2171AIDCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| OPA2171AIDCUT | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| OPA2171AIDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2171AIDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA4171AIDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| OPA4171AIPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

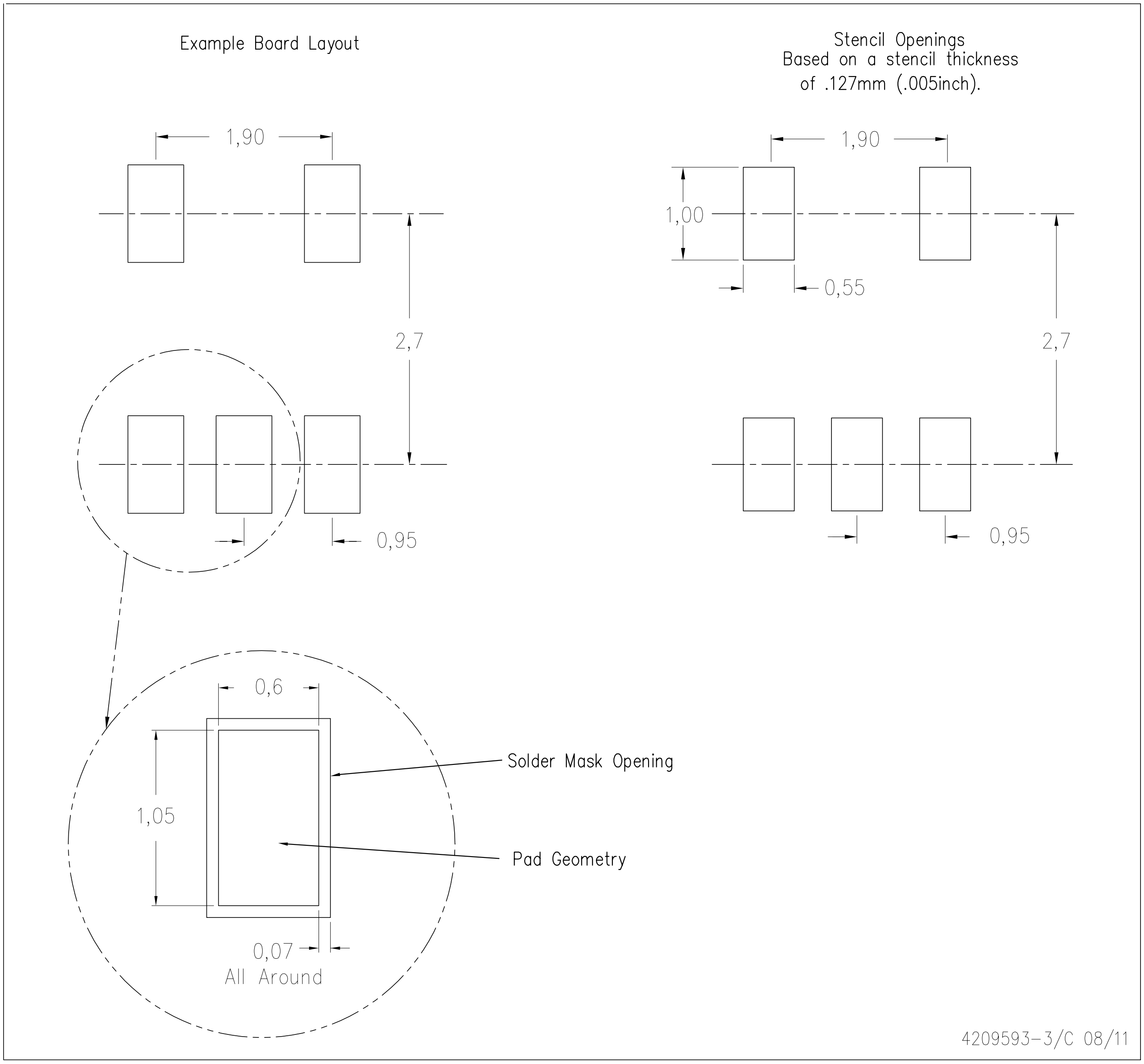
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE




4073253-4/N 12/14

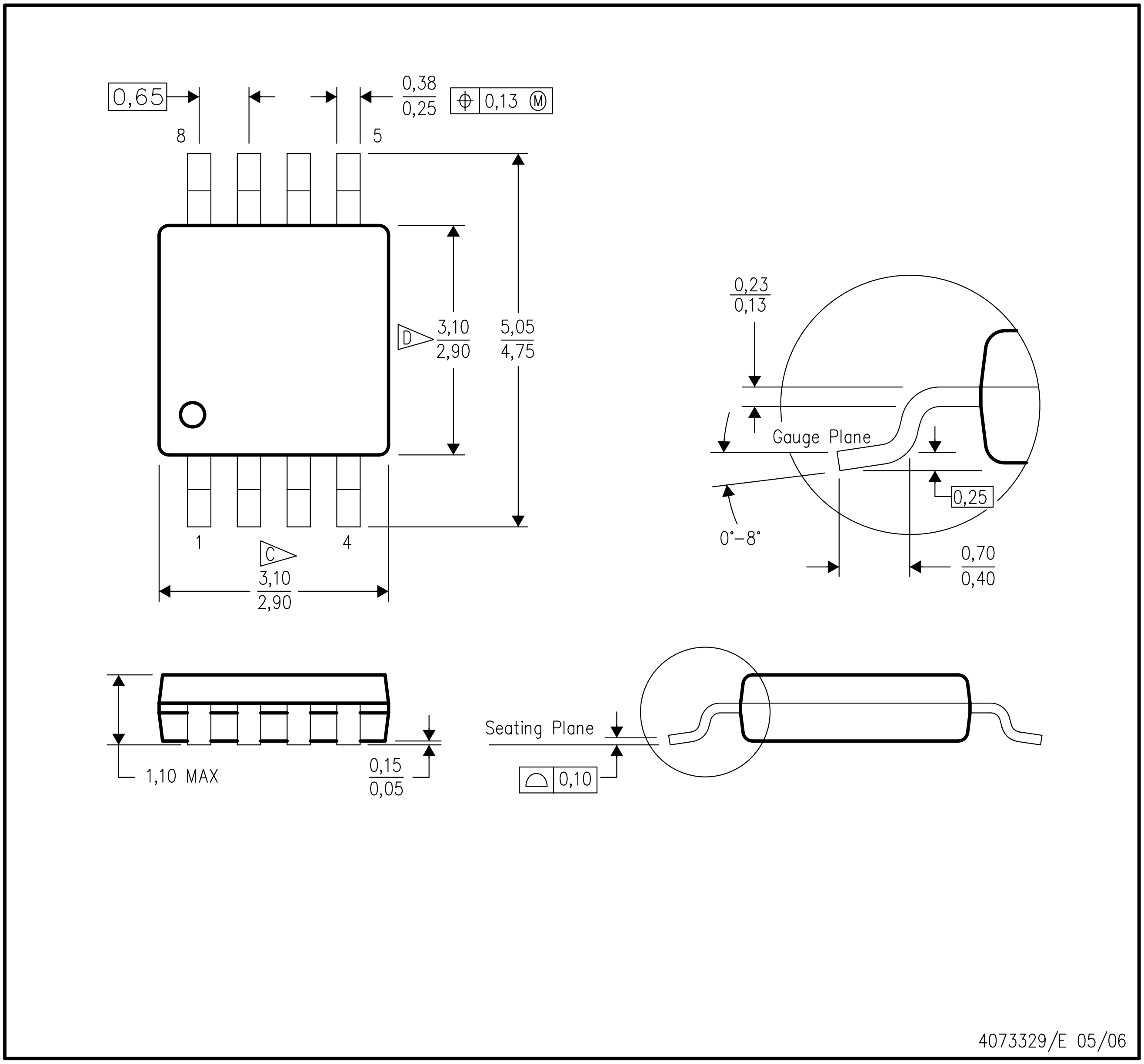
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



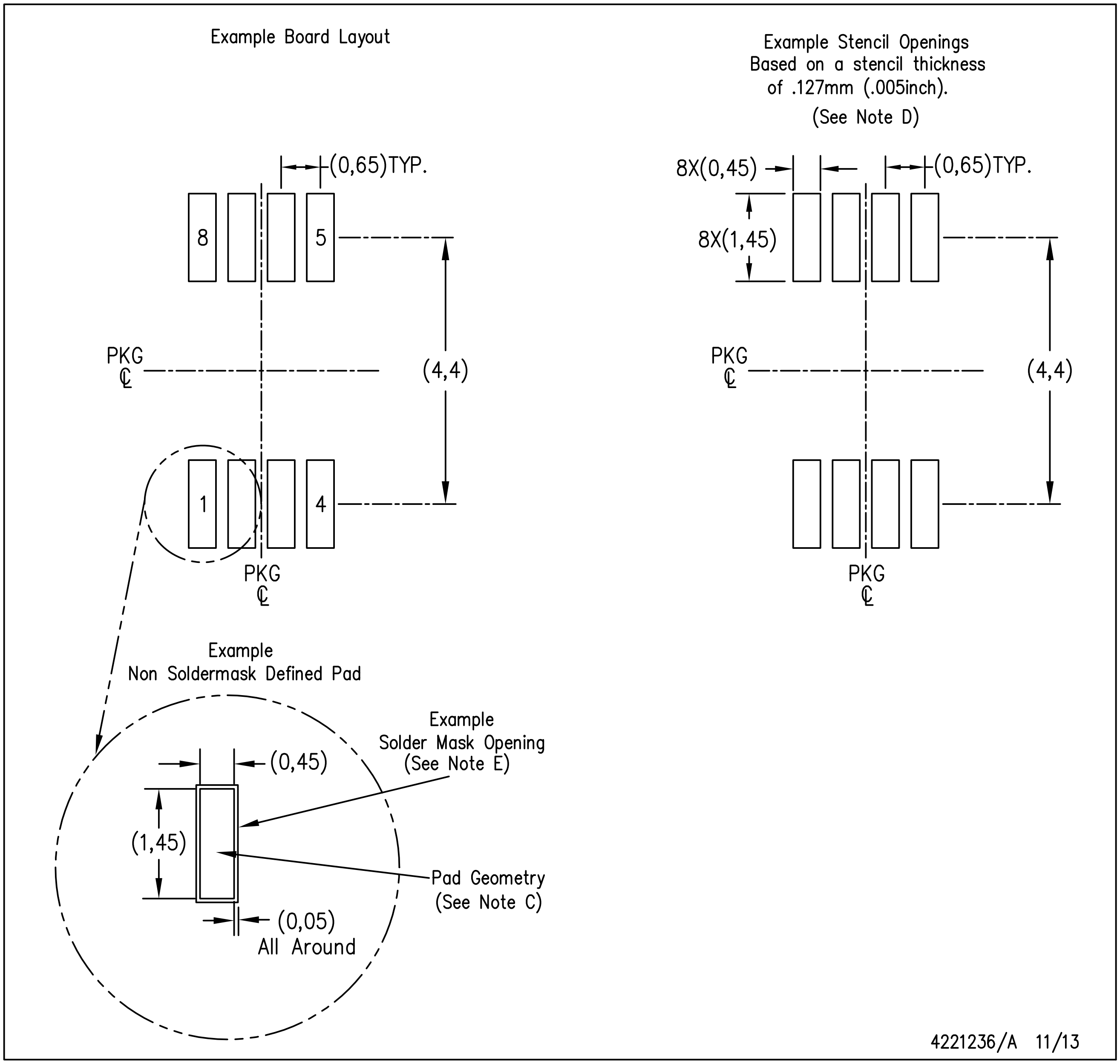

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



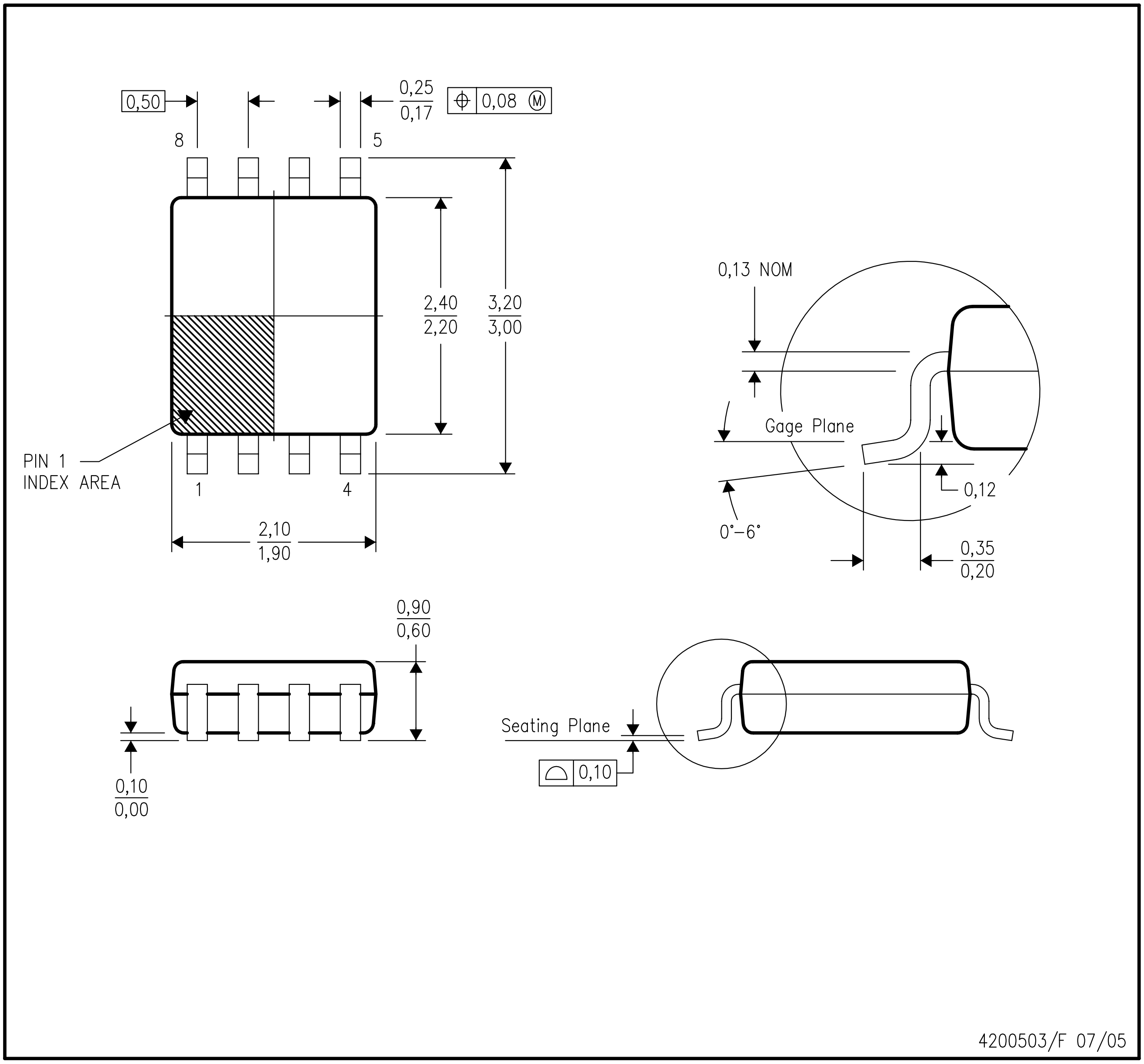

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



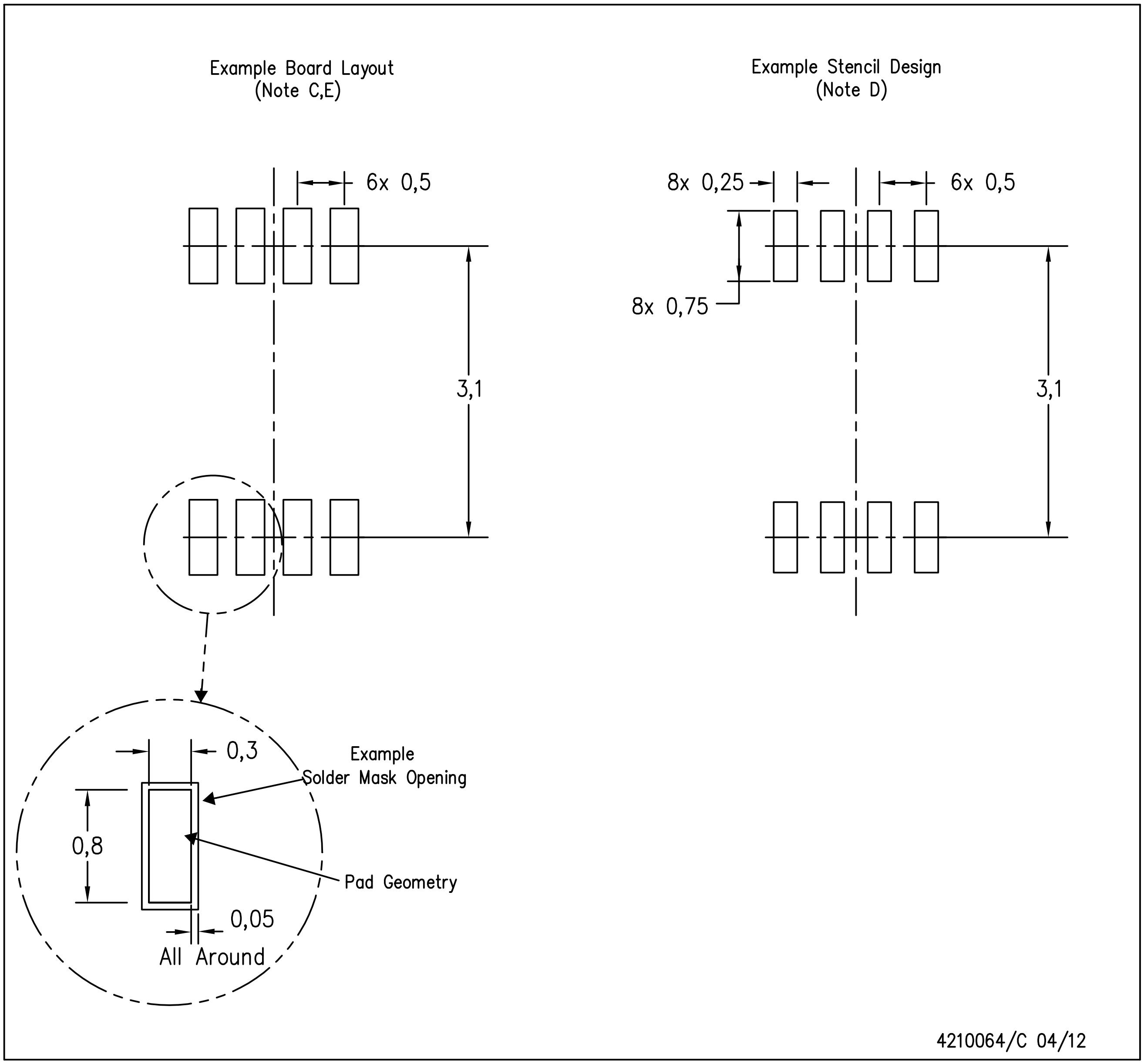

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

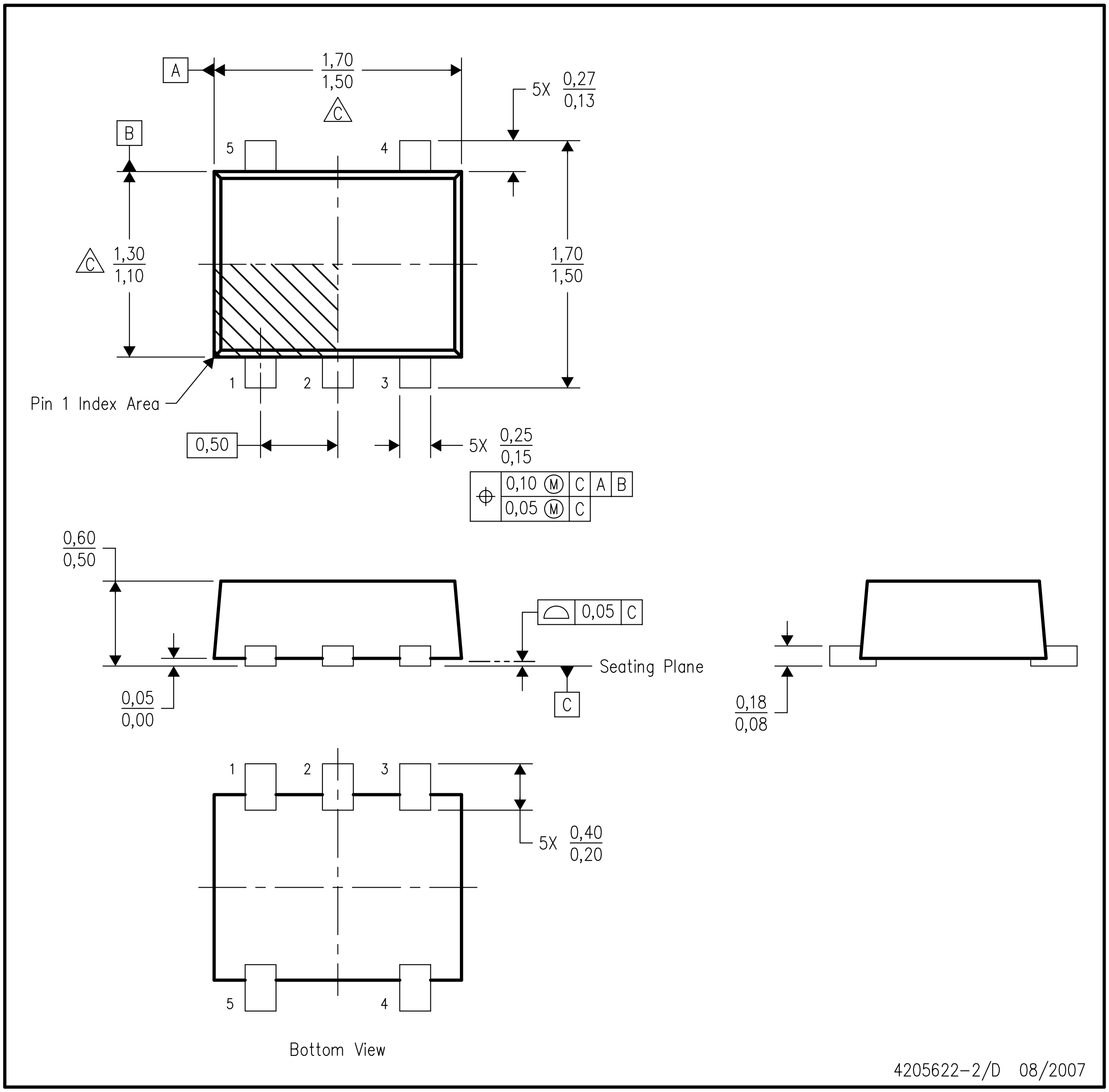



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

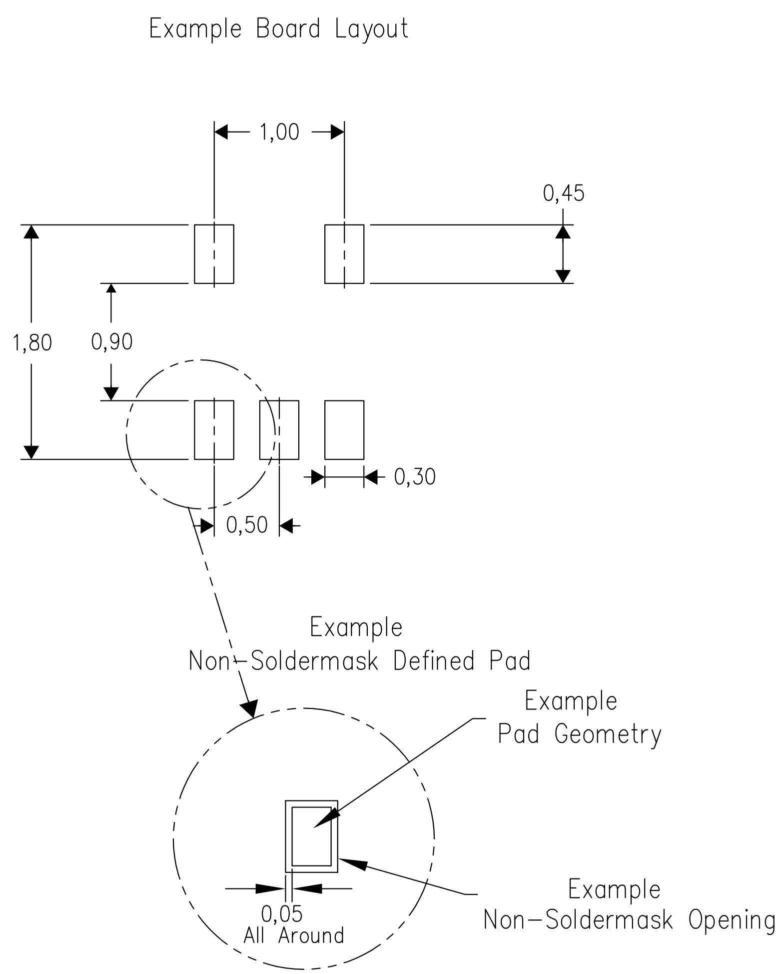



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

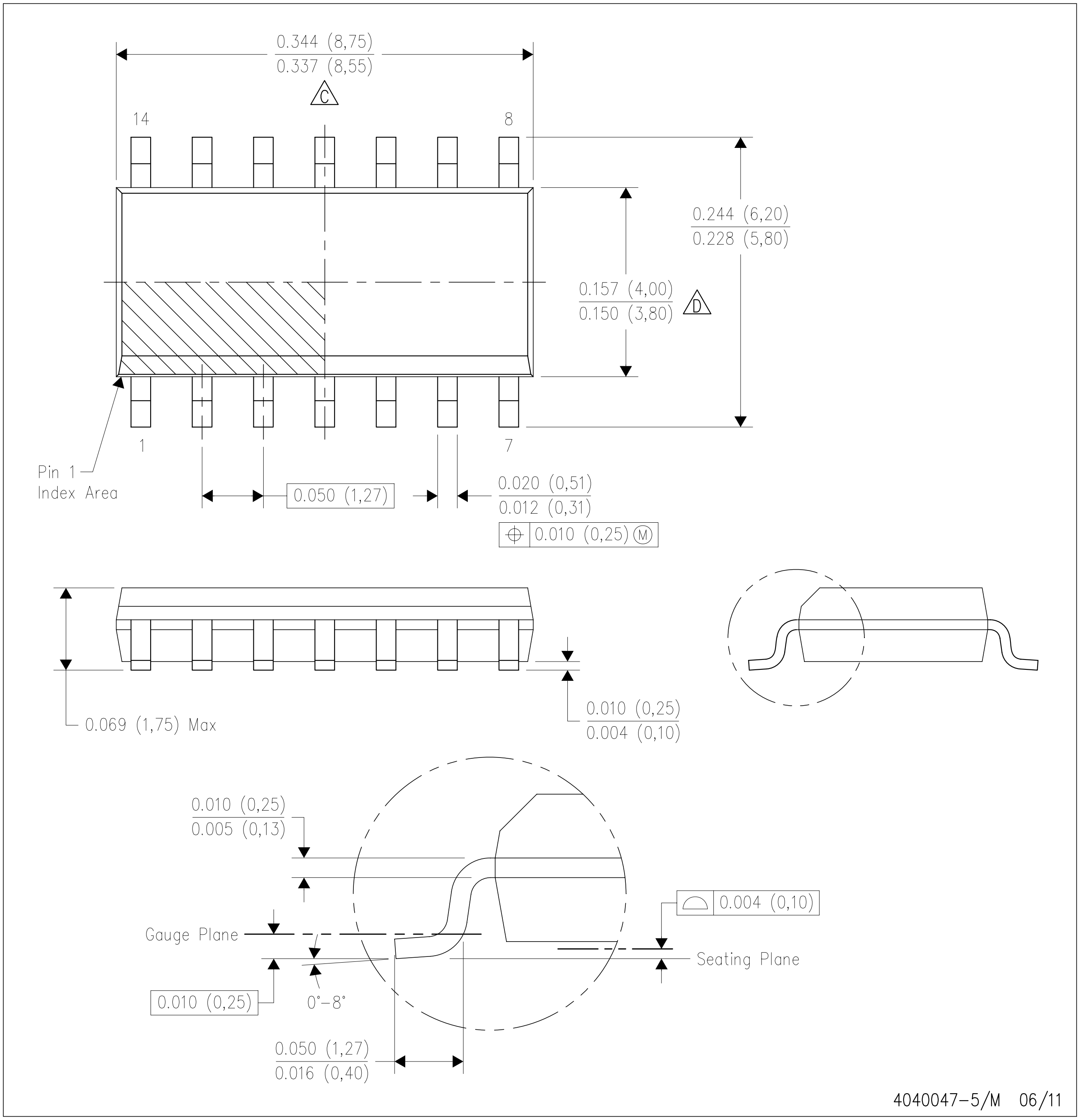
DRL (R-PDSO-N5) PLASTIC SMALL OUTLINE




4208207-2/E 06/12

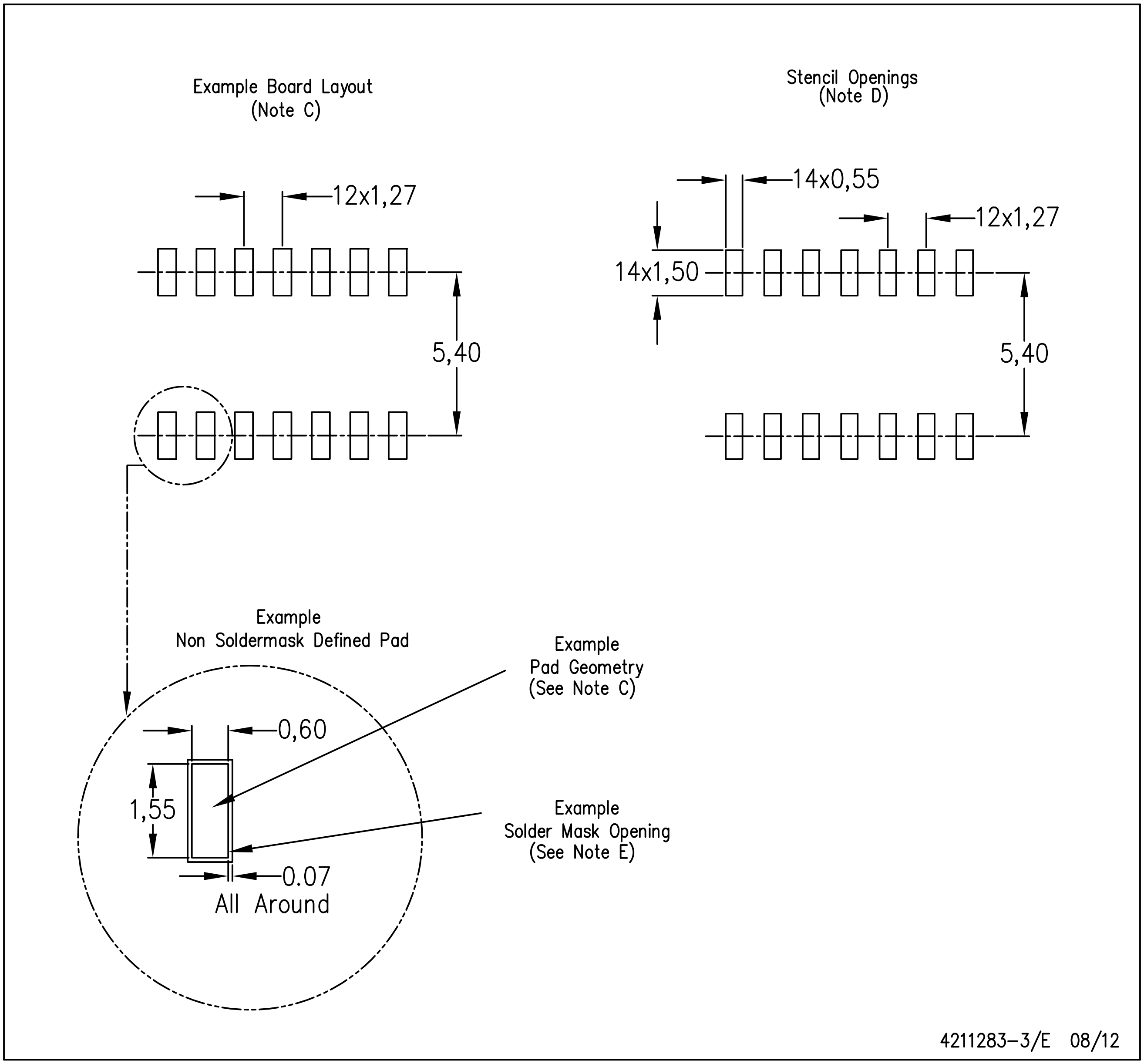
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



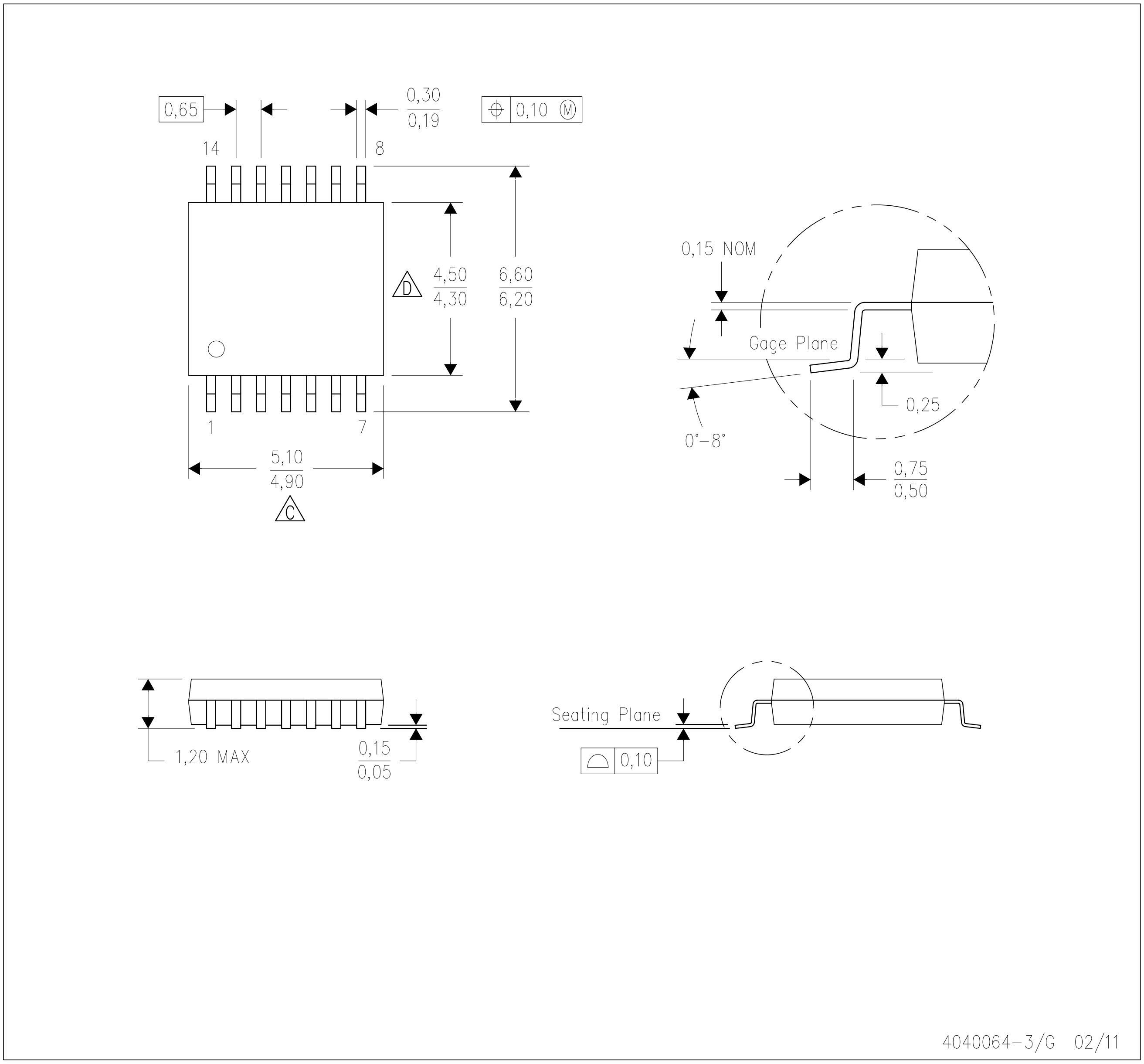

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



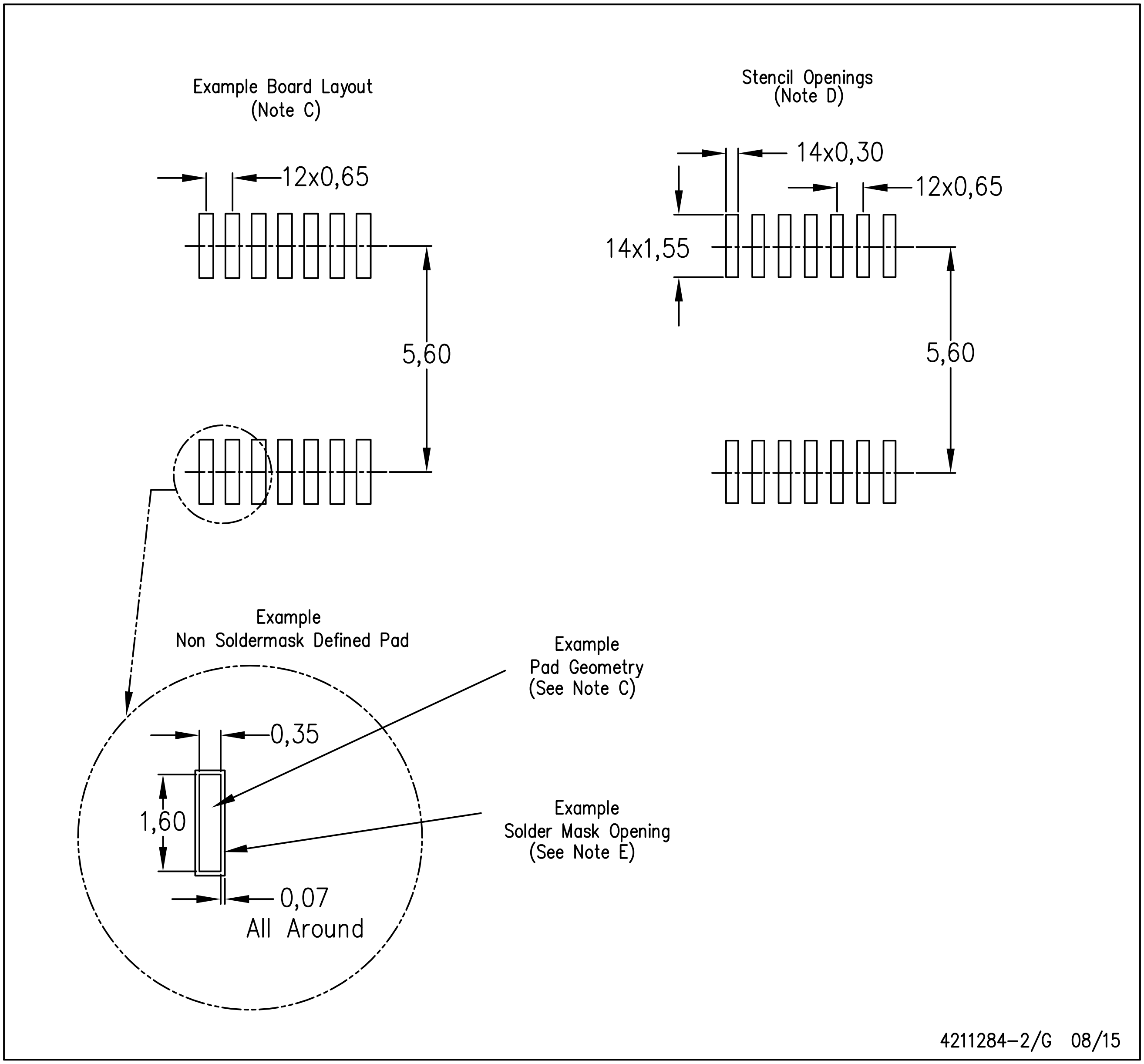

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



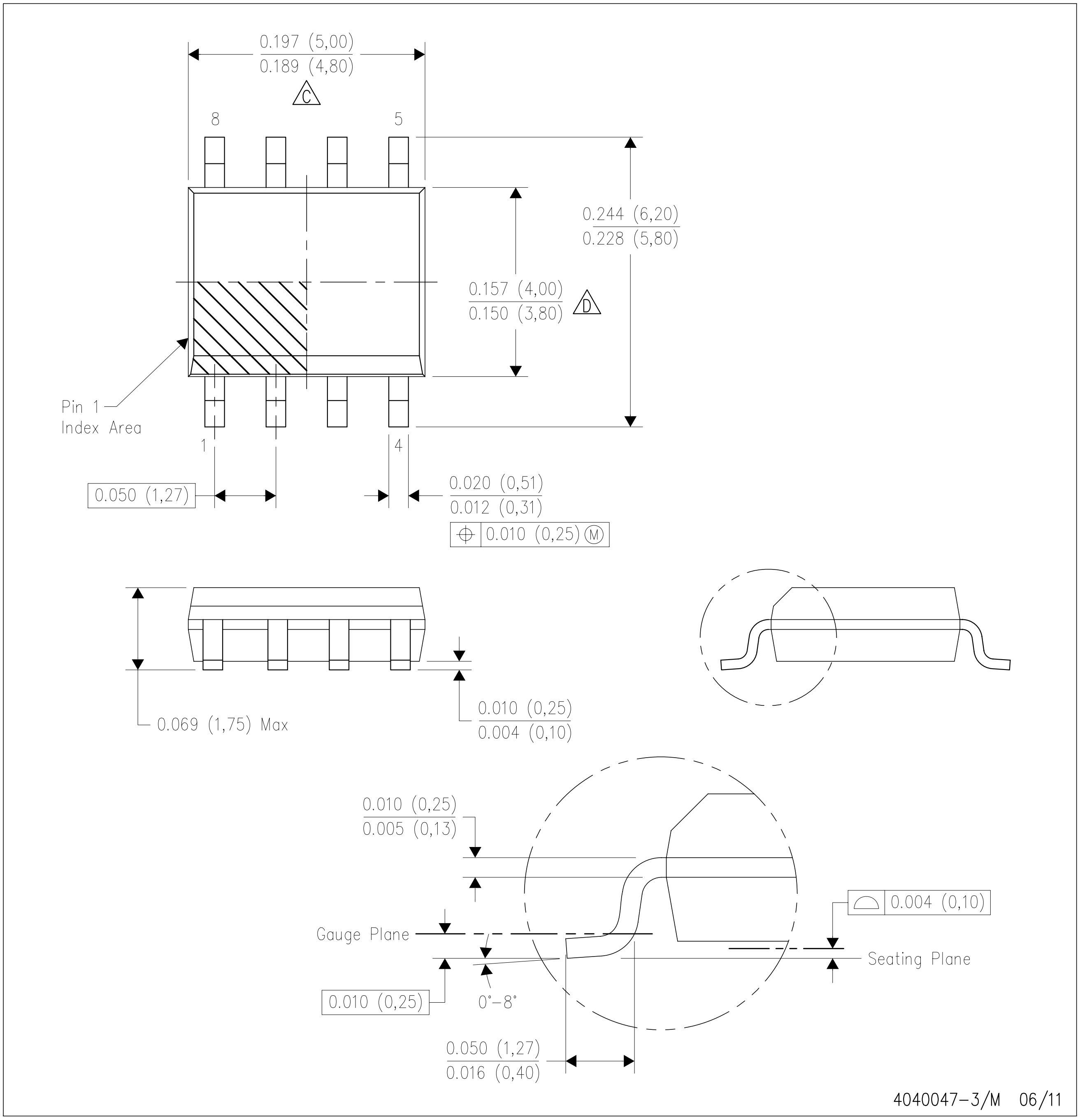

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



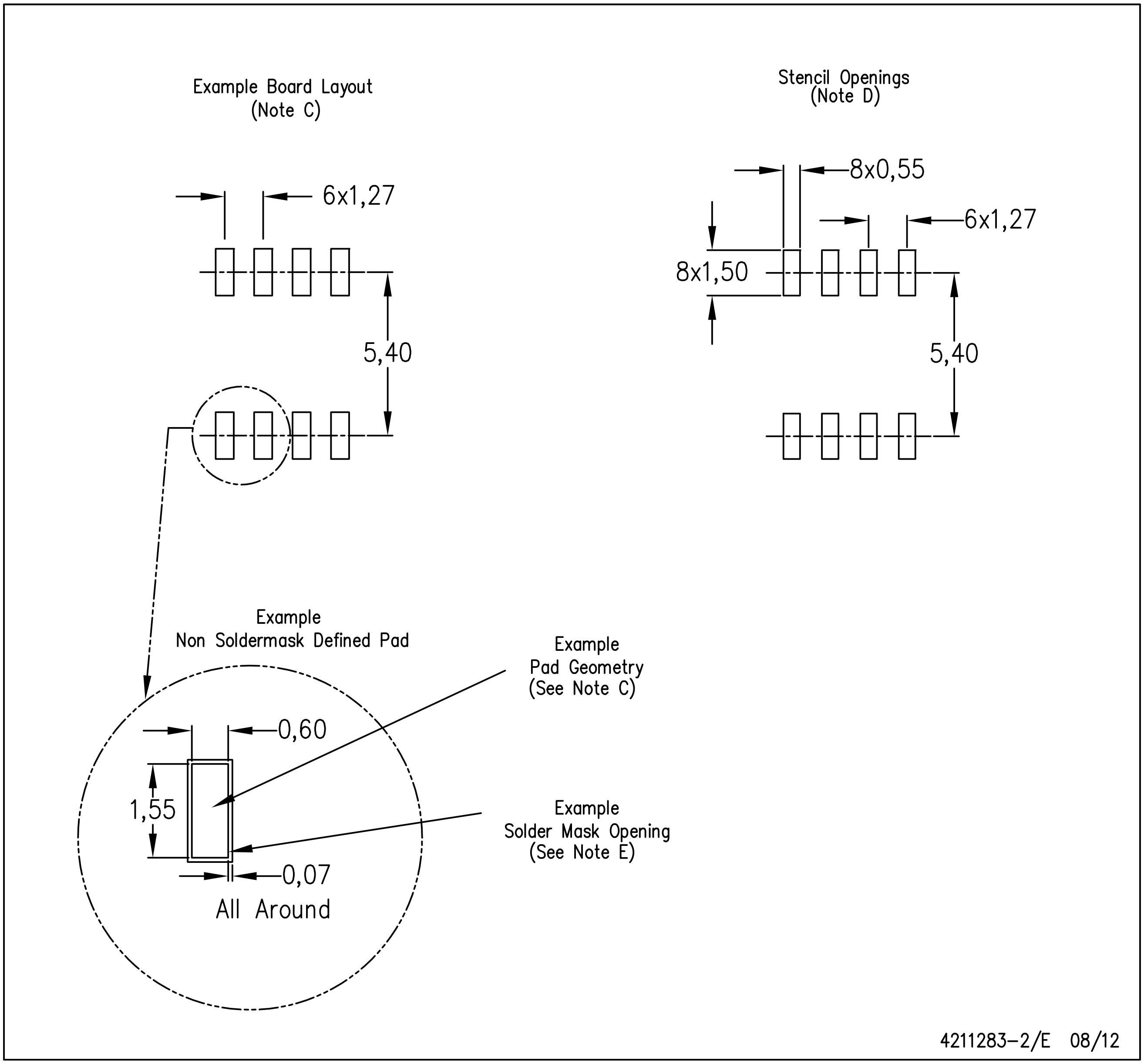

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE



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