36V, Single-Supply, SOT553, General-Purpose OPERATIONAL AMPLIFIERS

Check for Samples: OPA171, OPA2171, OPA4171

FEATURES

- **Supply Range: +2.7V to +36V, ±1.35V to ±18V**
- **Low Noise: 14nV/√Hz**
- **Low Offset Drift: ±0.3μV/°C (typ)**
- **RFI Filtered Inputs**
- **Input Range Includes the Negative Supply**
- **Input Range Operates to Positive Supply**
- **Rail-to-Rail Output**
- **Gain Bandwidth: 3MHz**
- **Low Quiescent Current: 475μA per Amplifier**
- **High Common-Mode Rejection: 120dB (typ)**
- **Low Input Bias Current: 8pA**
- **Industry-Standard Packages:**
  - **8-Pin SOIC**
  - **8-Pin MSOP**
  - **14-Pin TSSOP**
- ***micro*Packages:**
  - **Single in SOT553**
  - **Dual in VSSOP-8**

APPLICATIONS

- **Tracking Amplifier in Power Modules**
- **Merchant Power Supplies**
- **Transducer Amplifiers**
- **Bridge Amplifiers**
- **Temperature Measurements**
- **Strain Gauge Amplifiers**
- **Precision Integrators**
- **Battery-Powered Instruments**
- **Test Equipment**

Product Family

DEVICE	PACKAGE
OPA171	SOT553, SOT23-5, SO-8
OPA2171 (dual)	VSSOP-8, SO-8, MSOP-8
OPA4171 (quad)	TSSOP-14, SO-14

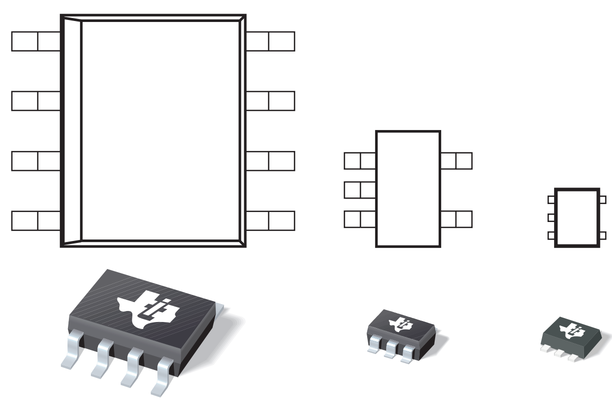
DESCRIPTION

The OPA171, OPA2171 and OPA4171 (OPAx171) are a family of 36V, single-supply, low-noise operational amplifiers with the ability to operate on supplies ranging from +2.7V (±1.35V) to +36V (±18V). These devices are available in micro-packages and offer low offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps, which are specified at only one supply voltage, the OPAx171 family is specified from +2.7V to +36V. Input signals beyond the supply rails do not cause phase reversal. The OPAx171 family is stable with capacitive loads up to 300pF. The input can operate 100mV below the negative rail and within 2V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail.

The OPAx171 series of op amps are specified from –40°C to +125°C.

Package Footprint Comparison (to Scale)



Package Height Comparison (to Scale)

Smallest Packaging for 36V Op Amps

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION (1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA171	SOT553	DRL	DAP	OPA171AIDRLT	Tape and Reel, 250
				OPA171AIDRLR	Tape and Reel, 4000
	SOT23-5	DBV	OSUI	OPA171AIDBVT	Tape and Reel, 250
				OPA171AIDBVR	Tape and Reel, 3000
	SO-8	D	O171A	OPA171AID	Rail, 75
				OPA171AIDR	Tape and Reel, 2500
OPA2171	MSOP-8	DGK	OPMI	OPA2171AIDGK	Rail, 80
				OPA2171AIDGKR	Tape and Reel, 2500
	VSSOP-8	DCU	OPOC	OPA2171AIDCUT	Tape and Reel, 250
				OPA2171AIDCUR	Tape and Reel, 3000
	SO-8	D	2171A	OPA2171AID	Rail, 75
				OPA2171AIDR	Tape and Reel, 2500
OPA4171	SO-14	D	OPA4171	OPA4171AID	Rail, 50
				OPA4171AIDR	Tape and Reel, 2500
	TSSOP-14	PW	OPA4171	OPA4171AIPW	Rail, 90
				OPA4171AIPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPAx171	UNIT
Supply voltage		±20	V
Signal input terminals	Voltage	(V–) – 0.5 to (V+) + 0.5	V
	Current	±10	mA
Output short circuit(2)		Continuous	
Operating temperature		–55 to +150	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
ESD ratings:	Human body model (HBM)	4	kV
	Charged device model (CDM)	750	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, V_S = +2.7V to +36V, V_{CM} = V_{OUT} = V_S/2, and R_{LOAD} = 10kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA171, OPA2171, OPA4171 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.25	±1.8	mV
Over temperature				**0.3**	**±2**	**mV**
Drift	**dV_{OS}/dT**			**0.3**	**±2**	**μV/°C**
vs power supply	**PSRR**	**V_S = +4V to +36V**		**1**	**±3**	**μV/V**
Channel separation, dc		dc		5		μV/V
INPUT BIAS CURRENT						
Input bias current	I_B			±8	±15	pA
Over temperature					**±3.5**	**nA**
Input offset current	I_{OS}			±4		pA
Over temperature					**±3.5**	**nA**
NOISE						
Input voltage noise		f = 0.1Hz to 10Hz		3		$μV_{PP}$
Input voltage noise density	e_n	f = 100Hz		25		nV/√Hz
		f = 1kHz		14		nV/√Hz
INPUT VOLTAGE						
Common-mode voltage range(1)	V_{CM}		(V–) – 0.1V		(V+) – 2V	V
Common-mode rejection ratio	**CMRR**	**V_S = ±2V, (V–) – 0.1V < V_{CM} < (V+) – 2V**	**90**	**104**		**dB**
		V_S = ±18V, (V–) – 0.1V < V_{CM} < (V+) – 2V	**104**	**120**		**dB**
INPUT IMPEDANCE						
Differential				100 || 3		MΩ || pF
Common-mode				6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain	**A_{OL}**	**V_S = +4V to +36V, (V–) + 0.35V < V_O < (V+) – 0.35V**	**110**	**130**		**dB**
FREQUENCY RESPONSE						
Gain bandwidth product	GBP			3.0		MHz
Slew rate	SR	G = +1		1.5		V/μs
Settling time	t_S	To 0.1%, V_S = ±18V, G = +1, 10V step		6		μs
		To 0.01% (12 bit), V_S = ±18V, G = +1, 10V step		10		μs
Overload recovery time		V_{IN} × Gain > V_S		2		μs
Total harmonic distortion + noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$		0.0002		%
OUTPUT						
Voltage output swing from rail	V_O	V_S = 5V, R_L = 10kΩ		30		mV
Over temperature		**R_L = 10kΩ, A_{OL} ≥ 110dB**	**(V–) + 0.35**		**(V+) – 0.35**	**V**
Short-circuit current	I_{SC}			+25/–35		mA
Capacitive load drive	C_{LOAD}			See Typical Characteristics		pF
Open-loop output resistance	R_O	f = 1MHz, I_O = 0A		150		Ω
POWER SUPPLY						
Specified voltage range	V_S		+2.7		+36	V
Quiescent current per amplifier	I_Q	I_O = 0A		475	595	μA
Over temperature		**I_O = 0A**			**650**	**μA**
TEMPERATURE						
Specified range			–40		+125	°C
Operating range			–55		+150	°C

(1) The input range can be extended beyond (V+) – 2V up to V+. See the *Typical Characteristics* and *Application Information* sections for additional information.

THERMAL INFORMATION: OPA171

THERMAL METRIC[1]		OPA171			UNITS
		D (SO)	DBV (SOT23)	DRL (SOT553)	
		8 PINS	5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	97.9	133.9	0.1	
θ_{JB}	Junction-to-board thermal resistance	87.7	83.6	42.4	
ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	
ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA2171

THERMAL METRIC[1]		OPA2171			UNITS
		D (SO)	DCU (VSSOP)	DGK (MSOP)	
		8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	134.3	175.2	195.3	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	72.1	74.9	59.4	
θ_{JB}	Junction-to-board thermal resistance	60.6	22.2	115.1	
ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	4.7	
ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	114.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

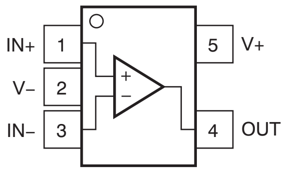
THERMAL INFORMATION: OPA4171

THERMAL METRIC[1]		OPA4171		UNITS
		D (SO)	PW (TSSOP)	
		14 PINS	14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	
θ_{JB}	Junction-to-board thermal resistance	49.4	59.3	
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	

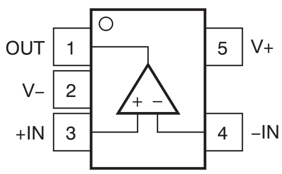
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

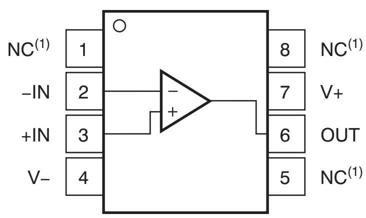
DRL PACKAGE: OPA171
SOT-553
(TOP VIEW)



DBV PACKAGE: OPA171
SOT23-5
(TOP VIEW)

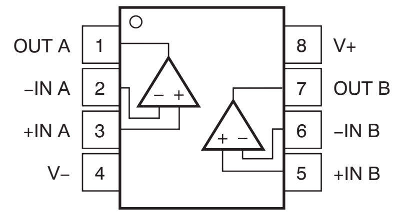


D PACKAGE: OPA171
SO-8
(TOP VIEW)

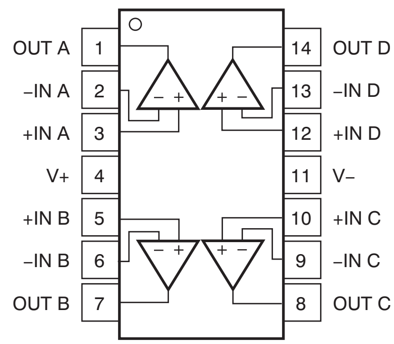


(1) No internal connection.

D, DCU, AND DGK PACKAGES: OPA2171
SO-8, VSSOP-8, AND MSOP-8
(TOP VIEW)



D AND PW PACKAGES: OPA4171
SO-14 AND TSSOP-14
(TOP VIEW)



TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

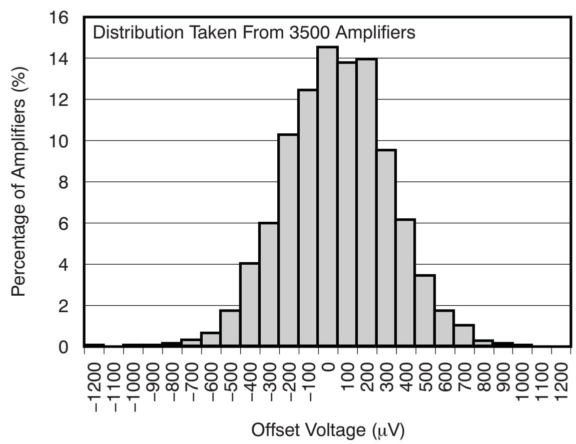

Figure 1.

OFFSET VOLTAGE DRIFT DISTRIBUTION

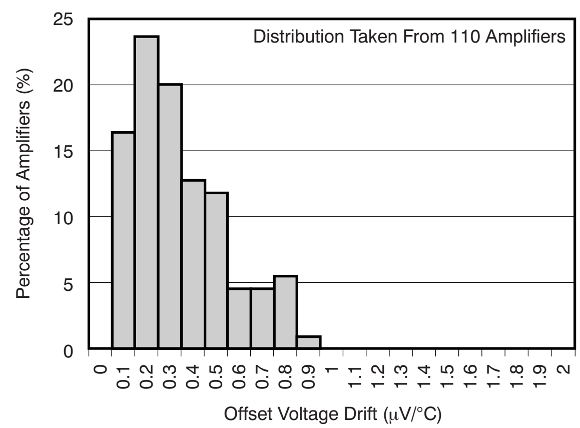

Figure 2.

OFFSET VOLTAGE vs TEMPERATURE

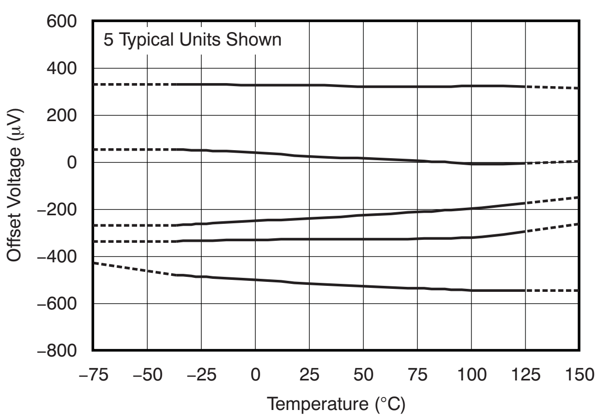

Figure 3.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

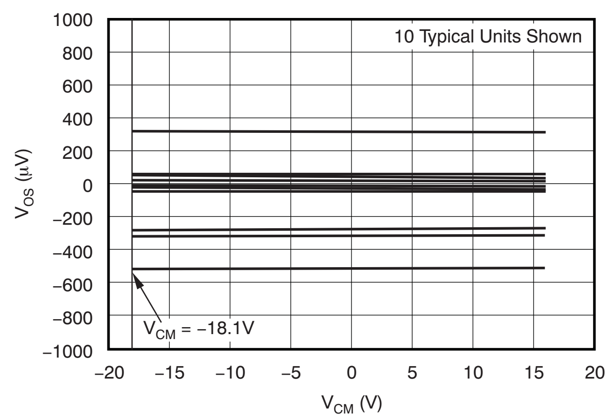

Figure 4.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (Upper Stage)

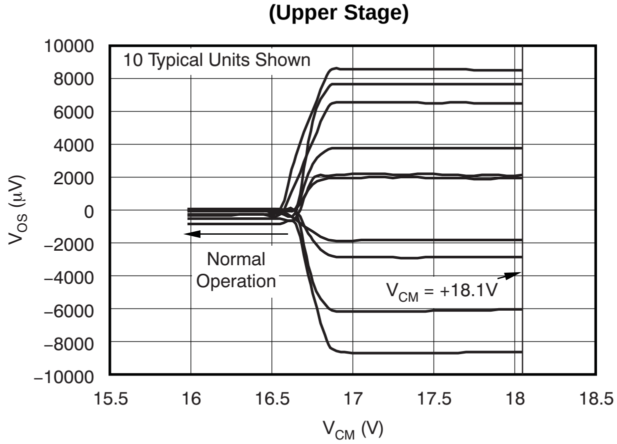

Figure 5.

OFFSET VOLTAGE vs POWER SUPPLY

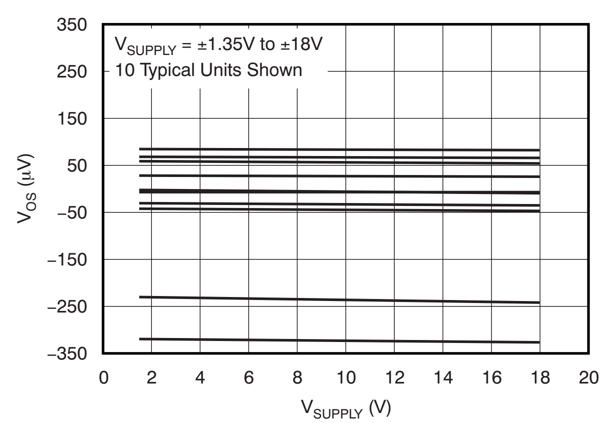

Figure 6.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

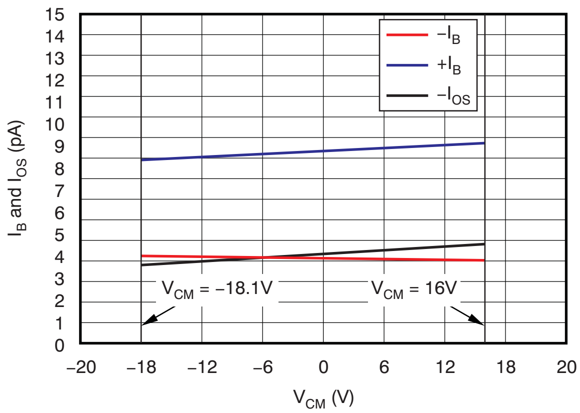

Figure 7.

INPUT BIAS CURRENT vs TEMPERATURE

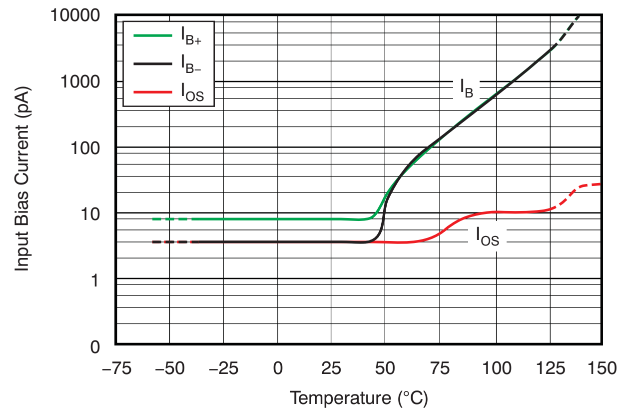

Figure 8.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

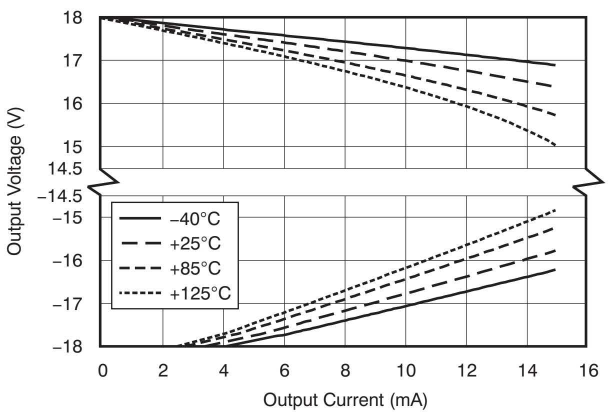

Figure 9.

CMRR AND PSRR vs FREQUENCY (Referred-to Input)

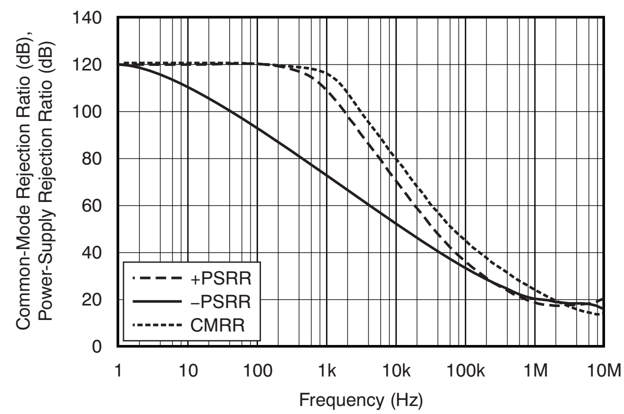

Figure 10.

CMRR vs TEMPERATURE

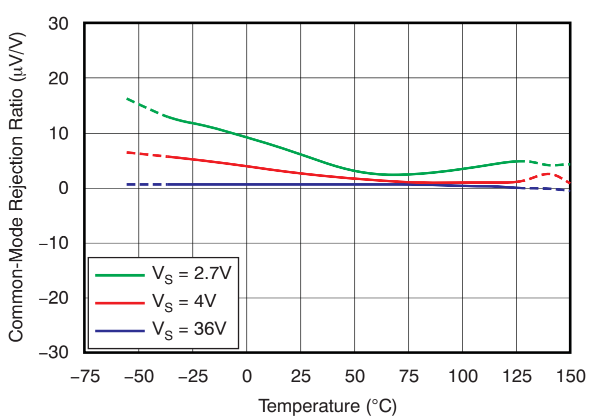

Figure 11.

PSRR vs TEMPERATURE

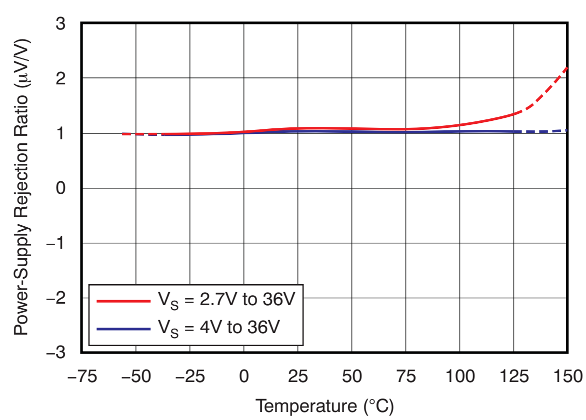

Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

0.1Hz TO 10Hz NOISE

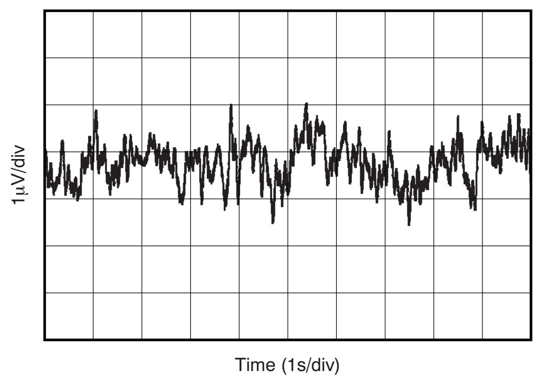

Figure 13.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

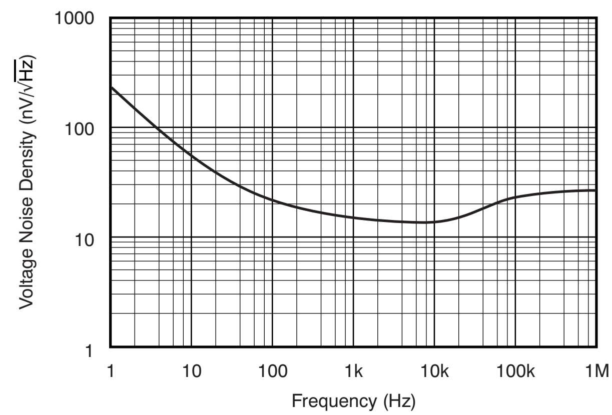

Figure 14.

THD+N RATIO vs FREQUENCY

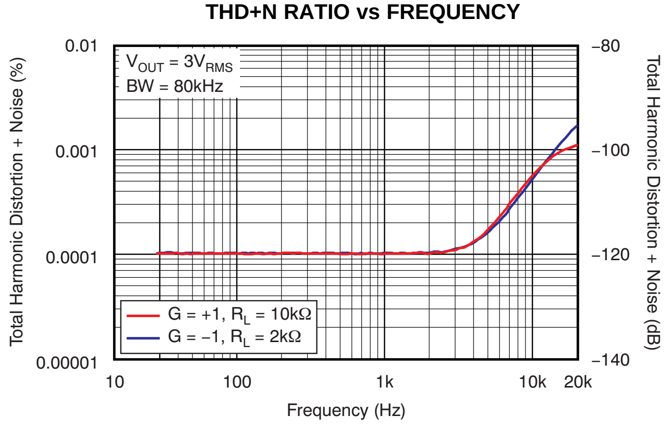

Figure 15.

THD+N vs OUTPUT AMPLITUDE

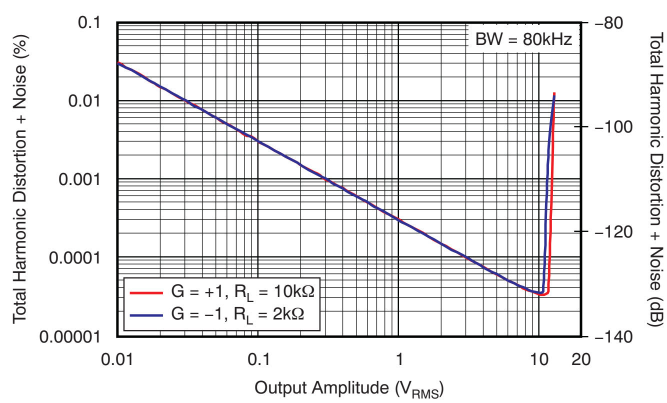

Figure 16.

QUIESCENT CURRENT vs TEMPERATURE

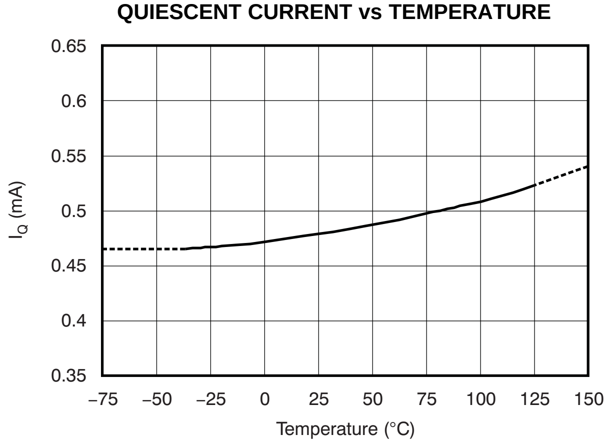

Figure 17.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

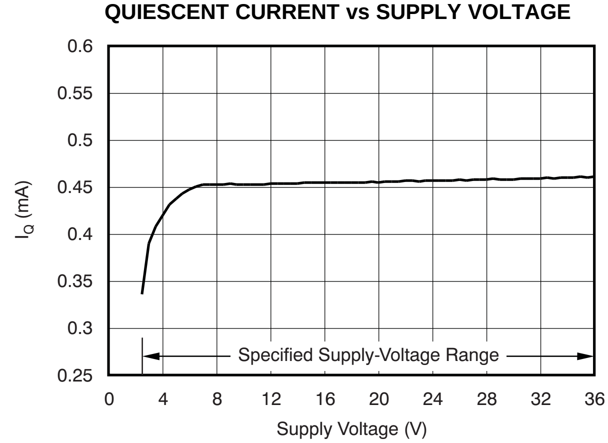

Figure 18.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

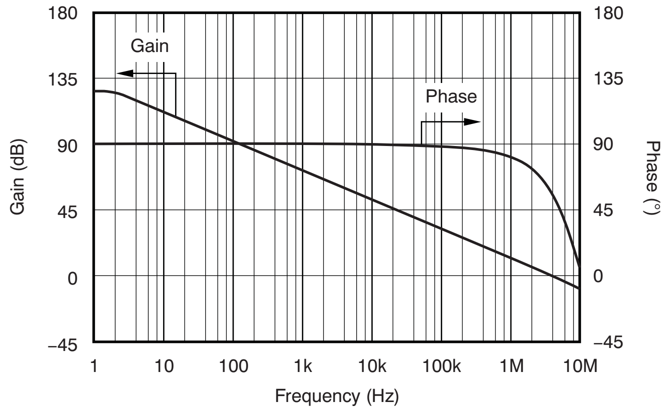

Figure 19.

CLOSED-LOOP GAIN vs FREQUENCY

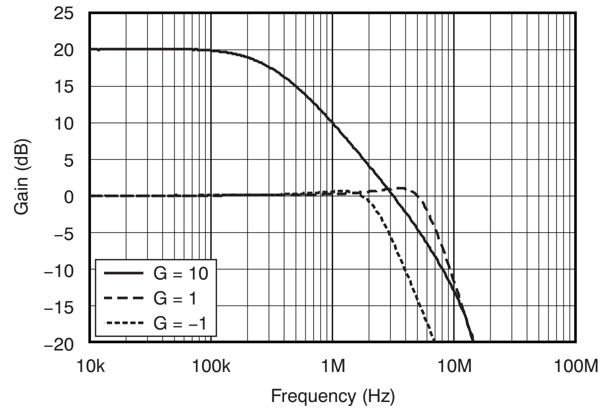

Figure 20.

OPEN-LOOP GAIN vs TEMPERATURE

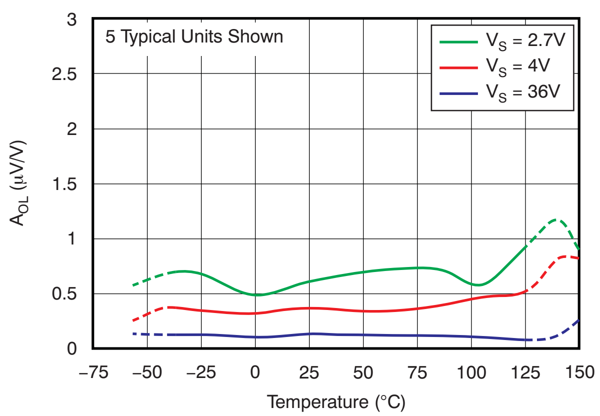

Figure 21.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

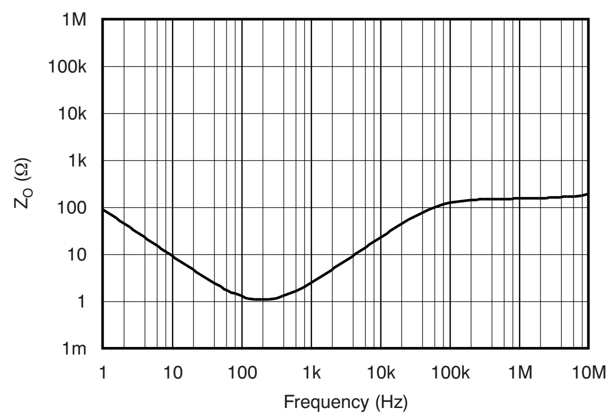

Figure 22.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

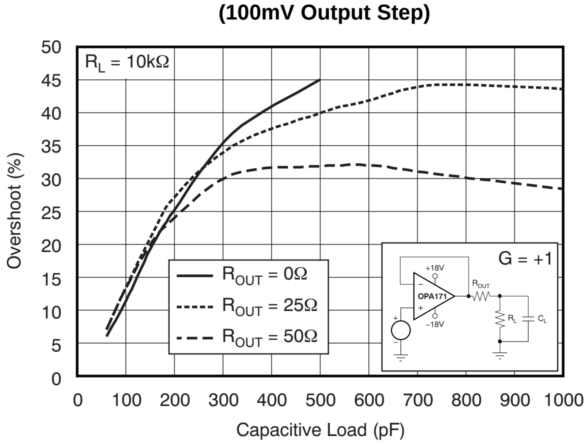

Figure 23.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

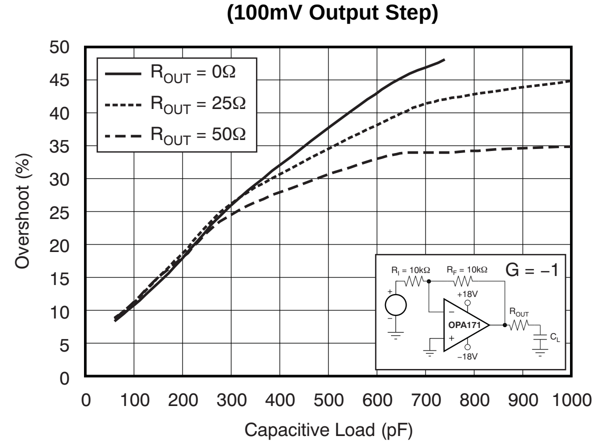

Figure 24.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

NO PHASE REVERSAL

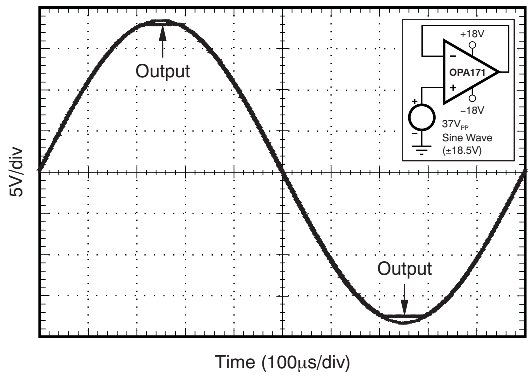

Figure 25.

POSITIVE OVERLOAD RECOVERY

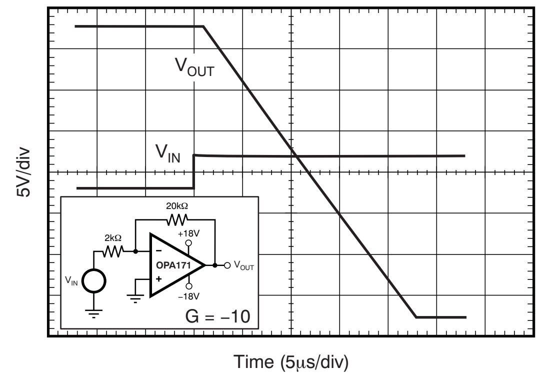

Figure 26.

NEGATIVE OVERLOAD RECOVERY

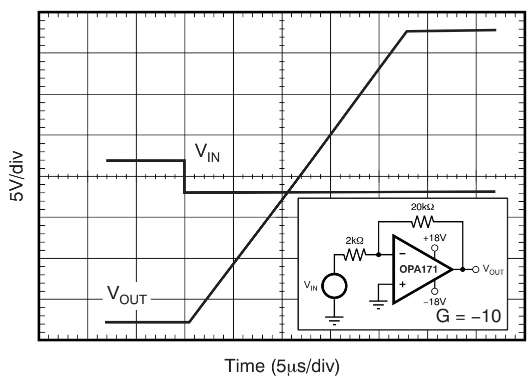

Figure 27.

SMALL-SIGNAL STEP RESPONSE (100mV)

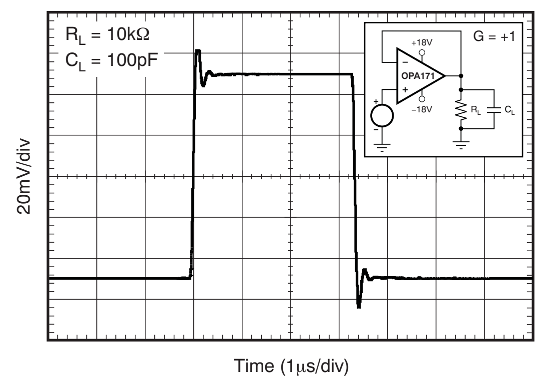

Figure 28.

SMALL-SIGNAL STEP RESPONSE (100mV)

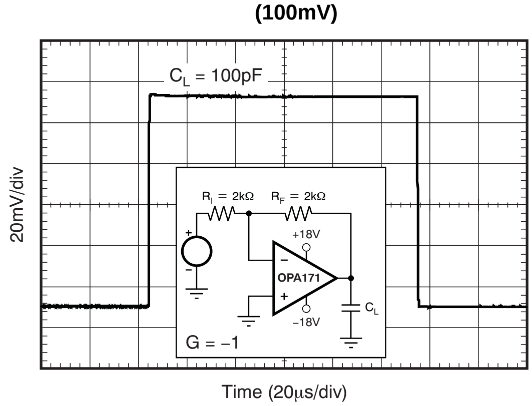

Figure 29.

LARGE-SIGNAL STEP RESPONSE

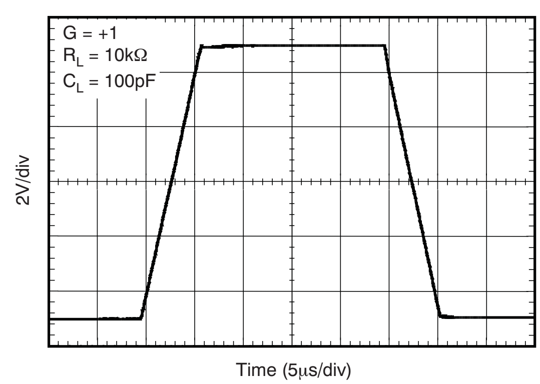

Figure 30.

TYPICAL CHARACTERISTICS (continued)

V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

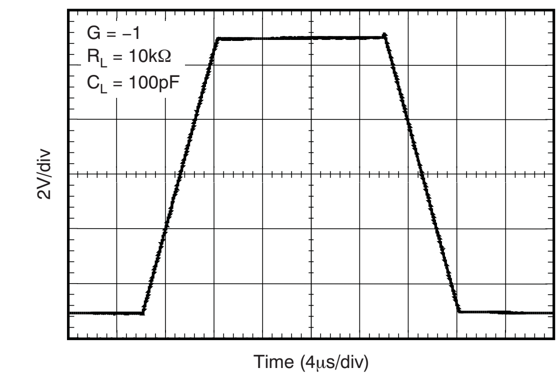

Figure 31.

LARGE-SIGNAL SETTLING TIME (10V Positive Step)

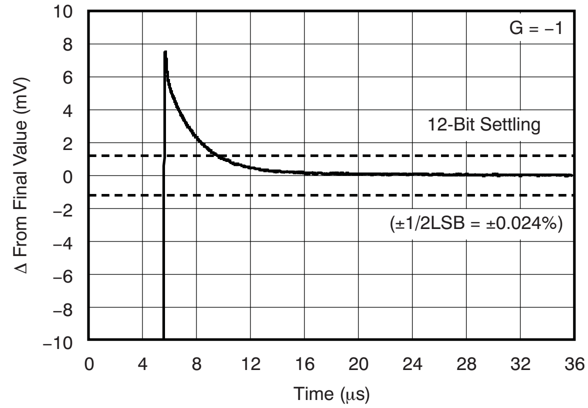

Figure 32.

LARGE-SIGNAL SETTLING TIME (10V Negative Step)

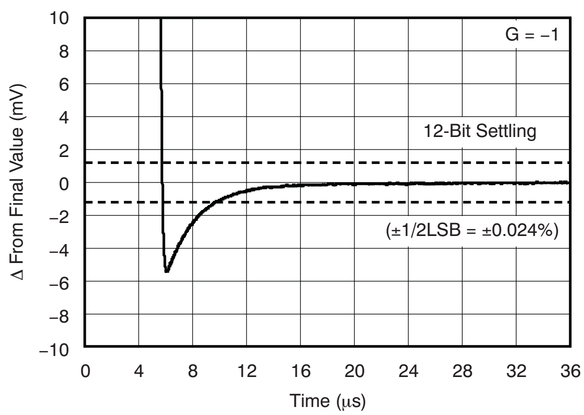

Figure 33.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

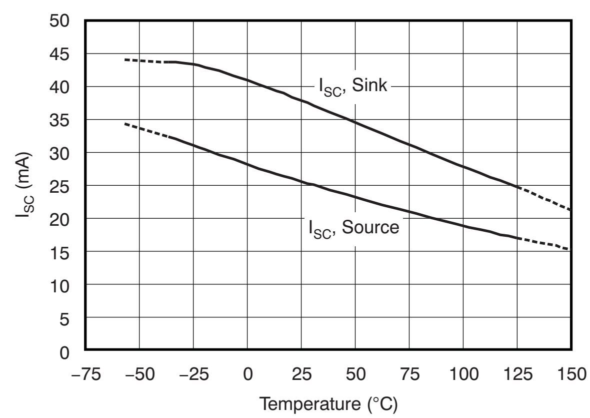

Figure 34.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

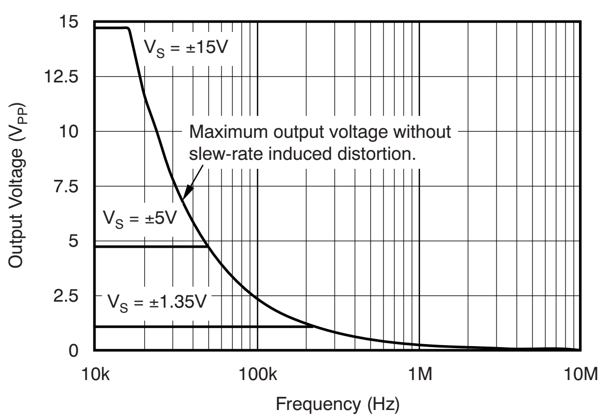

Figure 35.

CHANNEL SEPARATION vs FREQUENCY

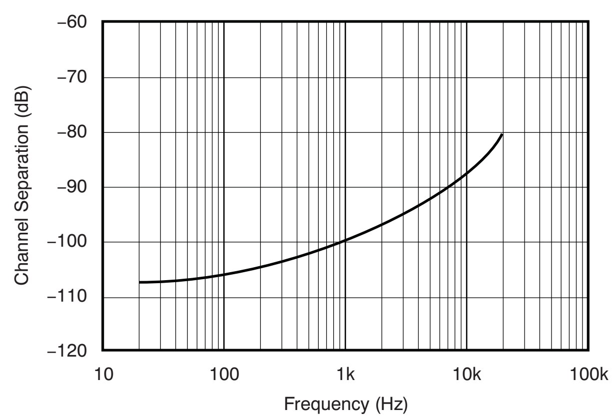

Figure 36.

APPLICATION INFORMATION

The OPAx171 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 2μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1μF capacitors are adequate.

OPERATING CHARACTERISTICS

The OPAx171 family of amplifiers is specified for operation from 2.7V to 36V (±1.35V to ±18V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1μF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPAx171 series extends 100mV below the negative rail and within 2V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100mV beyond the top rail, but with reduced performance within 2V of the top rail. The typical performance in this range is summarized in Table 2.

PHASE-REVERSAL PROTECTION

The OPAx171 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 37.

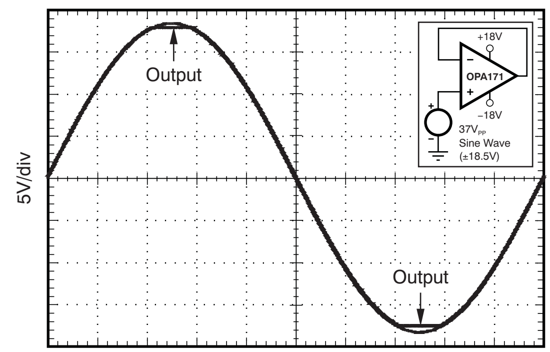

Figure 37. No Phase Reversal

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	**(V+) – 2**		**(V+) + 0.1**	**V**
Offset voltage		7		mV
vs Temperature		**12**		**μV/°C**
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/μs
Noise at f = 1kHz		30		nV/√Hz

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx171 have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50Ω) in series with the output. Figure 38 and Figure 39 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to Applications Bulletin AB-028 (*SBOA015*), available for download from the TI website for details of analysis techniques and application circuits.

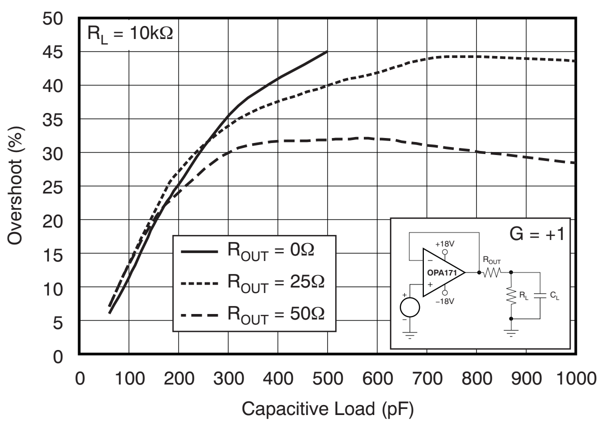

Figure 38. Small-Signal Overshoot versus Capacitive Load (100mV Output Step)

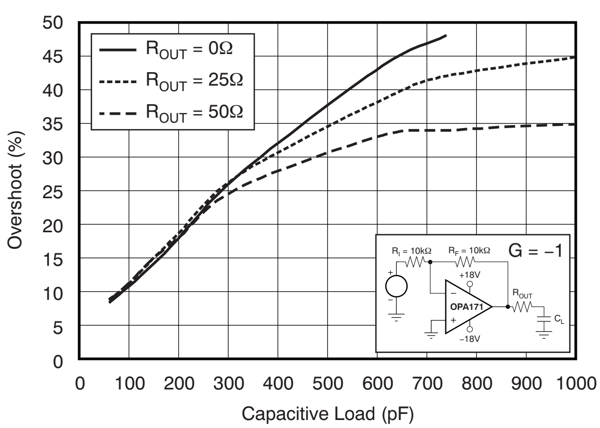

Figure 39. Small-Signal Overshoot versus Capacitive Load (100mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the Absolute Maximum Ratings. Figure 40 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

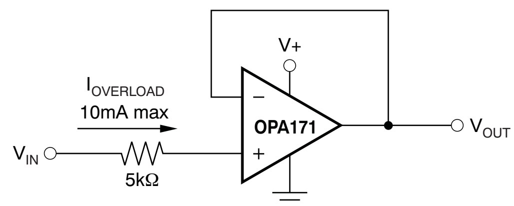

Figure 40. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.