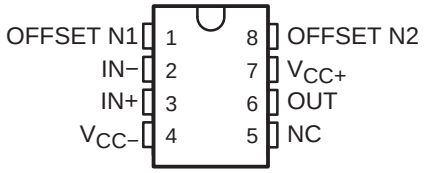
- **Low Noise**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Input-Voltage Range . . . 0 to ±14 V Typ**
- **Wide Supply-Voltage Range . . . ±3 V to ±18 V**

D OR P PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

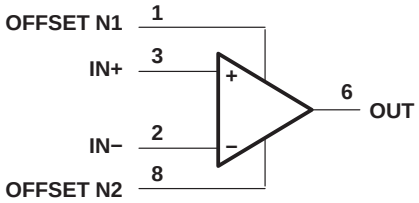
These devices are characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	OP07CP	OP07CP
		Tube of 50	OP07DP	OP07DP
	SOIC (D)	Tube of 75	OP07CD	OP07C
		Reel of 2500	OP07CDR	
		Tube of 75	OP07DD	OP07D
		Reel of 2500	OP07DDR	

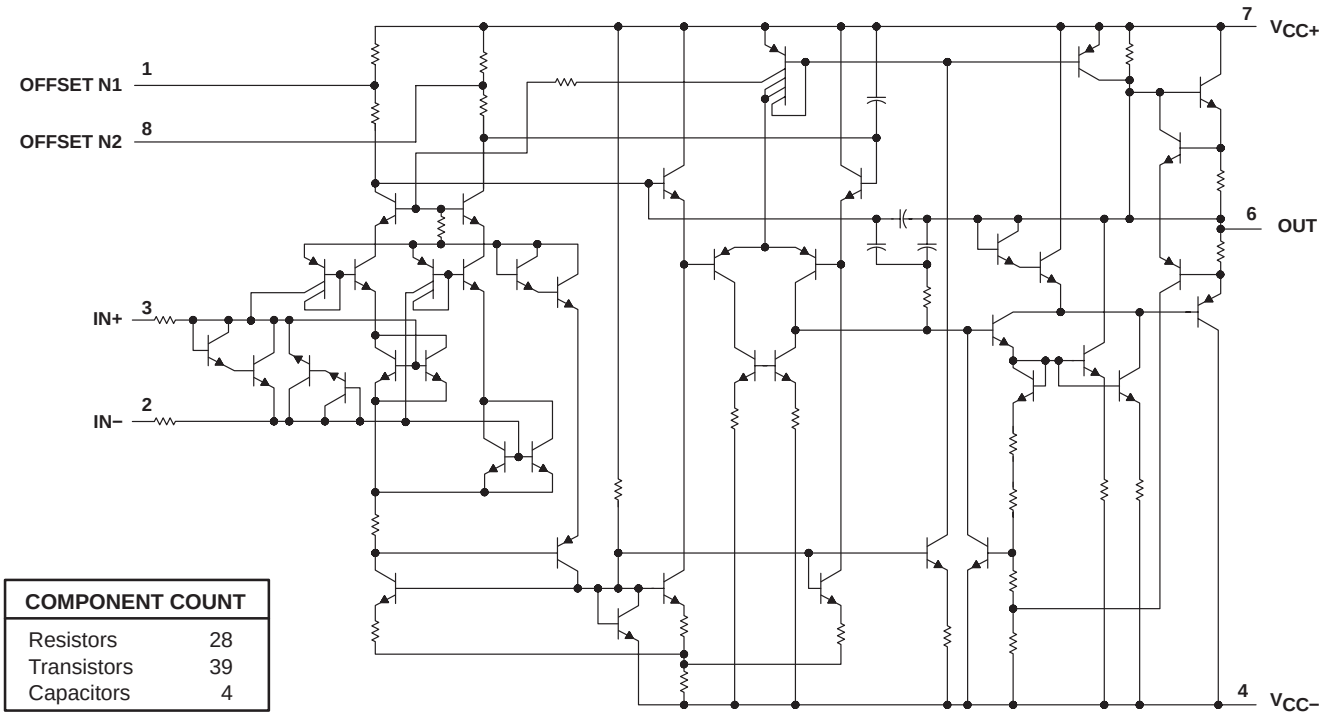
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematic



COMPONENT COUNT	
Resistors	28
Transistors	39
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . . 22 V
V_{CC-} (see Note 1) . . . . . −22 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage, V_I (either input, see Note 3) . . . . . ±22 V
Duration of output short circuit (see Note 4) . . . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 97°C/W
P package . . . . . 85°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	OP07C			OP07D			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	R_S = 50 Ω	25°C		60	150		60	150	µV
				0°C to 70°C		85	250		85	250	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0,	R_S = 50 Ω	0°C to 70°C		0.5	1.8		0.7	2.5	µV/°C
	Long-term drift of input offset voltage	See Note 6				0.4			0.5		µV/mo
	Offset adjustment range	R_S = 20 kΩ,	See Figure 1	25°C		±4			±4		mV
I_{IO}	Input offset current			25°C		0.8	6		0.8	6	nA
				0°C to 70°C		1.6	8		1.6	8	
α_{IIO}	Temperature coefficient of input offset current			0°C to 70°C		12	50		12	50	pA/°C
I_{IB}	Input bias current			25°C		±1.8	±7		±2	±12	nA
				0°C to 70°C		±2.2	±9		±3	±14	
α_{IIB}	Temperature coefficient of input bias current			0°C to 70°C		18	50		18	50	pA/°C
V_{ICR}	Common-mode input voltge range			25°C	±13	±14		±13	±14		V
				0°C to 70°C	±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	R_L ≥ 10 kΩ		25°C	±12	±13		±12	±13		V
		R_L ≥ 2 kΩ			±11.5	±12.8		±11.5	±12.8		
		R_L ≥ 1 kΩ				±12			±12		
		R_L ≥ 2 kΩ		0°C to 70°C	±11	±12.6		±11	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±3 V, R_L ≥ 500 kΩ	V_O = ±0.5 V,	25°C	100	400			400		V/mV
		V_O = ±10 V,	R_L = 2 kΩ	25°C	120	400		120	400		
				0°C to 70°C	100	400		100	400		
B_1	Unity-gain bandwidth			25°C	0.4	0.6		0.4	0.6		MHz
r_i	Input resistance			25°C	8	33		7	31		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V,	R_S = 50 Ω	25°C	100	120		94	110		dB
				0°C to 70°C	97	120		94	106		
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±3 V to ±18 V, R_S = 50 Ω		25°C		7	32		7	32	µV/V
				0°C to 70°C		10	51		10	51	
P_D	Power dissipation	V_O = 0,	No load	25°C		80	150		80	150	mW
		$V_{CC\pm}$ = ±3 V,	V_O = 0, No load			4	8		4	8	

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

NOTE 7: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OP-07DPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
OP-07DPSRE4	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
OP07CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07CDE4	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
OP07CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07CDRE4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
OP07CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
OP07DD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07DDE4	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07DDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07DDRE4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
OP07DP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.