LM3940 1A Low Dropout Regulator for 5V to 3.3V Conversion

Check for Samples: LM3940

FEATURES

- **Output voltage specified over temperature**
- **Excellent load regulation**
- **Guaranteed 1A output current**
- **Requires only one external component**
- **Built-in protection against excess temperature**
- **Short circuit protected**

APPLICATIONS

- **Laptop/Desktop Computers**
- **Logic Systems**

DESCRIPTION

The LM3940 is a 1A low dropout regulator designed to provide 3.3V from a 5V supply.

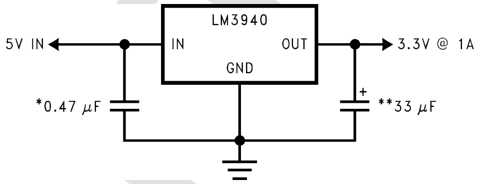
The LM3940 is ideally suited for systems which contain both 5V and 3.3V logic, with prime power provided from a 5V bus.

Because the LM3940 is a true low dropout regulator, it can hold its 3.3V output in regulation with input voltages as low as 4.5V.

The T0-220 package of the LM3940 means that in most applications the full 1A of load current can be delivered without using an additional heatsink.

The surface mount TO-263 package uses minimum board space, and gives excellent power dissipation capability when soldered to a copper plane on the PC board.

TYPICAL APPLICATION



*Required if regulator is located more than 1″ from the power supply filter capacitor or if battery power is used.
**See APPLICATION HINTS.

CONNECTION DIAGRAM

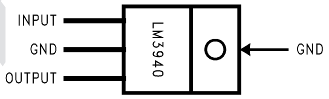


**Figure 1. 3-Lead TO-220 Package(Front View)
NSC Drawing Number TO3B**

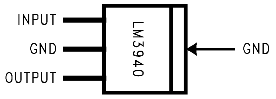


**Figure 2. 3-Lead TO-263 Package
(Front View)
NSC Drawing Number TS3B**

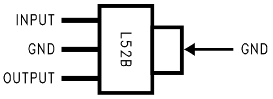


Figure 3. 3-Lead SOT-223
(Front View)
Package Marked L52B
NSC Drawing Number MP04A

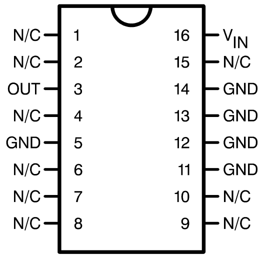


Figure 4. 16-Lead Ceramic Dual-in-Line Package
(Top View)
5962-9688401QEA
NSC Drawing Number J16A

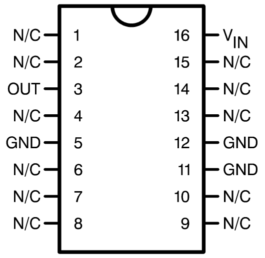
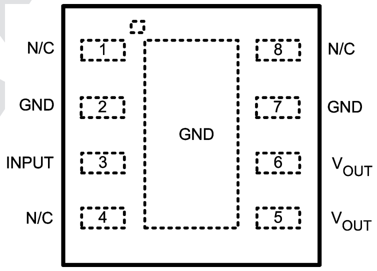


Figure 5. 16-Lead Ceramic Surface-Mount Package
(Top View)
5962-9688401QXA
NSC Drawing Number WG16A

8-Lead LLP



A. Pin 2 and pin 7 are fused to center DAP.

B. Pin 5 and 6 need to be tied together on PCB board.

Figure 6. (Top View)[(A)(B)]
NSC Drawing Number LDC08A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 seconds)	260°C
Power Dissipation (2)	Internally Limited
Input Supply Voltage	7.5V
ESD Rating (3)	2 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of θ_{JA} (for devices in still air with no heatsink) is 60°C/W for the TO-220 package, 80°C/W for the TO-263 package, and 174°C/W for the SOT-223 package. The effective value of θ_{JA} can be reduced by using a heatsink (see APPLICATION HINTS for specific information on heatsinking). The value of θ_{JA} for the LLP package is specifically dependant on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187. The θ_{JA} rating for the LLP is with a JESD51-7 test board having 6 thermal vias under the exposed pad.

(3) ESD rating is based on the human body model: 100 pF discharged through 1.5 kΩ.

Operating Ratings (1)

Junction Temperature Range, T_J	−40°C to +125°C
Input Supply Voltage, $V_{IN(MIN)}$	$V_O + V_{DO}$

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5V, I_L = 1A, C_{OUT} = 33 µF.

Symbol	Parameter	Conditions	Typical	LM3940 (1)		Units
				min	max	
V_O	Output Voltage	5 mA ≤ I_L ≤ 1A	3.3	3.20 **3.13**	3.40 **3.47**	V
$\frac{\Delta V_O}{\Delta V_I}$ (1)	Line Regulation	I_L = 5 mA 4.5V ≤ V_{IN} ≤ 5.5V	20		40	mV
$\frac{\Delta V_O}{I_L}$ (2)	Load Regulation	50 mA ≤ I_L ≤ 1A	35		50 **80**	
Z_O	Output Impedance	I_L (DC) = 100 mA I_L (AC) = 20 mA (rms) f = 120 Hz	35			mΩ
I_Q	Quiescent Current	4.5V ≤ V_{IN} ≤ 5.5V I_L = 5 mA	10		15 **20**	mA
		V_{IN} = 5V I_L = 1A	110		200 **250**	
e_n	Output Noise Voltage	BW = 10 Hz–100 kHz I_L = 5 mA	150			µV (rms)
V_{DO}	Dropout Voltage (2)	I_L = 1A	0.5		0.8 **1.0**	V
		I_L = 100 mA	110		150 **200**	mV
I_L(SC)	Short Circuit Current	R_L = 0	1.7	1.2		A

(1) All limits guaranteed for T_J = 25°C are 100% tested and are used to calculate Outgoing Quality Levels. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

(2) Dropout voltage is defined as the input-output differential voltage where the regulator output drops to a value that is 100 mV below the value that is measured at V_{IN} = 5V.

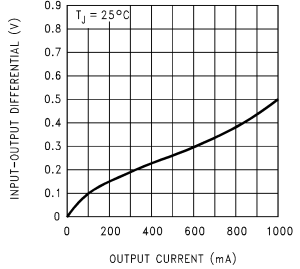
THERMAL PERFORMANCE

Thermal Resistance, Junction-to-Case, θ_{JC}	3-Lead TO-220	4	°C/W
	3-Lead TO-263	4	°C/W
	8-Lead LLP	6	°C/W
Thermal Resistance, Junction-to-Ambient, θ_{JA}	3-Lead TO-220	60	°C/W
	3-Lead TO-263	80	°C/W
	8-Lead LLP (1)	35	°C/W

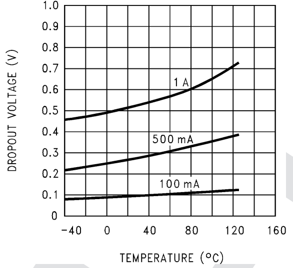
(1) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. The value of θ_{JA} (for devices in still air with no heatsink) is 60°C/W for the TO-220 package, 80°C/W for the TO-263 package, and 174°C/W for the SOT-223 package. The effective value of θ_{JA} can be reduced by using a heatsink (see APPLICATION HINTS for specific information on heatsinking). The value of θ_{JA} for the LLP package is specifically dependant on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187. The θ_{JA} rating for the LLP is with a JESD51-7 test board having 6 thermal vias under the exposed pad.

TYPICAL PERFORMANCE CHARACTERISTICS

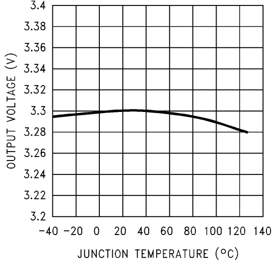
Dropout Voltage



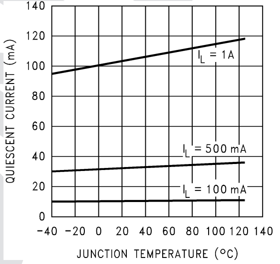
Dropout Voltage vs. Temperature



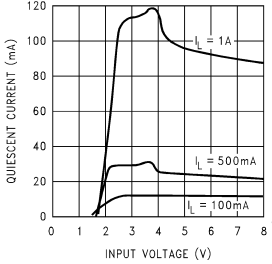
Output Voltage vs. Temperature



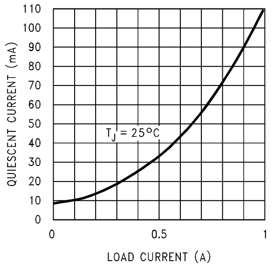
Quiescent Current vs. Temperature



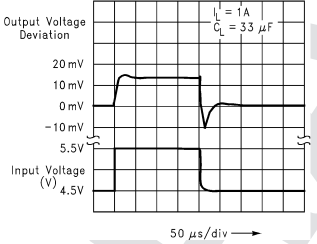
Quiescent Current vs. V_{IN}



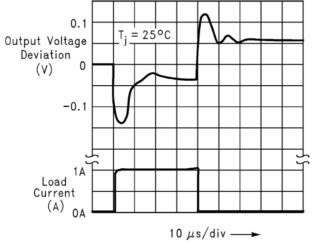
Quiescent Current vs. Load



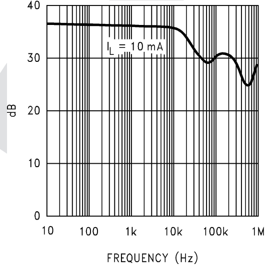
Line Transient Response



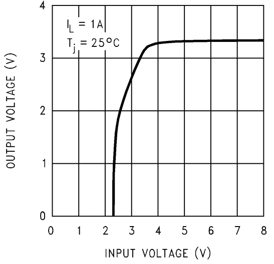
Load Transient Response



Ripple Rejection

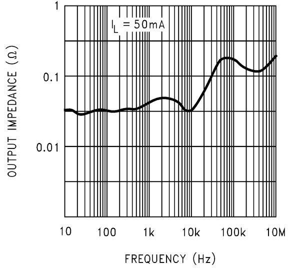


Low Voltage Behavior

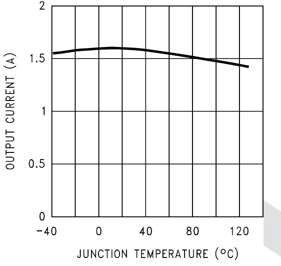


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Impedance



Peak Output Current



APPLICATION HINTS

EXTERNAL CAPACITORS

The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR (Equivalent Series Resistance) and minimum amount of capacitance.

MINIMUM CAPACITANCE:

The minimum output capacitance required to maintain stability is 33 μF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

ESR LIMITS:

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in Figure 7. ***It is essential that the output capacitor meet these requirements, or oscillations can result.***

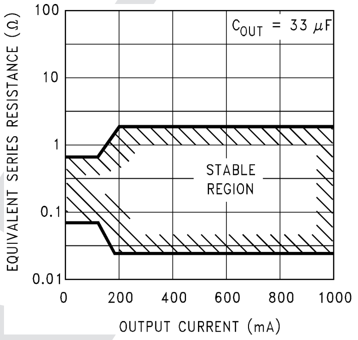


Figure 7. ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to −40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid Tantalum, with the total capacitance split about 75/25% with the Aluminum being the larger value.

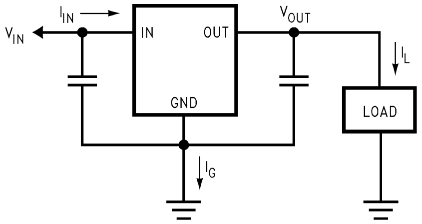
If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The “flatter” ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

Figure 8 shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



$I_{IN} = I_L + I_G$
$P_D = (V_{IN} - V_{OUT})\ I_L + (V_{IN})\ I_G$

Figure 8. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R (max). This is calculated by using the formula:

$T_R\ (max) = T_J\ (max) - T_A\ (max)$

Where: T_J (max) is the maximum allowable junction temperature, which is 125°C for commercial grade parts.

T_A (max) is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for T_R(max) and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $\theta_{(JA)}$, can now be found:

$\theta_{(JA)} = T_R\ (max)/P_D$

IMPORTANT: If the maximum allowable value for $\theta_{(JA)}$ is found to be ≥ 60°C/W for the TO-220 package, ≥ 80°C/W for the TO-263 package, or ≥174°C/W for the SOT-223 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

If the calculated value for $\theta_{(JA)}$falls below these limits, a heatsink is required.

HEATSINKING TO-220 PACKAGE PARTS

The TO-220 can be attached to a typical heatsink, or secured to a copper plane on a PC board. If a copper plane is to be used, the values of $\theta_{(JA)}$ will be the same as shown in the HEATSINKING TO-263 section for the TO-263.

If a manufactured heatsink is to be selected, the value of heatsink-to-ambient thermal resistance, $\theta_{(H-A)}$, must first be calculated:

$\theta_{(H-A)} = \theta_{(JA)} - \theta_{(C-H)} - \theta_{(J-C)}$

Where: $\theta_{(J-C)}$ is defined as the thermal resistance from the junction to the surface of the case. A value of 4°C/W can be assumed for $\theta_{(J-C)}$ for this calculation.

$\theta_{(C-H)}$ is defined as the thermal resistance between the case and the surface of the heatsink. The value of $\theta_{(C-H)}$ will vary from about 1.5°C/W to about 2.5°C/W (depending on method of attachment, insulator, etc.). If the exact value is unknown, 2°C/W should be assumed for $\theta_{(C-H)}$.

When a value for $\theta_{(H-A)}$ is found using the equation shown above, *a heatsink must be selected that has a value that is less than or equal to this number.*

$\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs. power dissipation for the heatsink.

HEATSINKING TO-263 AND SOT-223 PACKAGE PARTS

Both the TO-263 (“S”) and SOT-223 (“MP”) packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 9 shows for the TO-263 the measured values of $\theta_{(JA)}$ for different copper area sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking.*

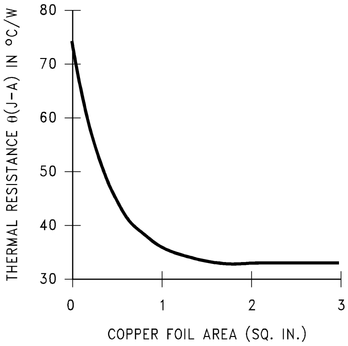


Figure 9. $\theta_{(JA)}$ vs. Copper (1 ounce) Area for the TO-263 Package

As shown in Figure 9, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(JA)}$ for the TO-263 package mounted to a PCB is 32°C/W.

As a design aid, *Figure 10* shows the maximum allowable power dissipation compared to ambient temperature for the TO-263 device (assuming $\theta_{(JA)}$ is 35°C/W and the maximum junction temperature is 125°C).

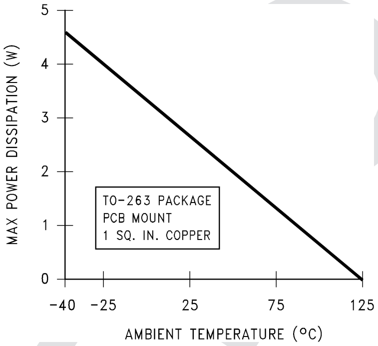


Figure 10. Maximum Power Dissipation vs. T_{AMB} for the TO-263 Package

Figure 11 and Figure 12 show the information for the SOT-223 package. Figure 12 assumes a $\theta_{(JA)}$ of 74°C/W for 1 ounce copper and 51°C/W for 2 ounce copper and a maximum junction temperature of 125°C.

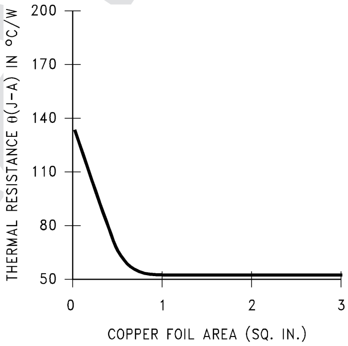


Figure 11. $\theta_{(JA)}$ vs. Copper (2 ounce) Area for the SOT-223 Package

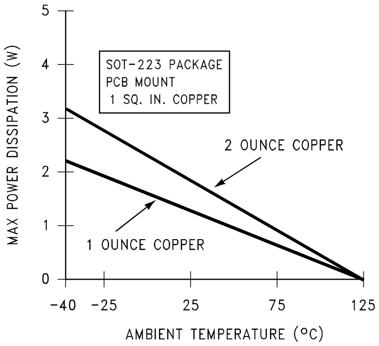


Figure 12. Maximum Power Dissipation vs. T_{AMB} for the SOT-223 Package

Please see AN1028 for power enhancement techniques to be used with the SOT-223 package.

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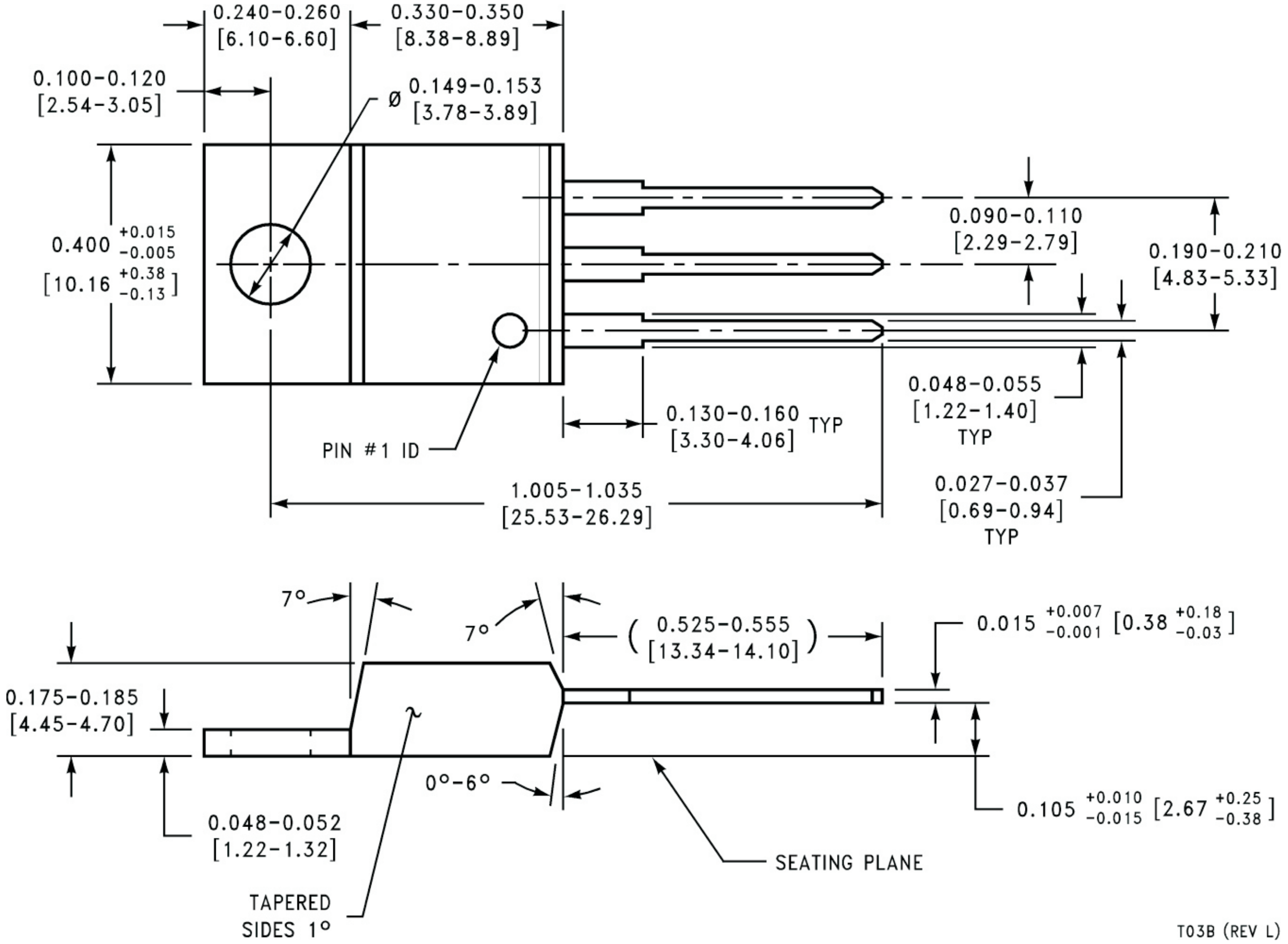
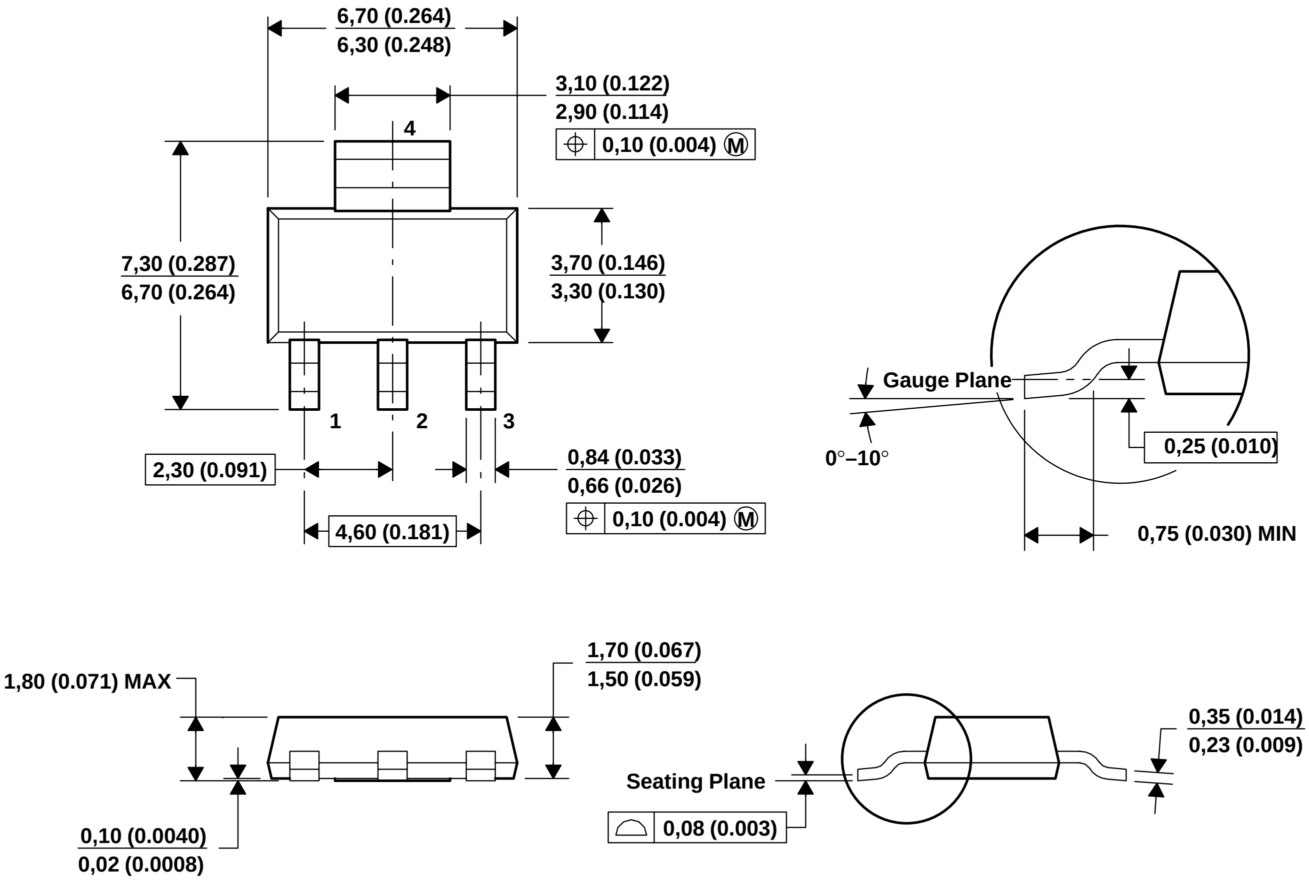

0.240–0.260
[6.10–6.60]
0.330–0.350
[8.38–8.89]
0.100–0.120
[2.54–3.05]
Ø 0.149–0.153
[3.78–3.89]
0.400 +0.015 −0.005
[10.16 +0.38 −0.13]
0.090–0.110
[2.29–2.79]
0.190–0.210
[4.83–5.33]
0.048–0.055
[1.22–1.40]
TYP
0.130–0.160 TYP
[3.30–4.06]
PIN #1 ID
1.005–1.035
[25.53–26.29]
0.027–0.037
[0.69–0.94]
TYP
7°
7°
(0.525–0.555)
[13.34–14.10]
0.015 +0.007 −0.001 [0.38 +0.18 −0.03]
0.175–0.185
[4.45–4.70]
0°–6°
0.105 +0.010 −0.015 [2.67 +0.25 −0.38]
0.048–0.052
[1.22–1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

DCY (R-PDSO-G4) PLASTIC SMALL-OUTLINE



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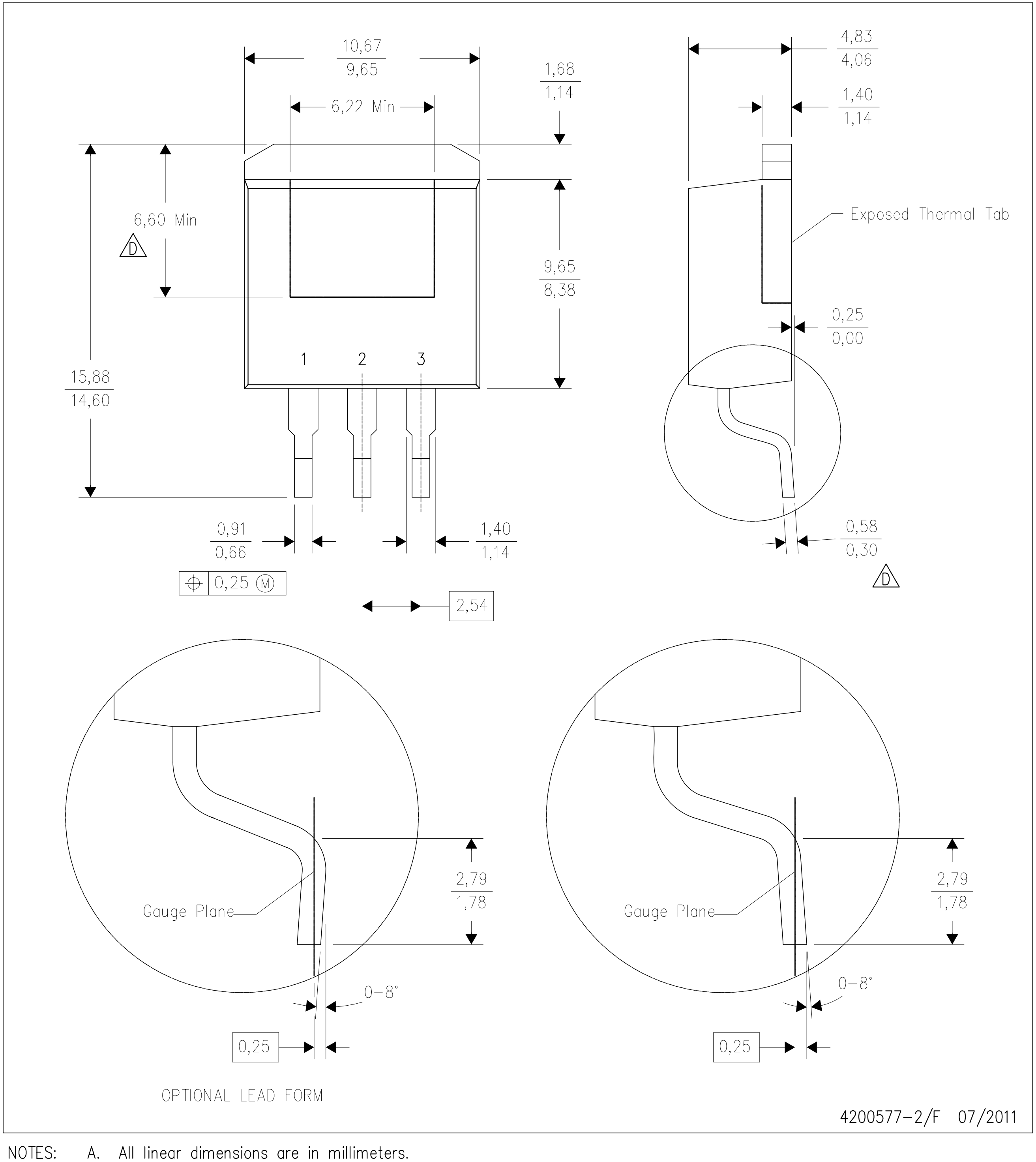
NOTES:
- A. All linear dimensions are in millimeters (inches).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC TO-261 Variation AA.

KTT (R-PSFM-G3) PLASTIC FLANGE-MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

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