

LM98725

*LM98725 3 Channel, 16-Bit, 81 MSPS Analog Front End with LVDS/CMOS Output,
Integrated CCD/CIS Sensor Timing Generator and Spread Spectrum Clock
Generation*



Literature Number: SNAS474D

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3 Channel, 16-Bit, 81 MSPS Analog Front End with LVDS/CMOS Output, Integrated CCD/CIS Sensor Timing Generator and Spread Spectrum Clock Generation

General Description

The LM98725 is a fully integrated, high performance 16-Bit, 81 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative architecture utilizing Correlated Double Sampling (CDS), typically employed with CCD arrays, or Sample and Hold (S/H) inputs (for higher speed CCD or CMOS image sensors). The signal paths utilize 8 bit Programmable Gain Amplifiers (PGA), a +/-9-Bit offset correction DAC and independently controlled Digital Black Level correction loops for each input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for each of the three analog inputs. The signals are then routed to a 81MHz high performance analog-to-digital converter (ADC). The fully differential processing channel shows exceptional noise immunity, having a very low noise floor of -74dB. The 16-bit ADC has excellent dynamic performance making the LM98725 transparent in the image reproduction chain.

A very flexible integrated Spread Spectrum Clock Generation (SSCG) modulator is included to assist with EM compliance and reduce system costs.

Applications

- Multi-Function Peripherals
- High-speed Currency/Check Scanners
- Flatbed or Handheld Color Scanners
- High-speed Document Scanners

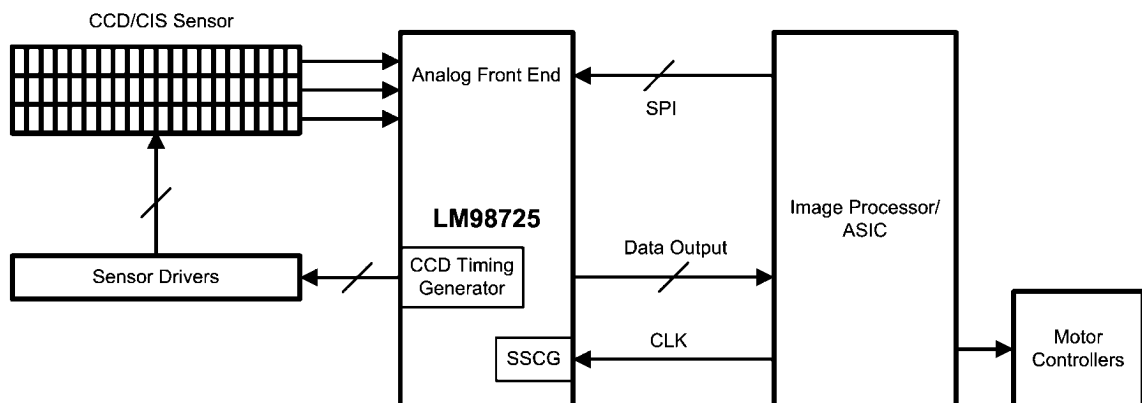
Features

- LVDS/CMOS Outputs
- LVDS/CMOS/Crystal Clock Source with PLL Multiplication
- Integrated Flexible Spread Spectrum Clock Generation
- CDS or S/H Processing for CCD or CIS sensors
- Independent Gain/Offset Correction for Each Channel
- Automatic per-Channel Gain and Offset Calibration
- Programmable Input Clamp Voltage
- Flexible CCD/CIS Sensor Timing Generator

Key Specifications

- | | |
|--------------------------|------------------------------------|
| ■ Maximum Input Level | 1.2 or 2.4 Volt Modes |
| ■ | (both with + or - polarity option) |
| ■ ADC Resolution | 16-Bit |
| ■ ADC Sampling Rate | 81 MSPS |
| ■ INL | +17/- 28 LSB (typ) |
| ■ Channel Sampling Rate | 30/30/27 MSPS |
| ■ PGA Gain Steps | 256 Steps |
| ■ PGA Gain Range | 0.62 to 8.3x |
| ■ Analog DAC Resolution | +/-9 Bits |
| ■ Analog DAC Range | +/-307mV or +/-614mV |
| ■ Digital DAC Resolution | +/-6 Bits |
| ■ Digital DAC Range | -2048 LSB to + 2016 LSB |
| ■ SNR | -74dB (@0dB PGA Gain) |
| ■ Power Dissipation | 755mW (LVDS) |
| ■ Operating Temp | 0 to 70°C |
| ■ Supply Voltage | 3.3V Nominal (3.0V to 3.6V range) |

System Block Diagram



LM98725 Overall Chip Block Diagram

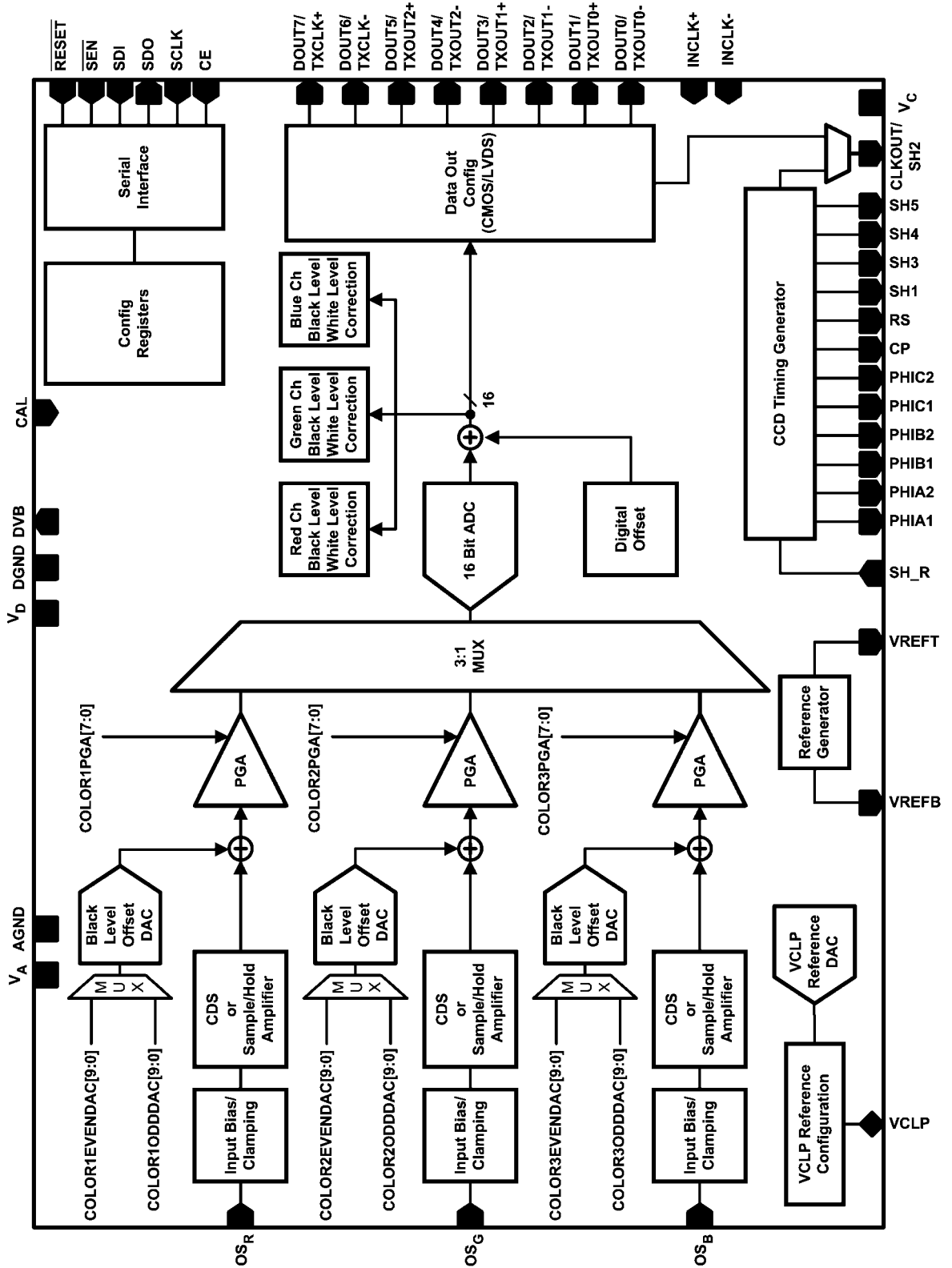
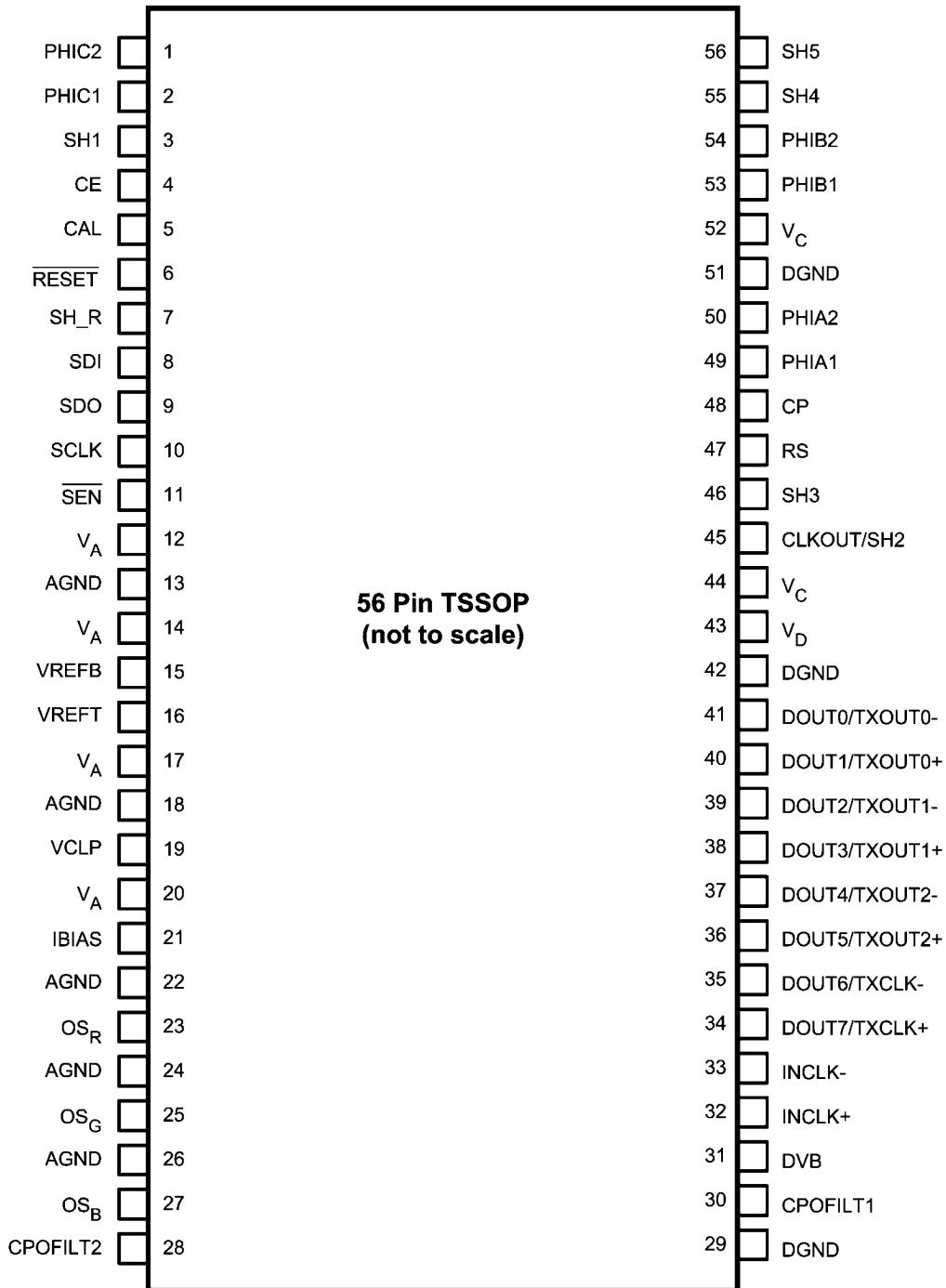


FIGURE 1. Chip Block Diagram

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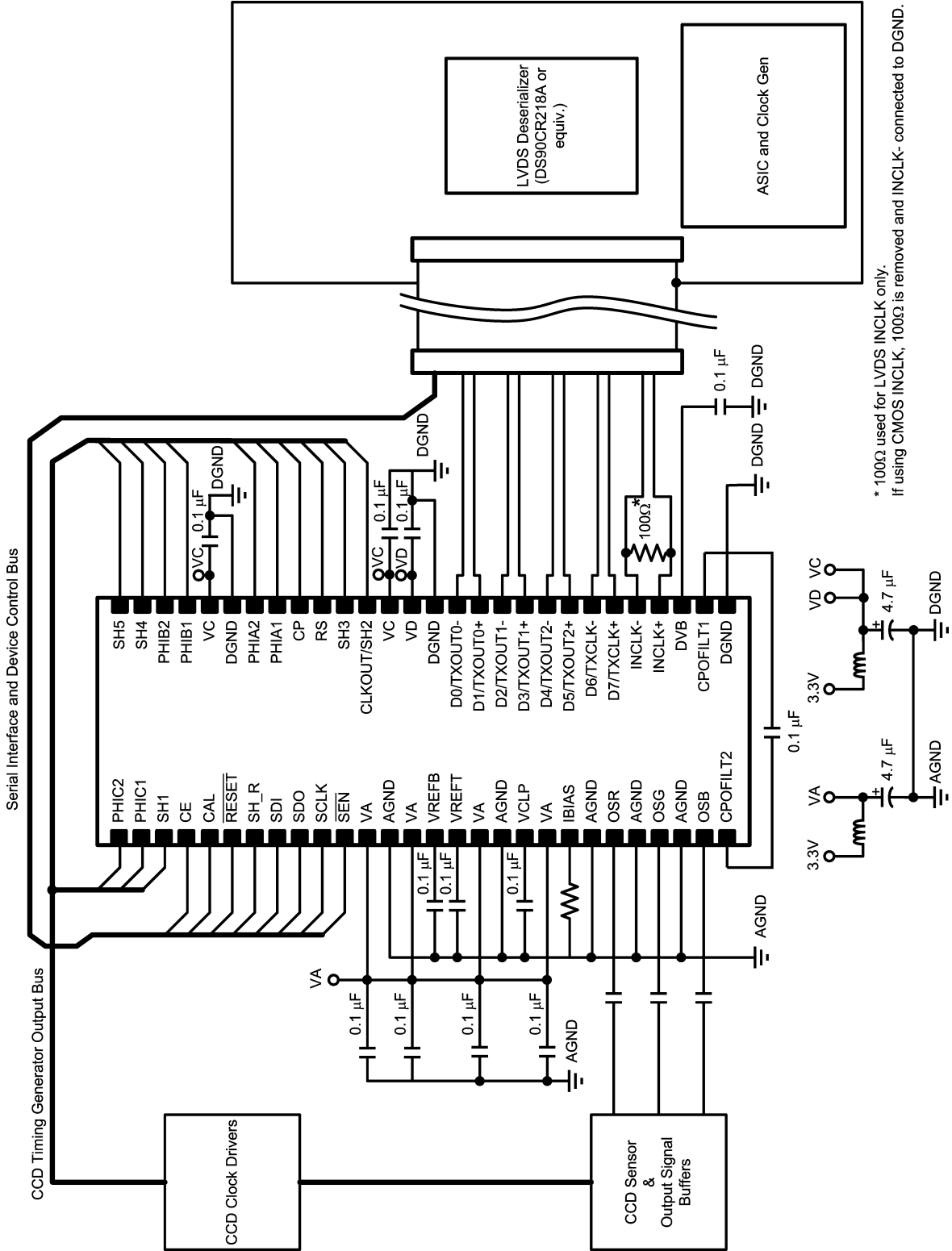
LM98725 Pin Out Diagram



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FIGURE 2. LM98725 Pin Out Diagram

Typical Application Diagram



* 100Ω used for LVDS INCLK only.
If using CMOS INCLK, 100Ω is removed and INCLK- connected to DGND.

FIGURE 3. Typical Application Diagram

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Pin Descriptions

Pin	Name	I/O	Typ	Res	Description	
1	PHIC2	O	D	PU	Configurable high speed sensor timing output.	
2	PHIC1	O	D	PD	Configurable high speed sensor timing output.	
3	SH1	O	D	PU	Configurable low speed sensor timing output.	
4	CE	I	D		Chip Serial Interface Address Setting Input	
					CE Level	Address
					V _D	01
					Float	10
	DGND	00				
5	CAL	I	D	PD	Initiate calibration sequence. Leave unconnected or tie to DGND if unused.	
6	RESET	I	D	PU	Active-low master reset. NC when function not being used.	
7	SH_R	I	D	PD	External request for an SH interval.	
8	SDI	I	D	PD	Serial Interface Data Input.	
9	SDO	O	D		Serial Interface Data Output.	
10	SCLK	I	D	PD	Serial Interface shift register clock.	
11	SEN	I	D	PU	Active-low chip enable for the Serial Interface.	
12	V _A		P		Analog power supply. Bypass voltage source with 4.7μF and pin with 0.1μF to AGND.	
13	AGND		P		Analog ground return.	
14	V _A		P		Analog power supply. Bypass voltage source with 4.7μF and pin with 0.1μF to AGND.	
15	VREFB	O	A		Bottom of ADC reference. Bypass with a 0.1μF capacitor to ground.	
16	VREFT	O	A		Top of ADC reference. Bypass with a 0.1μF capacitor to ground.	
17	V _A		P		Analog power supply. Bypass voltage source with 4.7μF and pin with 0.1μF to AGND.	
18	AGND		P		Analog ground return.	
19	VCLP	IO	A		Input Clamp Voltage. Normally bypassed with a 0.1μF, and a 4.7μF capacitor to AGND. An external reference voltage may be applied to this pin.	
20	V _A		P		Analog power supply. Bypass voltage source with 4.7μF and pin with 0.1μF to AGND.	
21	IBIAS	O	A		Bias setting pin. Connect a 9.0 kOhm 1% resistor to AGND.	
22	AGND		P		Analog ground return.	
23	OS _R	I	A		Analog input signal. Typically sensor Red output AC-coupled thru a capacitor.	
24	AGND		P		Analog ground return.	
25	OS _G	I	A		Analog input signal. Typically sensor Green output AC-coupled thru a capacitor.	
26	AGND		P		Analog ground return.	
27	OS _B	I	A		Analog input signal. Typically sensor Blue output AC-coupled thru a capacitor.	
28	CPOFIL2		A		Charge Pump Filter Capacitor. Bypass this supply pin with a 0.1μF capacitor to CPOFIL1.	
29	DGND		P		Digital ground return.	
30	CPOFIL1		A		Charge Pump Filter Capacitor. Bypass this supply pin with a 0.1μF capacitor to CPOFIL2.	
31	DVB	O	D		Digital Core Voltage bypass. Not an input. Bypass with 0.1μF capacitor to DGND.	
32	INCLK+	I	D		Clock Input. Non-Inverting input for LVDS clocks or CMOS clock input. CMOS clock is selected when pin 29 is held at DGND, otherwise clock is configured for LVDS operation.	
33	INCLK-	I	D		Clock Input. Inverting input for LVDS clocks, connect to DGND for CMOS clock.	
34	DOUT7/ TXCLK+	O	D		Bit 7 of the digital video output bus in CMOS Mode, LVDS Frame Clock+ in LVDS Mode.	
35	DOUT6/ TXCLK-	O	D		Bit 6 of the digital video output bus in CMOS Mode, LVDS Frame Clock- in LVDS Mode.	
36	DOUT5/ TXOUT2+	O	D		Bit 5 of the digital video output bus in CMOS Mode, LVDS Data Out2+ in LVDS Mode.	

Pin	Name	I/O	Typ	Res	Description
37	DOUT4/ TXOUT2-	O	D		Bit 4 of the digital video output bus in CMOS Mode, LVDS Data Out2- in LVDS Mode.
38	DOUT3/ TXOUT1+	O	D		Bit 3 of the digital video output bus in CMOS Mode, LVDS Data Out1+ in LVDS Mode.
39	DOUT2/ TXOUT1-	O	D		Bit 2 of the digital video output bus in CMOS Mode, LVDS Data Out1- in LVDS Mode.
40	DOUT1/ TXOUT0+	O	D		Bit 1 of the digital video output bus in CMOS Mode, LVDS Data Out0+ in LVDS Mode.
41	DOUT0/ TXOUT0-	O	D		Bit 0 of the digital video output bus in CMOS Mode, LVDS Data Out0- in LVDS Mode.
42	DGND	O	D	PD	Configurable sensor control output.
43	V _D		P		Power supply for the digital circuits. Bypass this supply pin with 0.1µF capacitor. A single 4.7µF capacitor should be used between the supply and the VD, VR and VC pins.
44	V _C		P		Power supply for the sensor control outputs. Bypass this supply pin with 0.1µF capacitor.
45	CLKOUT/SH2	O	D		Output clock for registering output data when using CMOS outputs, or a configurable low speed sensor timing output.
46	SH3	O	D		Configurable low speed sensor timing output.
47	RS	O	D		Configurable high speed sensor timing output.
48	CP	O	D		Configurable high speed sensor timing output.
49	PHIA1	O	D		Configurable high speed sensor timing output.
50	PHIA2	O	D		Configurable high speed sensor timing output.
51	DGND		P		Digital ground return.
52	V _C		P		Power supply for the sensor control outputs. Bypass this supply pin with 0.1µF capacitor.
53	PHIB1	O	D		Configurable high speed sensor timing output.
54	PHIB2	O	D		Configurable high speed sensor timing output.
55	SH4	O	D		Configurable low speed sensor timing output.
56	SH5	O	D		Configurable low speed sensor timing output.

(I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog), (PU=Pull Up with an internal resistor), (PD=Pull Down with an internal resistor.).

Absolute Maximum Ratings *(Note 1, Note 2)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VA,VR,VD,VC)	4.2V
Voltage on Any Input Pin (Not to exceed 4.2V)	-0.3V to (VA + 0.3V)
Voltage on Any Output Pin (except DVB and not to exceed 4.2V)	-0.3V to (VA + 0.3V)
DVB Output Pin Voltage	2.0V
Input Current at any pin other than Supply Pins <i>(Note 3)</i>	±25 mA
Package Input Current (except Supply Pins) <i>(Note 3)</i>	±50 mA
Maximum Junction Temperature (TA)	150°C

Thermal Resistance (θ_{JA})	<66°C/W
Package Dissipation at $T_A = 25^\circ\text{C}$ <i>(Note 4)</i>	>1.89W
ESD Rating <i>(Note 5)</i>	
Human Body Model	2500V
Machine Model	250V
Storage Temperature	-65°C to +150°C
<i>Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 6)</i>	

Operating Ratings *(Note 1, Note 2)*

Operating Temperature Range	0°C ≤ T_A ≤ +70°C
All Supply Voltage	+3.0V to +3.6V

Electrical Characteristics

The following specifications apply for VA = VD = VR = VC = 3.3V, CL = 10pF, and f_{INCLK} = 27MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	Min <i>(Note 9)</i>	Typ <i>(Note 8)</i>	Max <i>(Note 9)</i>	Units
CMOS Digital Input DC Specifications (RESETb, SH_R, SCLK, SENb)						
V _{IH}	Logical "1" Input Voltage		2.0			V
V _{IL}	Logical "0" Input Voltage				0.8	V
V _{IHYST}	Logic Input Hysteresis			0.6		
I _{IH}	Logical "1" Input Current	V _{IH} = VD RESET, SEN SH_R, SCLK, SDI, CAL CE		100 65 30		nA μA nA
I _{IL}	Logical "0" Input Current	V _{IL} = DGND RESET, SEN SH_R, SCLK, SDI, CAL CE		-65 -100 -30		μA nA μA
CMOS Digital Output DC Specifications (SH1 to SH5, RS, CP, PHIA, PHIB, PHIC)						
V _{OH}	Logical "1" Output Voltage	I _{OUT} = -0.5mA	3.0			V
V _{OL}	Logical "0" Output Voltage	I _{OUT} = 1.6mA			0.21	V
I _{OS}	Output Short Circuit Current	V _{OUT} = DGND V _{OUT} = VD		18 -25		mA
I _{OZ}	CMOS Output TRI-STATE Current	V _{OUT} = DGND V _{OUT} = VD		20 -25		nA
CMOS Digital Output DC Specifications (CMOS Data Outputs)						
V _{OH}	Logical "1" Output Voltage	I _{OUT} = -0.5mA		2.3		V
V _{OL}	Logical "0" Output Voltage	I _{OUT} = 1.6mA		0.12		V
I _{OS}	Output Short Circuit Current	V _{OUT} = DGND V _{OUT} = VD		12 -14		mA
I _{OZ}	CMOS Output TRI-STATE Current	V _{OUT} = DGND V _{OUT} = VD		20 -25		nA
LVDS/CMOS Clock Receiver DC Specifications (INCLK+ and INCLK- Pins)						

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
V _{IHL}	Differential LVDS Clock High Threshold Voltage	R _L = 100Ω V _{CM} (LVDS Input Common Mode Voltage) = 1.25V			200	mV
V _{ILL}	Differential LVDS Clock Low Threshold Voltage		-200			mV
V _{IHC}	CMOS Clock High Threshold Voltage	INCLK- = DGND	2.0			V
V _{ILC}	CMOS Clock Low Threshold Voltage				0.8	V
I _{IHL}	CMOS Clock Input High Current			230	260	μA
I _{ILC}	CMOS Clock Input Low Current		-135	-120		μA
LVDS Output DC Specifications						
V _{OD}	Differential Output Voltage	R _L = 100Ω	280	390	490	mV
V _{OS}	LVDS Output Offset Voltage		1.08	1.20	1.33	V
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V, R _L = 100Ω		8.5		mA
Power Supply Specifications						
I _A	VA Analog Supply Current	LVDS Output Data Format		152	180	mA
		LVDS Output Data Format (Powerdown)		3.6	6	mA
		CMOS Output Data Format (40 MHz)		136	168	mA
I _D	VD Digital Output Driver Supply Current	LVDS Output Data Format		76	94	mA
		LVDS Output Data Format (Powerdown)		8.5	17	mA
		CMOS Output Data Format (ATE Loading of CMOS Outputs > 50 pF) (40 MHz)		46	68	mA
I _C	VC CCD Timing Generator Output Driver Supply Current	Typical sensor outputs: SH1-SH5, PHIA, PHIB, PHIC, RS, CP (ATE Loading of CMOS Outputs > 50pF)		1	4	mA
PWR	Average Power Dissipation	LVDS Output Data Format		755	885	mW
		LVDS Output Data Format (Powerdown)		40	70	mW
		CMOS Output Data Format (ATE Loading of CMOS Outputs > 50pF) (40 MHz)		600	740	mW
Input Sampling Circuit Specifications						
V _{IN}	Input Voltage Level	CDS Gain=1x, PGA Gain=1x CDS Gain=2x, PGA Gain= 1x		2.3 1.22		Vp-p

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
I_{IN_SH}	Sample and Hold Mode Input Leakage Current	Source Followers Off CDS Gain = 1x $OS_x = VA$ ($OS_x = AGND$)	(-200)	32 (-165)	50	μA
		Source Followers Off CDS Gain = 2x $OS_x = VA$ ($OS_x = AGND$)	(-290)	55 (-240)	70	μA
		Source Followers On CDS Gain = 2x $OS_x = VA$ ($OS_x = AGND$)	(-250)	20 (-50)	250	nA
C_{SH}	Sample/Hold Mode Equivalent Input Capacitance	CDS Gain = 1x		2.5		pF
		CDS Gain = 2x		4		pF
I_{IN_CDS}	CDS Mode Input Leakage Current	Source Followers Off $OS_x = VA$ ($OS_x = AGND$)	(-250)	10 (-50)	250	nA
R_{CLPIN}	CLPIN Switch Resistance (OS_x to VCLP Node)			16	55	Ω
VCLP Reference Circuit Specifications						
V_{VCLP}	VCLP Voltage 000	VCLP Voltage Setting = 000		0.85VA		V
	VCLP Voltage 001	VCLP Voltage Setting = 001		0.9VA		V
	VCLP Voltage 010	VCLP Voltage Setting = 010		0.95VA		V
	VCLP Voltage 011	VCLP Voltage Setting = 011		0.6VA		V
	VCLP Voltage 100	VCLP Voltage Setting = 100		0.55VA		V
	VCLP Voltage 101	VCLP Voltage Setting = 101		0.4VA		V
	VCLP Voltage 110	VCLP Voltage Setting = 110		0.35VA		V
	VCLP Voltage 111	VCLP Voltage Setting = 111		0.15VA		V
I_{SC}	VCLP DAC Short Circuit Output Current	0001 xxxxb VCLP Config. Register =		30		mA
Black Level Offset DAC Specifications						
	Resolution			10		Bits
	Monotonicity		Guaranteed by characterization			
	Offset Adjustment Range Referred to AFE Input	CDS Gain = 1x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF		-614 614		mV
		CDS Gain = 2x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF		-307 307		mV
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF	-17500 +16130		-16130 +17500	LSB
	DAC LSB Step Size	CDS Gain = 1x Referred to AFE Output		1.2 (32)		mV (LSB)
DNL	Differential Non-Linearity		-0.84	+0.74/ -0.37	+2.4	LSB
INL	Integral Non-Linearity		-2.5	+0.72/ -0.56	+2.5	LSB
PGA Specifications						
	Gain Resolution			8		Bits
	Monotonicity		Guaranteed by characterization			
	Maximum Gain	CDS Gain = 1x	7.7	8.3	8.8	V/V
		CDS Gain = 1x	17.7	18.4	18.9	dB

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
	Minimum Gain	CDS Gain = 1x	0.58	0.62	0.67	V/V
		CDS Gain = 1x	-4.7	-4.2	-3.5	dB
	PGA Function	Gain (V/V) = (180/(277-PGA Code)) Gain (dB) = 20LOG10(180/(277-PGA Code))				
	Channel Matching	Minimum PGA Gain		3		%
		Maximum PGA Gain		12.7		
ADC Specifications						
V _{REFT}	Top of Reference			2.07		V
V _{REFB}	Bottom of Reference			0.89		V
V _{REFT} - V _{REFB}	Differential Reference Voltage		1.06	1.18	1.30	V
	Ovrange Output Code			65535		
	Underrange Output Code			0		
Digital Offset "DAC" Specifications						
	Resolution			7		Bits
	Digital Offset DAC LSB Step Size	Referred to AFE Output		32		LSB
	Offset Adjustment Range Referred to AFE Output	Min DAC Code =7b0000000 Mid DAC Code =7b1000000 Max DAC Code = 7b1111111		-2048 0 +2016		LSB
Full Channel Performance Specifications						
DNL	Differential Non-Linearity	(Note 10)	-0.999	+0.8/-0.7	2.5	LSB
INL	Integral Non-Linearity	(Note 10)	-75	+18/-25	75	LSB
SNR	Total Output Noise	Minimum PGA Gain (Note 10)		-76		dB
				10	26	LSB RMS
		Maximum PGA Gain (Note 10)		-56		dB
	Channel to Channel Crosstalk	Mode 3		26		LSB
		Mode 2		17		

AC Timing Specifications

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX} ; all other limits $T_A = 25^\circ C$.**

Symbol	Parameter	Conditions	Min (<i>Note 9</i>)	Typ (<i>Note 8</i>)	Max (<i>Note 9</i>)	Units
Input Clock Timing Specifications						
f_{INCLK}	Input Clock Frequency	INCLK = PIXCLK (Pixel Rate Clock)	0.66 1 1		27 (Mode 3) 30 (Mode 2) 30 (Mode 1)	MHz
		INCLK = ADCCLK (ADC Rate Clock)	2		81 (Mode 3) 60 (Mode 2) 30 (Mode 1)	MHz
T_{dc}	Input Clock Duty Cycle		40/60	50/50	60/40	%
Full Channel Latency Specifications						
t_{LAT3}	3 Channel Mode Pipeline Delay	PIXPHASE0		24		T_{ADC}
		PIXPHASE1		23 1/2		
		PIXPHASE2		23		
		PIXPHASE3		22 1/2		
t_{LAT2}	2 Channel Mode Pipeline Delay	PIXPHASE0		21		T_{ADC}
		PIXPHASE1		20 1/2		
		PIXPHASE2		20		
		PIXPHASE3		19 1/2		
t_{LAT1}	1 Channel Mode Pipeline Delay	PIXPHASE0		19		T_{ADC}
		PIXPHASE1		18 1/2		
		PIXPHASE2		18		
		PIXPHASE3		17 1/2		
SH_R Timing Specifications						
t_{SHR_S}	SH_R Setup Time			2		ns
t_{SHR_H}	SH_R Hold Time			2		ns
LVDS Output Timing Specifications						
TX_{pp0}	TXCLK to Pulse Position 0	LVDS Output Specifications not tested in production. Min/Max guaranteed by design, characterization and statistical analysis.	-0.26	0	0.26	ns
TX_{pp1}	TXCLK to Pulse Position 1		1.50	1.76	2.02	ns
TX_{pp2}	TXCLK to Pulse Position 2		3.26	3.53	3.79	ns
TX_{pp3}	TXCLK to Pulse Position 3		5.03	5.29	5.55	ns
TX_{pp4}	TXCLK to Pulse Position 4		6.80	7.06	7.32	ns
TX_{pp5}	TXCLK to Pulse Position 5		8.56	8.82	9.08	ns
TX_{pp6}	TXCLK to Pulse Position 6		10.32	10.58	10.84	ns
CMOS Output Timing Specifications						
t_{CRDO}	CLKOUT Rising Edge to CMOS Output Data Transition	$f_{INCLK} = 40MHz$ INCLK = ADCCLK (ADC Rate Clock)	2	4.5	9	ns
Serial Interface Timing Specifications						

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
f_{SCLK}	Input Clock Frequency	$f_{SCLK} \leq f_{INCLK}$ INCLK = PIXCLK (Pixel Rate Clock) Mode 3/2/1			27/30/30	MHz
		$f_{SCLK} \leq f_{INCLK}$ INCLK = ADCCLK (ADC Rate Clock) Mode 3/2/1			81/60/30	MHz
	SCLK Duty Cycle			50/50		ns
t_{IH}	Input Hold Time		1.5			ns
t_{IS}	Input Setup Time		2.5			ns
t_{SENSC}	SCLK Start Time After SEN Low		1.5			ns
t_{SCSEN}	\overline{SEN} High after last SCLK Rising Edge		2.5			ns
t_{SENV}	\overline{SEN} Pulse Width	INCLK present	6			T_{INCLK}
		INCLK stopped (Note 11, Note 12)	50			ns
t_{OD}	Output Delay Time			11	14	ns
t_{HZ}	Data Output to High Z				0.5	T_{SCLK}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.

Note 2: All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.

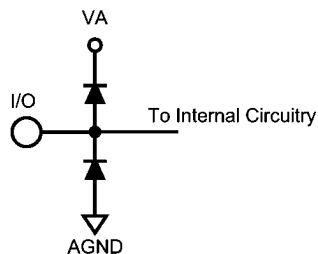
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > V_A$ or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 k Ω resistor. Machine model is 220 pF discharged through 0 Ω .

Note 6: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 7: The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per note 3. However, input errors will be generated if the input goes above V_A and below AGND.



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Note 8: Typical figures are at $T_A = 25^\circ\text{C}$, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 9: Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: This parameter guaranteed by design and characterization.

Note 11: If the input INCLK is divided down to a lower internal clock rate via the PLL, the parameter t_{SENV} will be increased by the same factor.

Note 12: When the Spread Spectrum Clock Generation feature is enabled, t_{SENV} should be increased by 1.

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
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