LM80

LM80 Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor

Literature Number: SNIS102E

National Semiconductor

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Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor

General Description

The LM80 provides 7 positive voltage inputs, temperature measurement, fan speed measurement, and hardware monitoring on an I²C™ interface. The LM80 performs WATCHDOG comparisons of all measured values and an open-drain interrupt output becomes active when any values exceed programmed limits. A Chassis Intrusion input is provided to monitor and reset an external circuit designed to latch a chassis intrusion event.

The LM80 is especially suited to interface to both linear and digital temperature sensors. The 10 mV LSB and 2.56 volt input range is ideal for accepting inputs from a linear sensor such as the LM50. The $\overline{\text{BTI}}$ is used as an input from either digital or thermostat sensors such as LM75 and LM56.

The LM80's 2.8V to 5.75V supply voltage range, low supply current, and I²C interface make it ideal for a wide range of applications. These include hardware monitoring and protection applications in personal computers, electronic test equipment, and office electronics.

Features

- Temperature sensing
- 7 positive voltage inputs
- 2 programmable fan speed monitoring inputs
- 10 mV LSB and 2.56V input range accepts outputs from linear temperature sensors such as the LM50
- Chassis Intrusion Detector input
- WATCHDOG comparison of all monitored values
- Separate input to show status in Interrupt Status Register of additional external temperature sensors such as the LM56 or LM75
- I²C Serial Bus interface compatibility
- Shutdown mode to minimize power consumption
- Programmable $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin: $\overline{\text{RST_OUT}}$ provides a Reset output; $\overline{\text{OS}}$ provides an Interrupt Output activated by an Overtemperature Shutdown event

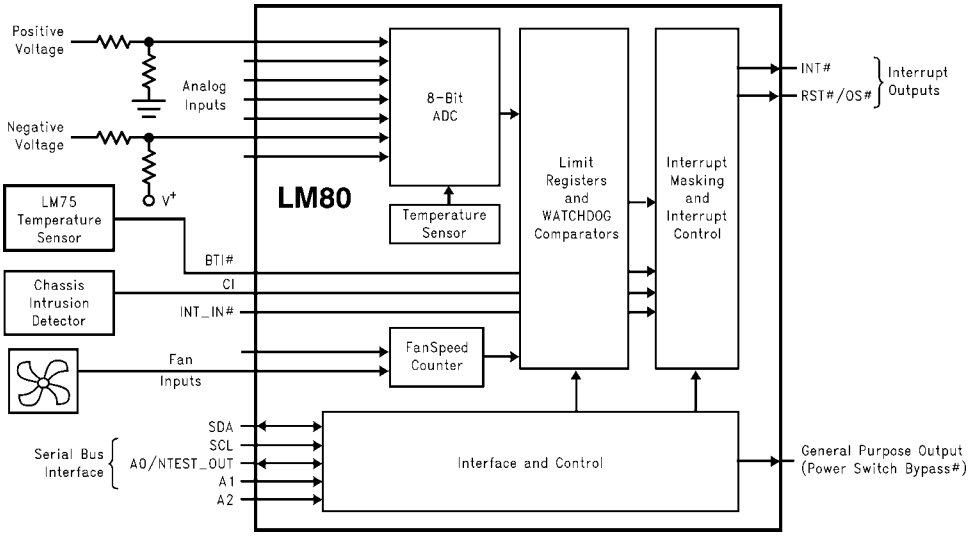
Key Specifications

Voltage monitoring Error	±1% (max)
Temperature Error −25°C to +125°C	± 3°C (max)
Supply Voltage Range	2.8V to 5.75V
Supply Current: Operating	0.2 mA typ
Supply Current: Shutdown	15 µA typ
ADC Resolution	8 Bits
Temperature Resolution	0.5°C

Applications

- System Thermal and Hardware Monitoring for Servers and PCs
- Office Electronics
- Electronic Test Equipment and Instrumentation

Typical Application



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# Indicates Active Low ("Not")

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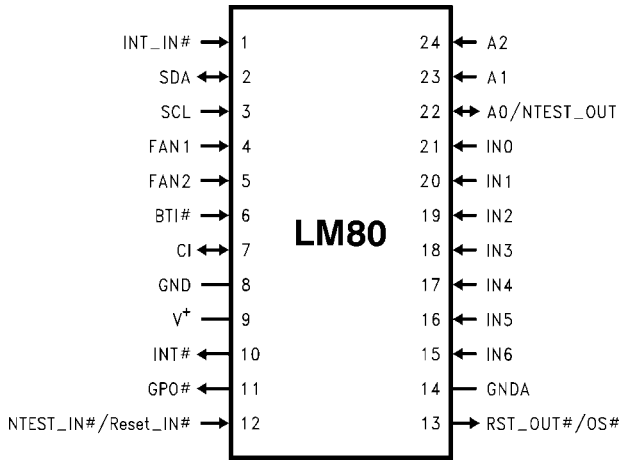
Ordering Information

Temperature Range $-25°C \leq T_A \leq +125°C$		NS Package Number	Specified Power Supply Voltage
Order Number	Device Marking		
LM80CIMT-3[1] LM80CIMTX-3 [2]	LM80CIMT-3	MTC24B	3.3V
LM80CIMT-5[1] LM80CIMTX-5[2]	LM80CIMT-5	MTC24B	5.0V

Note: [1]-Rail transport media, 62 parts per rail
[2]-Tape and reel transport media, 3400 parts per reel

Connection Diagram



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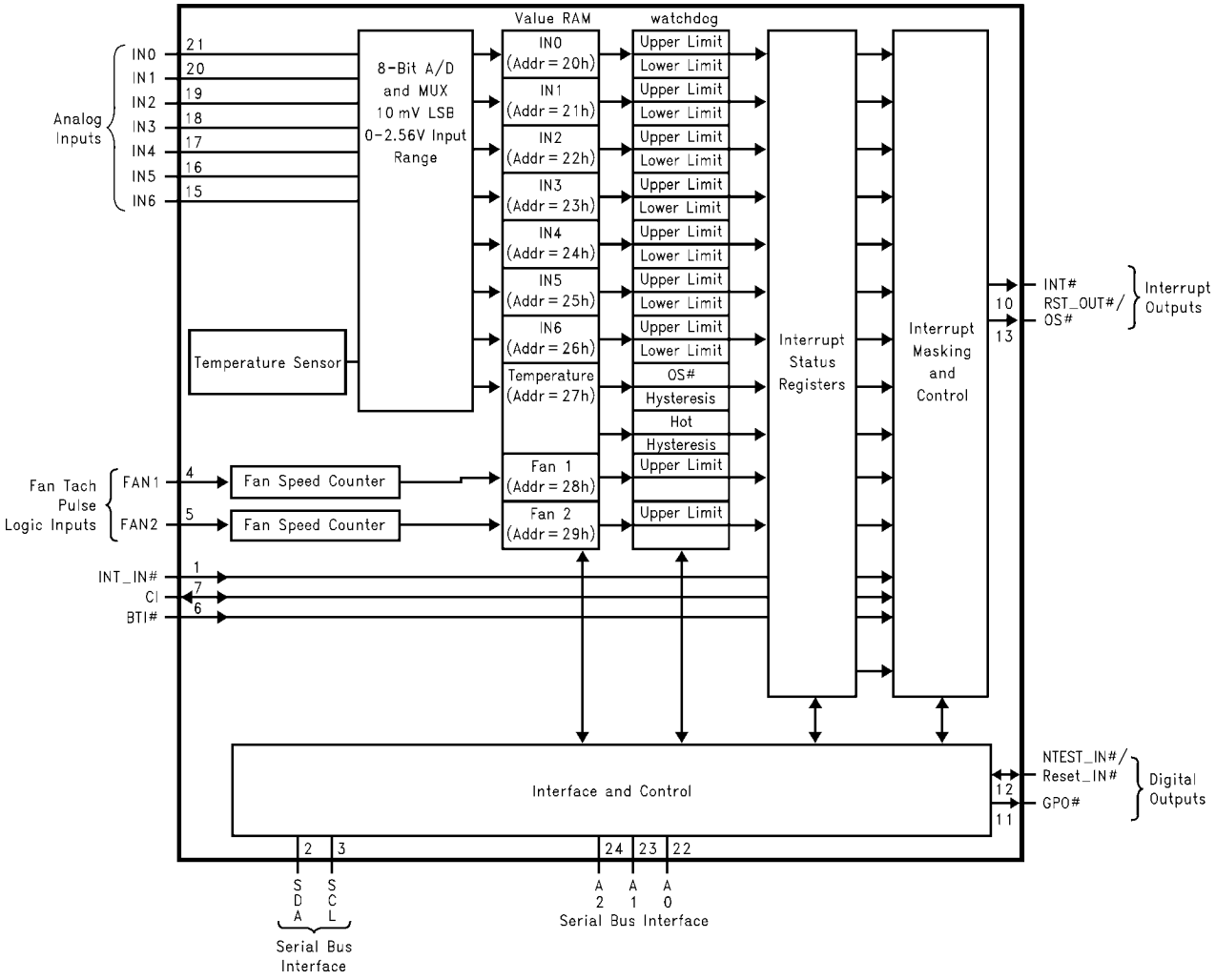
Block Diagram



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Pin Descriptions

Pin Name(s)	Pin Number	Number of Pins	Type	Description
$\overline{\text{INT_IN}}$	1	1	Digital Input	This is an active low input that propagates the $\overline{\text{INT_IN}}$ signal to the $\overline{\text{INT}}$ output of the LM80 via Interrupt Mask Register 1 Bit 7 and $\overline{\text{INT}}$ enable Bit 1 of the Configuration Register.
SDA	2	1	Digital I/O	Serial Bus bidirectional Data. Open-drain output.
SCL	3	1	Digital Input	Serial Bus Clock.
FAN1-FAN2	4-5	2	Digital Inputs	0 to V^+ fan tachometer inputs.
$\overline{\text{BTI}}$	6	1	Digital Input	Board Temperature Interrupt driven by O.S. outputs of additional temperature sensors such as LM75. Provides internal pull-up of 10 kΩ.
CI (Chassis Intrusion)	7	1	Digital I/O	An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM80. The LM80 provides an internal open drain on this line, controlled by Bit 5 of the Configuration Register, to provide a minimum 10 ms reset of this line.
GND	8	1	GROUND	Internally connected to all of the digital circuitry.
V^+ (+2.8V to +5.75V)	9	1	POWER	+3.3V or +5V V^+ power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
$\overline{\text{INT}}$	10	1	Digital Output	Non-Maskable Interrupt (open source)/$\overline{\text{Interrupt Request}}$ (open drain). The mode is selected with Bit 5 of the Configuration Register and the output is enabled when Bit 1 of the Configuration Register is set to 1. The default state is disabled.
$\overline{\text{GPO}}$ ($\overline{\text{Power Switch Bypass}}$)	11	1	Digital Output	An active low open drain output intended to drive an external P-channel power MOSFET for software power control.
$\overline{\text{NTEST_IN}}$/ $\overline{\text{RESET_IN}}$	12	1	Digital Input	An active-low input that enables NAND Tree board-level connectivity testing. Refer to Section 10.0 on NAND Tree testing. Whenever NAND Tree connectivity is enabled the LM80 is also reset to its power on state.
$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$	13	1	Digital Output	Master Reset, 5 mA driver (open drain), active low output with a 10 ms minimum pulse width. Available when enabled via Bit 4 in Configuration Register and Bit 7 of the Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register. Bit 6 of the Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register enables this output as an active low Overtemperature Shutdown ($\overline{\text{OS}}$).
GNDA	14	1	GROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs. This pin needs to be taken to a low noise analog ground plane for optimum performance.
IN6-IN0	15-21	7	Analog Inputs	0V to 2.56V full scale range Analog Inputs.
A0/NTEST_OUT	22	1	Digital I/O	The lowest order bit of the Serial Bus Address. This pin functions as an output when doing a NAND Tree test.
A1-A2	23-24	2	Digital Inputs	The two highest order bits of the Serial Bus Address.
TOTAL PINS		**24**		

Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage (V^+)	6.5V
Voltage on Any Input or Output Pin	−0.3V to (V^++0.3V)
Ground Difference (GND - GNDA)	±300 mV
Input Current at any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Maximum Junction Temperature (T_J max)	150°C
ESD Susceptibility(Note 5)	
Human Body Model	2000V
Machine Model	125V
Soldering Information	
MTC24B Package (Note 6) :	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	235°C
Storage Temperature	−65°C to +150°C
For soldering specifications, see product folder at www.national.com and www.national.com/ms/MS/MS-SOLDERING.pdf	

Operating Ratings (Note 1, Note 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM80CIMT-3, LM80CIMT-5	−25°C ≤ T_A ≤ +125°C
Specified Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM80CIMT-3, LM80CIMT-5	−25°C ≤ T_A ≤ +125°C
Junction to Ambient Thermal Resistance (θ_{JA}(Note 4))	
NS Package Number: MTC24B	95°C/W
Supply Voltage (V^+)	+2.8V to +5.75V
Ground Difference (|GND − GNDA|)	≤ 100 mV
V_{IN} Voltage Range:	−0.05V to V^+ + 0.05V

DC Electrical Characteristics

The following specifications apply for +2.8 V_{DC} ≤V^+ ≤ +3.8 V_{DC} for LM80CIMT-3, +4.25 V_{DC} ≤V^+ ≤ +5.75 V_{DC} for LM80CIMT-5, IN0-IN6 R_S = 25Ω, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (Note 7)

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
I^+	Supply Current	Interface Inactive and V^+= 5.75V	0.2	**2.0**	mA (max)
		Interface Inactive and V^+= 3.8V	0.18	**1.5**	mA (max)
		Shutdown Mode	15		µA
TEMPERATURE-to-DIGITAL CONVERTER CHARACTERISTICS					
	Temperature Error	−25°C ≤ T_A ≤ +125°C		**±3**	°C (max)
	Resolution			**0.5**	°C (min)
ANALOG-to-DIGITAL CONVERTER CHARACTERISTICS					
	Resolution (8 bits with full-scale at 2.56V)		10		mV
TUE	Total Unadjusted Error	(Note 10)		**±1**	% (max)
DNL	Differential Non-Linearity			**±1**	LSB (max)
PSS	Power Supply Sensitivity		±1		%/V
t_C	Total Monitoring Cycle Time	(Note 11) 9-bit Temp resolution 12-bit Temp resolution	1.0	**1.5** **2**	sec (max) sec (max)
MULTIPLEXER/ADC INPUT CHARACTERISTICS					
	On Resistance		0.5	**10**	kΩ (max)
	Input Current (On Channel Leakage Current)		±1		µA
	Off Channel Leakage Current		±1		µA

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
FAN RPM-to-DIGITAL CONVERTER					
	Fan RPM Error	+25°C ≤ T_A ≤ +75°C		**±10**	% (max)
		−10°C ≤ T_A ≤ +100°C		**±15**	% (max)
		−25°C ≤ T_A ≤ +125°C		**±20**	% (max)
	Full-scale Count			**255**	(max)
	FAN1 and FAN2 Nominal Input RPM (See *Section 6.0*)	Divisor = 1, Fan Count = 153 (*Note 12*)	8800		RPM
		Divisor = 2, Fan Count = 153 (*Note 12*)	4400		RPM
		Divisor = 3, Fan Count = 153 (*Note 12*)	2200		RPM
		Divisor = 4, Fan Count = 153 (*Note 12*)	1100		RPM
	Internal Clock Frequency	+25°C ≤ T_A ≤ +75°C	22.5	**20.2** **24.8**	kHz (min) kHz (max)
		−10°C ≤ T_A ≤ +100°C	22.5	**19.1** **25.9**	kHz (min) kHz (max)
		−25°C ≤ T_A ≤ +125°C	22.5	**18** **27**	kHz (min) kHz (max)
DIGITAL OUTPUTS: A0/NTEST_OUT, $\overline{\text{INT}}$					
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = +5.0 mA at V+ = +4.25V, I_{OUT} = +3.0 mA at V+ = +2.8V		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = −5.0 mA at V+ = +5.75V, I_{OUT} = −3.0 mA at V+ = +3.8V		**0.4**	V (max)
OPEN DRAIN OUTPUTS: $\overline{\text{GPO}}$, $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$, CI					
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} =− 5.0 mA at V+ = +5.75V, I_{OUT} = −3.0 mA at V+ = +3.8V		**0.4**	V (min)
I_{OH}	High Level Output Current	V_{OUT} = V+	0.1	**100**	µA (max)
	$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$, CI Pulse Width		30	**10**	ms (min)
OPEN DRAIN SERIAL BUS OUTPUT: SDA					
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = −3.0 mA at V+ = +5.75V, I_{OUT} = −3.0 mA at V+ = +3.8V		**0.4**	V (min)
I_{OH}	High Level Output Current	V_{OUT} = V+	0.1	**100**	µA (max)
DIGITAL INPUTS: A0/NTEST_Out, A1-A2, $\overline{\text{BTI}}$, CI (Chassis Intrusion), $\overline{\text{INT_IN}}$, and $\overline{\text{NTEST_IN}}$/Reset_IN					
$V_{IN(1)}$	Logical "1" Input Voltage			**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage			**0.8**	V (max)
SERIAL BUS INPUTS (SCL, SDA) and FAN TACH PULSE INPUTS (FAN1, FAN2)					
$V_{IN(1)}$	Logical "1" Input Voltage			**0.7 × V+**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage			**0.3 × V+**	V (max)
ALL DIGITAL INPUTS Except for $\overline{\text{BTI}}$					
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = V+	−0.005	**−1**	µA (min)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0 V_{DC}	0.005	**1**	µA (max)
C_{IN}	Digital Input Capacitance		20		pF
$\overline{\text{BTI}}$ Digital Input					
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = V+	−1	**−10**	µA (min)
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0 V_{DC}	500	**2000**	µA (max)
C_{IN}	Digital Input Capacitance		20		pF

AC Electrical Characteristics

The following specifications apply for +2.8 V_{DC} ≤V+ ≤ +3.8 V_{DC} for LM80CIMT-3, +4.25 V_{DC} ≤V+ ≤ +5.75 V_{DC} for LM80CIMT-5, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C. (*Note 13*)

Symbol	Parameter	Conditions	Typical (*Note 8*)	Limits (*Note 9*)	Units (Limits)
SERIAL BUS TIMING CHARACTERISTICS					
t_1	SCL (Clock) Period			**2.5**	µs (min)
t_2	Data In Setup Time to SCL High			**100**	ns (min)
t_3	Data Out Stable After SCL Low			**0**	ns (min)
t_4	SDA Low Setup Time to SCL Low (start)			**100**	ns (min)
t_5	SDA High Hold Time After SCL High (stop)			**100**	ns (min)

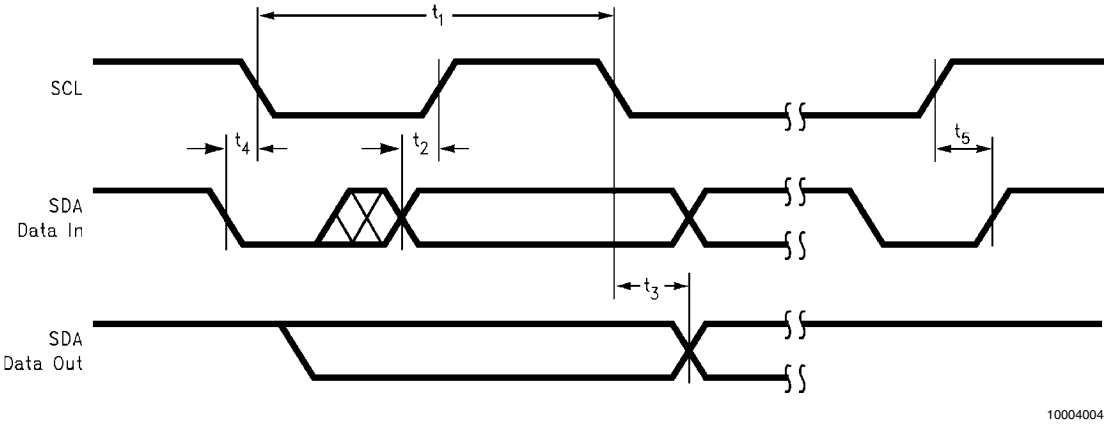


FIGURE 1. Serial Bus Timing Diagram

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified

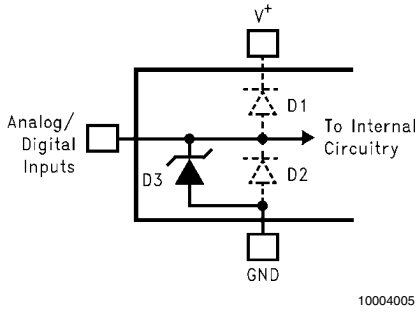
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}< (GND or GNDA) or V_{IN}>V+), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J max - T_A)/\theta_{JA}$.

Note 5: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 6: See the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Each input and output is protected by a nominal 6.5V breakdown voltage zener diode to GND; as shown below, input voltage magnitude up to 0.3V above V+ or 0.3V below GND will not damage the LM80. There are parasitic diodes that exist between the inputs and the power supply rails. Errors in the ADC conversion can occur if these diodes are forward biased by more than 50 mV. As an example, if V+ is 4.50 V_{DC}, input voltage must be ≤ 4.55 V_{DC}, to ensure accurate conversions.



An x indicates that the diode exists.

Pin Name	D1	D2	D3		Pin Name	D1	D2	D3
$\overline{\text{INT_IN}}$	x	x	x		$\overline{\text{NTEST_IN}}$/ $\overline{\text{Reset_IN}}$			x
CI		x	x		IN0-IN6	x	x	x
$\overline{\text{GPO}}$		x	x		$\overline{\text{BTI}}$	x	x	x
FAN1–FAN2			x		$\overline{\text{INT}}$	x	x	x
SCL			x		A1-A2	x	x	x
SDA		x	x		A0/NTEST_Out	x	x	x
$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$		x						

FIGURE 2. ESD Protection Input Structure

Note 8: Typicals are at T_J=T_A=25°C and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

Note 11: Total Monitoring Cycle Time includes temperature conversion, 7 analog input voltage conversions and 2 tachometer readings. Each input voltage conversion takes 100 ms typical and 112 ms maximum. 8-plus sign Temperature resolution takes 100 ms typical and 112 ms maximum, while 11-bit plus sign takes 800 ms typical and 900 ms maximum. Fan tachometer readings take 20 ms typical, at 4400 rpm, and 200 ms max.

Note 12: The total fan count is based on 2 pulses per revolution of the fan tachometer output.

Note 13: Timing specifications are tested at the Serial Bus Input logic levels, $V_{IN(0)}$ = 0.3 × V+ for a falling edge and $V_{IN(1)}$ =0.7 × V+ for a rising edge, when the SCL and SDA edge rates are similar.

Test Circuit

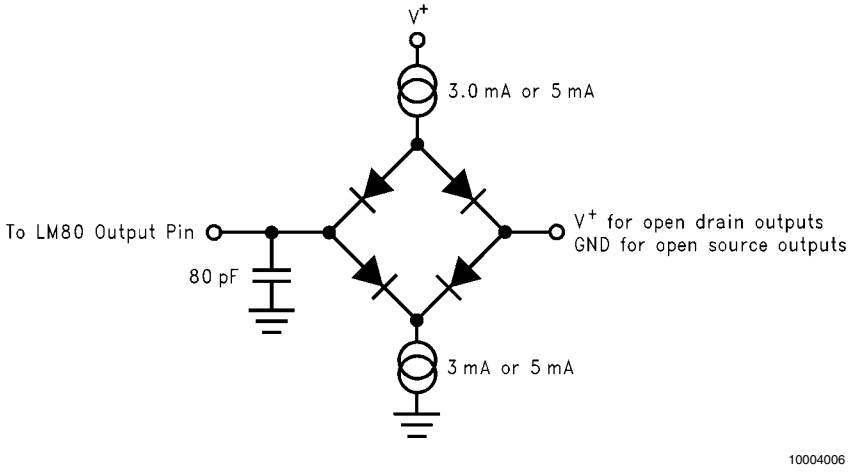


FIGURE 3. Digital Output Load Test Circuitry

Functional Description

1.0 GENERAL DESCRIPTION

The LM80 provides 7 analog inputs, a temperature sensor, a Delta-Sigma ADC (Analog-to-Digital Converter), 2 fan speed counters, WATCHDOG registers, and a variety of inputs and outputs on a single chip. A two wire Serial Bus interface is provided. The LM80 performs power supply, temperature, fan control and fan monitoring for personal computers.

The LM80 continuously converts analog inputs to 8-bit digital words with a 10 mV LSB (Least Significant Bit) weighting, yielding input ranges of 0 to 2.56V. The Analog inputs are intended to be connected to the several power supplies present in a a typical computer. Temperature can be converted to a 9-bit or 12-bit two's complement word with resolutions of 0.5°C LSB or 0.0625°C LSB, respectively.

Fan inputs can be programmed to accept either fan failure indicator or tachometer signals. Fan failure signals can be programmed to be either active high or active low. Fan inputs measure the period of tachometer pulses from the the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with and acceptable range of 0 to V^+ volts and a transition level of approximately $V^+/2$ volts. Full scale fan counts are 255 (8-bit counter), which represent a stopped or very slow fan. Nominal speed based on a count of 153, are programmable from 1100 to 8800 RPM. Signal conditioning circuitry is included to accommodate slow rise and fall times.

The LM80 provides a number of internal registers, as detailed in *Figure 4*. These include:

Configuration Register: Provides control and configuration.

Interrupt Status Registers: Two registers to provide status of each WATCHDOG limit or Interrupt event.

Interrupt Mask Registers: Allows masking of individual Interrupt sources, as well as separate masking for each of both hardware Interrupt outputs.

Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Registers: Bits 0-5 of this register contain the divisor bits for FAN1 and FAN2 inputs. Bits 6-7 control the function of the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ output.

$\overline{\text{OS}}$ Configuration/Temperature Resolution Register: The configuration of the $\overline{\text{OS}}$ (Overtemperature Shutdown) is controlled by the lower 3 bits of this register. Bit 3 enables 12-bit temperature conversions. Bits 4-7 reflect the lower four bits of the temperature reading for a 12-bit resolution.

Value RAM: The monitoring results: temperature, voltages, fan counts, and Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register limits are all contained in the Value RAM. The Value RAM consists of a total of 32 bytes. The first 10 bytes are all of the results, the next 20 bytes are the Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register limits, and are located at 20h-3Fh, including two unused bytes in the upper locations.

When the LM80 is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every second. Each measured value is compared to values stored in WATCHDOG, or Limit registers. When the measured value violates the programmed limit the LM80 will set a corresponding Interrupt in the Interrupt Status Registers. Two hardware Interrupt lines, $\overline{\text{INT}}$ and $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ are available. $\overline{\text{INT}}$ is fully programmable with masking of each Interrupt source, and masking of each output. $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ is dedicated to the temperature reading WATCHDOG registers. In addition, the Fan Divisor register has control bits to enable or disable the hardware Interrupts.

Additional digital inputs are provided for chaining of $\overline{\text{INT}}$, outputs of multiple external LM75 temperature sensors via the $\overline{\text{BTI}}$ (Board Temperature Interrupt) input, and a CI (Chassis Intrusion) input. The Chassis Intrusion input is designed to accept an active high signal from an external circuit that latches when the case is removed from the computer.

2.0 INTERFACE

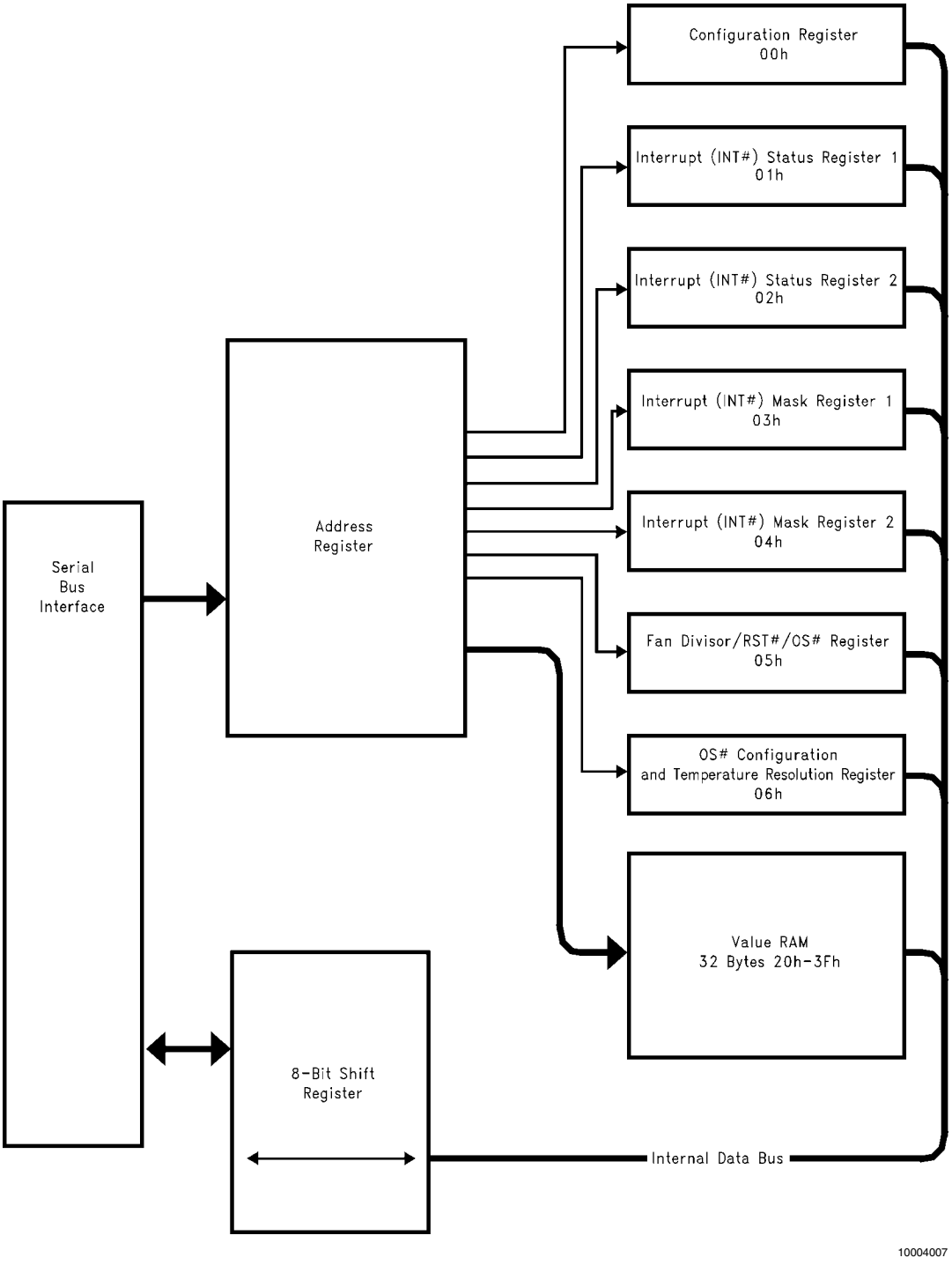


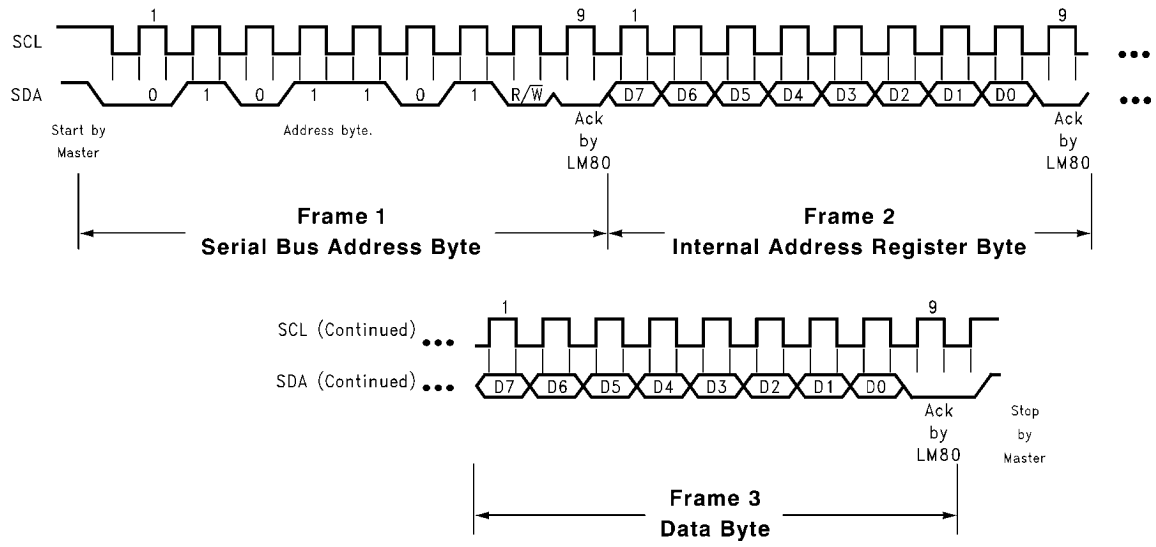
FIGURE 4. LM80 Register Structure

2.1 Internal Registers of the LM80

TABLE 1. The internal registers and their corresponding internal LM80 address is as follows:

Register	LM80 Internal Hex Address (This is the data to be written to the Address Register)	Power on Value	Notes
Configuration Register	00h	0000 1000	
Interrupt Status Register 1	01h	0000 0000	
Interrupt Status Register 2	02h	0000 0000	
Interrupt Mask Register 1	03h	0000 0000	
Interrupt Mask Register 2	04h	0000 0000	
Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register	05h	0001 0100	FAN1 and FAN2 divisor = 2 (count of 153 = 4400 RPM)
$\overline{\text{OS}}$/ Configuration and Temperature Resolution Register	06h	0000 0001	
Value RAM	20h-3Fh		

2.2 Serial Bus Interface



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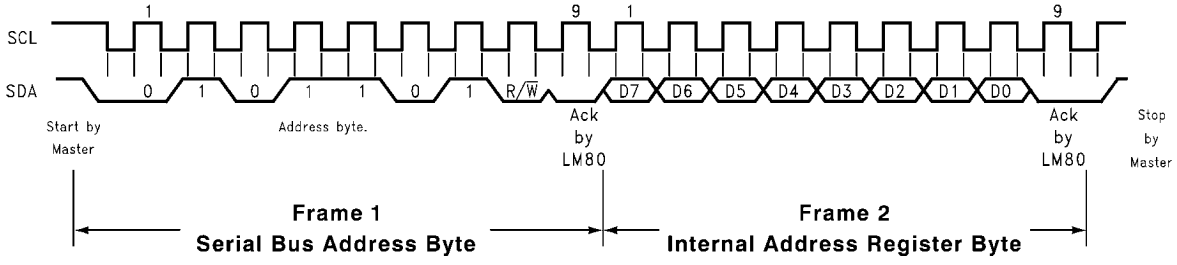
(a) Serial Bus Write to the Internal Address Register followed by the Data Byte



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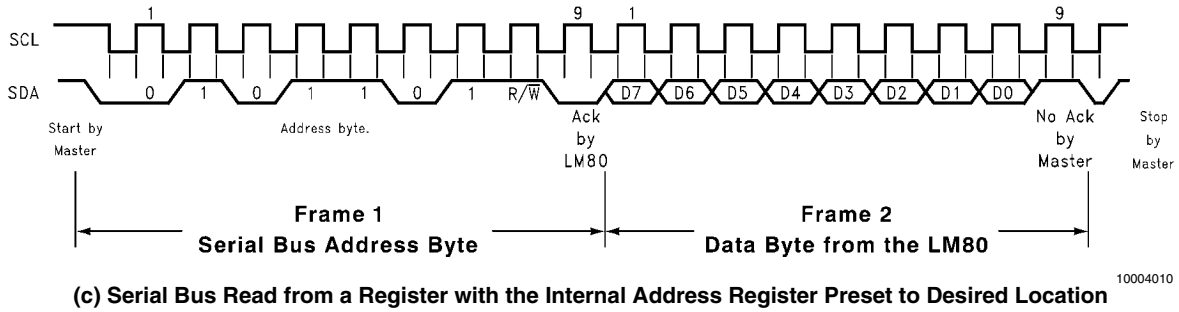
(b) Serial Bus Write to the Internal Address Register Only



(c) Serial Bus Read from a Register with the Internal Address Register Preset to Desired Location

FIGURE 5. Serial Bus Timing

The Serial Bus control lines consists of the SDA (serial data), SCL (serial clock) and A0-A1 (address) pins. The LM80 can only operate as a slave. The SCL line only controls the serial interface, all other clock functions within LM80 such as the ADC and fan counters are done with a separate asynchronous internal clock.

When using the Serial Bus Interface a write will always consist of the LM80 Serial Bus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. If the Internal Address Register is known to be at the desired Address, simply read the LM80 with the Serial Bus Interface Address byte, followed by the data byte read from the LM80.
2. If the Internal Address Register value is unknown, write to the LM80 with the Serial Bus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Interface Address byte, followed by the data byte read from the LM80.

The default power on Serial Bus address for the LM80 is: 0101 (A2)(A1)(A0) binary, where A0-A2 reflect the state of the pins defined by the same names.

All of these communications are depicted in the Serial Bus Interface Timing Diagrams as shown in *Figure 5*.

3.0 USING THE LM80

3.1 Power On

When power is first applied, the LM80 performs a "power on reset" on several of its registers. The power on condition of registers is shown in *Table 1*. Registers whose power on values are not shown have power on conditions that are indeterminate (this includes the value RAM and WATCHDOG limits). The ADC is inactive. In most applications, usually the first action after power on would be to write WATCHDOG limits into the Value RAM.

3.2 Resets

Configuration Register INITIALIZATION accomplishes the same function as power on reset. The Value RAM conversion results, and Value RAM WATCHDOG limits are not Reset and will be indeterminate immediately after power on. If the Value RAM contains valid conversion results and/or Value RAM WATCHDOG limits have been previously set, they will not be affected by a Configuration Register INITIALIZATION. Power on reset, or Configuration Register INITIALIZATION, clear or initialize the following registers (the initialized values are shown in *Table 1*):

Configuration Register
Interrupt Status Register 1
Interrupt Status Register 2
Interrupt Mask Register 1
Interrupt Mask Register 2
Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register
$\overline{\text{OS}}$ Configuration/Temperature Resolution Register
Value Ram (Registers at Address 20h - 3Fh, which include: Temperature reading, IN0-IN6 readings, FAN1 and FAN2 readings, and WATCHDOG limits)

Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This Bit automatically clears after being set.

The LM80 can be reset to it's "power on state" by taking $\overline{\text{NTEST_IN}}$/$\overline{\text{Reset_IN}}$ pin low for at least 50 ns.

3.3 Using the Configuration Register

The Configuration Register provides all control over the LM80. At power on, the ADC is stopped and INT_Clear is asserted, clearing the $\overline{\text{INT}}$ and $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ hardwire outputs. The Configuration Register starts and stops the LM80, enables and disables $\overline{\text{INT}}$ outputs, clears and sets CI and $\overline{\text{GPO}}$ I/O pins, initiates reset pulse on $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin, and provides the Reset function described in *Section 3.2*.

Bit 0 of the Configuration Register controls the monitoring loop of the LM80. Setting Bit 0 low stops the LM80 monitoring loop and puts the LM80 in shutdown mode, reducing power consumption. Serial Bus communication is possible with any register in the LM80 although activity on these lines will increase shutdown current, up to as much as maximum rated supply current, while the activity takes place. Taking Bit 0 high starts the monitoring loop, described in more detail subsequently.

Bit 1 of the Configuration Register enables the $\overline{\text{INT}}$ Interrupt hardwire output when this bit is taken high.

Bit 2 of the Configuration Register defines whether the $\overline{\text{INT}}$ pin is open source or open drain.

Bit 3 clears the $\overline{\text{INT}}$ output when taken high. The LM80 monitoring function will stop until bit 3 is taken low. The content of the Interrupt ($\overline{\text{INT}}$) Status Registers will not be affected.

Bit4, when taken high, will initiate a 10 ms RESET signal on the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ output (when this pin is in the $\overline{\text{RST}}$ mode).

When bit 5 is taken high the CI (Chassis Intrusion) pin is reset.

Bit 6 of the configuration register sets or clears the $\overline{\text{GPO}}$ output. This pin can be used in software power control by activating an external power control MOSFET.

3.4 Starting Conversions

3.4 STARTING CONVERSION The monitoring function (Analog inputs, temperature, and fan speeds) in the LM80 is started by writing to the Configuration Register and setting INT_Clear (Bit 3), low, and Start (Bit 0), high. The LM80 then performs a round-robin monitoring of all analog inputs, temperature, and fan speed inputs approximately once a second. If the temperature resolution is set to 12 bits one complete monitoring function will take approximately 2 seconds. The sequence of items being monitored corresponds to locations in the Value RAM (except for the Temperature reading) and is:

1. Temperature
2. IN0
3. IN1
4. IN2
5. IN3
6. IN4
7. IN5
8. IN6
9. Fan 1
10. Fan 2

3.5 Reading Conversion Results

The conversion results are available in the Value RAM. Conversions can be read at any time and will provide the result of the last conversion. Because the ADC stops, and starts a new conversion whenever the conversion is read, reads of any single value should not be done more often than once every 120 ms. When reading all values with the temperature resolution set to 9-bits, allow at least 1.5 seconds between reading groups of values. Reading more frequently than once every 1.5 seconds can also prevent complete updates of Interrupt Status Registers and Interrupt Outputs. If the temperature resolution is set to 12-bit, allow at least 2.0 seconds between reading groups of values.

A typical sequence of events upon power on of the LM80 would consist of:

1. Set WATCHDOG Limits
2. Set Interrupt Masks
3. Start the LM80 monitoring process

4.0 ANALOG INPUTS

The 8-bit ADC has a 10 mV LSB, yielding a 0V to 2.55V (2.56 - 1LSB) input range. This is true for all analog inputs. In PC monitoring applications these inputs would most often be connected to power supplies. The 2.5, 3.3, ± 5 and ± 12 volt inputs should be attenuated with external resistors to any desired value within the input range. Care should be taken not to exceed the power supply voltage (V^+) at any time.

A typical application, such as is shown in *Figure 6*, might select the input voltage divider to provide 1.9V at the analog inputs of the LM80. This is sufficiently high for good resolution of the voltage, yet leaves headroom for upward excursions from the supply of about 25%. To simplify the process of resistor selection, set the value of R2 first. Select a value for R2 or R4 between 10 kΩ and 100 kΩ This is low enough to avoid errors due to input leakage currents yet high enough to both protect the inputs under overdrive conditions as well as min-

imize loading of the source. Then select R1 or R3 to provide a 1.9V input as show in *Figure 6*.

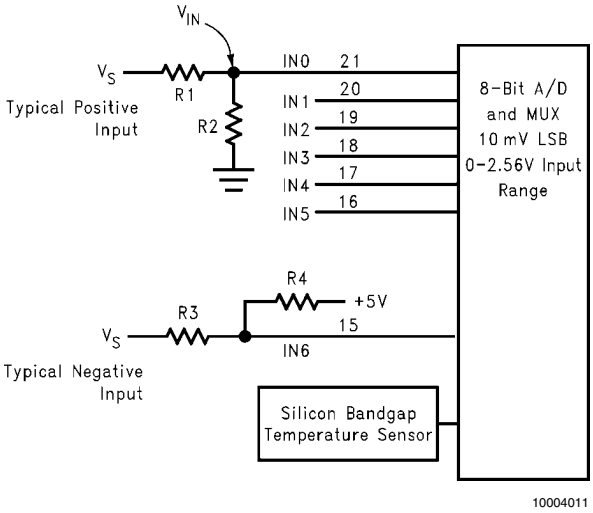


FIGURE 6. Input Examples. Resistor values shown in table provide approximately 1.9V at the analog inputs.

For positive input voltages the equation for calculating R1 is as follows:

$$R1 = [(V_S - V_{IN}) / V_{IN}] R2$$

For negative input voltages the equation for Calculating R3 is as follows:

$$R3 = [(V_S - V_{IN}) / (V_{IN} - 5V)] R4$$

The analog inputs have internal diodes that clamp inputs exceeding the power supply and ground. Exceeding any analog input has no detrimental effect on other channels. The input diodes will also clamp voltages appearing at the inputs of an un-powered LM80. External resistors should be included to limit input currents to the values given in the ABSOLUTE MAXIMUM RATINGS for Input Current At Any Pin. Inputs with the attenuator networks will usually meet these requirements. If it is possible for inputs without attenuators to be turned on while LM80 is powered off, additional resistors of about 10 kΩ should be added in series with the inputs to limit the input current.

Voltage Measurements (V_S)	R1 or R3	R2 or R4	Voltage at Analog Inputs (ADC code 190)
+2.5V	23.7 kΩ	75 kΩ	+1.9V
+3.3V	22.1 kΩ	30 kΩ	+1.9V
+5.0V	24 kΩ	14.7 kΩ	+1.9V
+12V	160 kΩ	30.1 kΩ	+1.9V
−12V	160 kΩ	35.7 kΩ	+1.9V
−5V	36 kΩ	16.2 kΩ	+1.9V

5.0 LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to the AGND pin or a supply with low noise. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers should be located physically as close as possible to the LM80.

The power supply bypass, the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors connected between pin 9 and ground, should also be located as close as possible to the LM80.

6.0 FAN INPUTS

Inputs are provided for signals from fans equipped with tachometer outputs. These are logic-level inputs with an approximate threshold of V+/2. Signal conditioning in the LM80 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to V+. In the event these inputs are supplied from fan outputs which exceed 0 to V+, either resistive division or diode clamping must be included to keep inputs within an acceptable range, as shown in *Figure 7*. R2 is selected so that it does not develop excessive error voltage due to input leakage. R1 is selected based on R2 to provide a minimum input of 2V and a maximum of V+. R1 should be as low as possible to provide the maximum possible input up to V+ for best noise immunity. Alternatively, use a shunt reference or zener diode to clamp the input level.

If fans can be powered while the power to the LM80 is off, the LM80 inputs will provide diode clamping. Limit input current to the Input Current at Any Pin specification shown in the ABSOLUTE MAXIMUM RATINGS section. In most cases, open collector outputs with pull-up resistors inherently limit this current. If this maximum current could be exceeded, either a larger pull up resistor should be used or resistors connected in series with the fan inputs.

The Fan Inputs gate an internal 22.5 kHz oscillator for one period of the Fan signal into an 8-bit counter (maximum count = 255). The default divisor, located in the VID/Fan Divisor Register, is set to 2 (choices are 1, 2, 4, and 8) providing a nominal count of 153 for a 4400 rpm fan with two pulses per revolution. Typical practice is to consider 70% of normal RPM a fan failure, at which point the count will be 219.

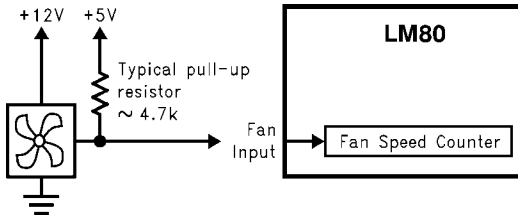
Determine the fan count according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

Note that Fan 1 and Fan 2 Divisors are programmable via the Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register.

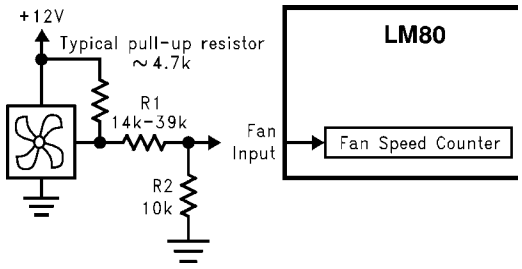
FAN1 and FAN2 inputs can also be programmed to be level sensitive digital inputs.

Fans that provide only one pulse per revolution would require a divisor set twice as high as fans that provide two pulses, thus maintaining a nominal fan count of 153. Therefore the divisor should be set to 4 for a fan that provides 1 pulse per revolution with a nominal RPM of 4400.



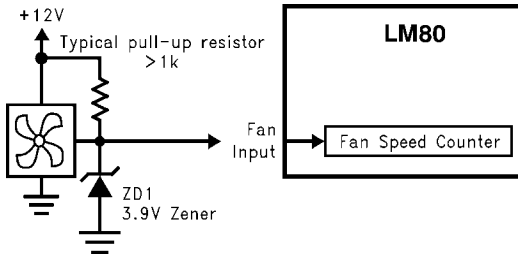
10004012

(a) Fan with Tach Pull-Up to +5V



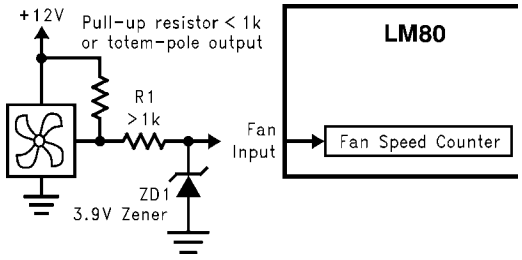
10004013

(b) Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Resistor Attenuator



10004014

(c) Fan with Tach Pull-Up to +12V and Diode Clamp



10004015

(d) Fan with Strong Tach Pull-Up or Totem Pole Output and Diode Clamp

FIGURE 7. Alternatives for Fan Inputs

Counts are based on 2 pulses per revolution tachometer outputs.

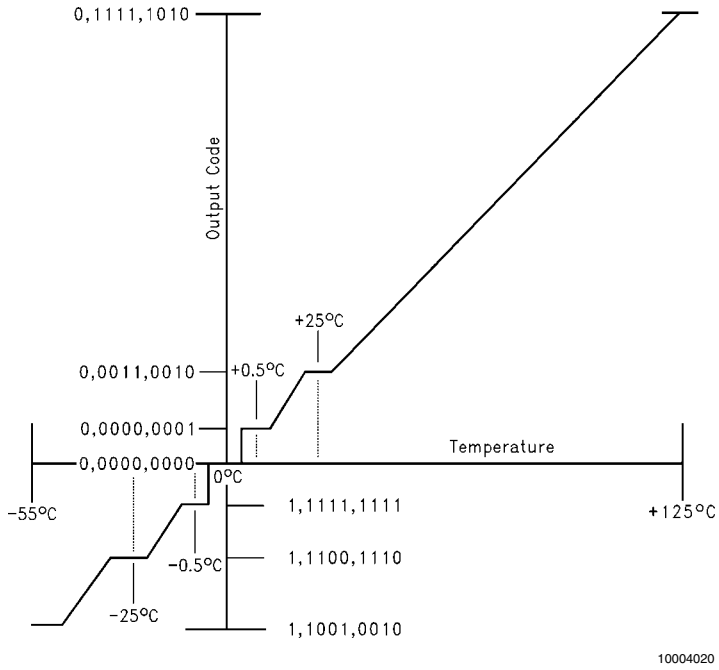
RPM	Time per Revolution	Counts for "Divide by 2" (Default) in Decimal	Comments
4400	13.64 ms	153 counts	Typical RPM
3080	19.48 ms	219 counts	70% RPM
2640	22.73 ms	255 counts (maximum counts)	60% RPM

Mode Select	Nominal RPM	Time per Revolution	Counts for the Given Speed in Decimal	70% RPM	Time per Revolution for 70% RPM
Divide by 1	8800	6.82 ms	153	6160	9.74 ms
Divide by 2	4400	13.64 ms	153	3080	19.48 ms
Divide by 4	2200	27.27 ms	153	1540	38.96 ms
Divide by 8	1100	54.54 ms	153	770	77.92 ms

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

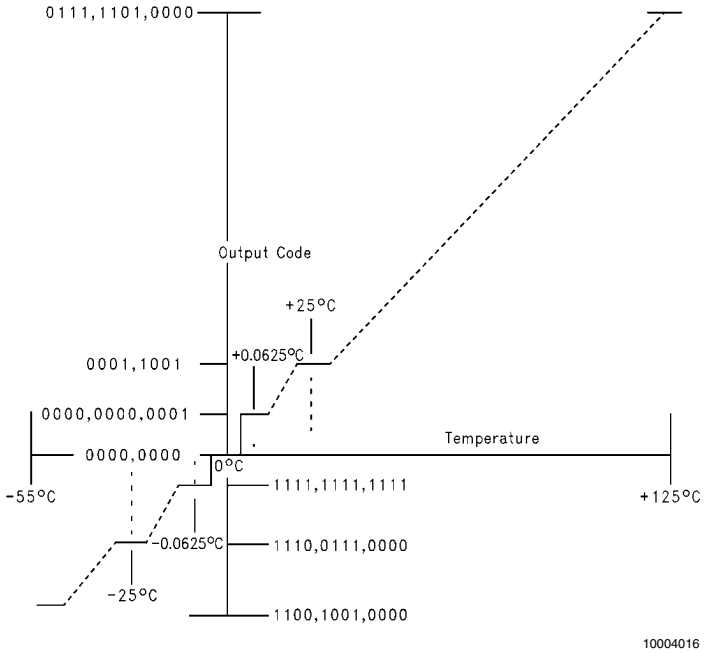
7.0 TEMPERATURE MEASUREMENT SYSTEM

The LM80 bandgap type temperature sensor and ADC perform 9-bit or a 12-bit two's-complement conversions of the temperature. An 8-bit digital comparator is also incorporated that compares the readings to the user-programmable Hot and Overtemperature setpoints, and Hysteresis values.



(Non-Linear Scale for Clarity)

FIGURE 8. 9-bit Temperature-to-Digital Transfer Function



(Non-Linear Scale for Clarity)

FIGURE 9. 12-bit Temperature-to-Digital Transfer Function

7.1 Temperature Data Format

Temperature data can be read from the Temperature, T_{hot}, $T_{hot\ hyst}$, T_{os} and $T_{os\ hyst}$ setpoint registers; and written to the T_{hot}, $T_{hot\ hyst}$, T_{os} and $T_{os\ hyst}$ setpoint registers. These registers are located in register addresses 38h - 3Bh, and each setpoint is represented by an 8-bit, two's complement word with an LSB (Least Significant Bit) equal to 1°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1.0°C	0000 0001	01h
+0°C	0000 0000	00h
−1.0°C	1111 1111	FFh
−25°C	1110 0111	E7h
−55°C	1100 1001	C9h

By default Temperature Register data is represented by a 9-bit two's complement digital word with the LSB having a resolution of 0.5°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0 1111 1010	0 FAh
+25°C	0 0011 0010	0 32h
+1.5°C	0 0000 0011	0 03h
+0°C	0 0000 0000	0 00h
−0.5°C	1 1111 1111	1 FFh
−25°C	1 1100 1110	1 CEh
−55°C	1 1001 0010	1 92h

Temperature Register data can also be represented by a 12-bit two's complement digital word with a LSB of 0.0625°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1100 0000	7 D0h
+25°C	0001 1001 0000	1 90h
+1.0°C	0000 0001 0000	0 10h
+0.0625°C	0000 0000 0001	0 01h
0°C	0000 0000 0000	00h
−0.0625°C	1111 1111 1111	F FFh
−1.0°C	1111 1111 0000	F F0h
−25°C	1110 0111 0000	E 70h
−55°C	1100 1001 0000	C 90h

The 8 MSBs of the Temperature reading can be found at Value RAM address 27 h. The remainder of the Temperature reading can be found in the $\overline{OS}$ Configuration/Temperature Resolution Register bits 7-4. In 9-bit format bit 7 is the only valid bit.

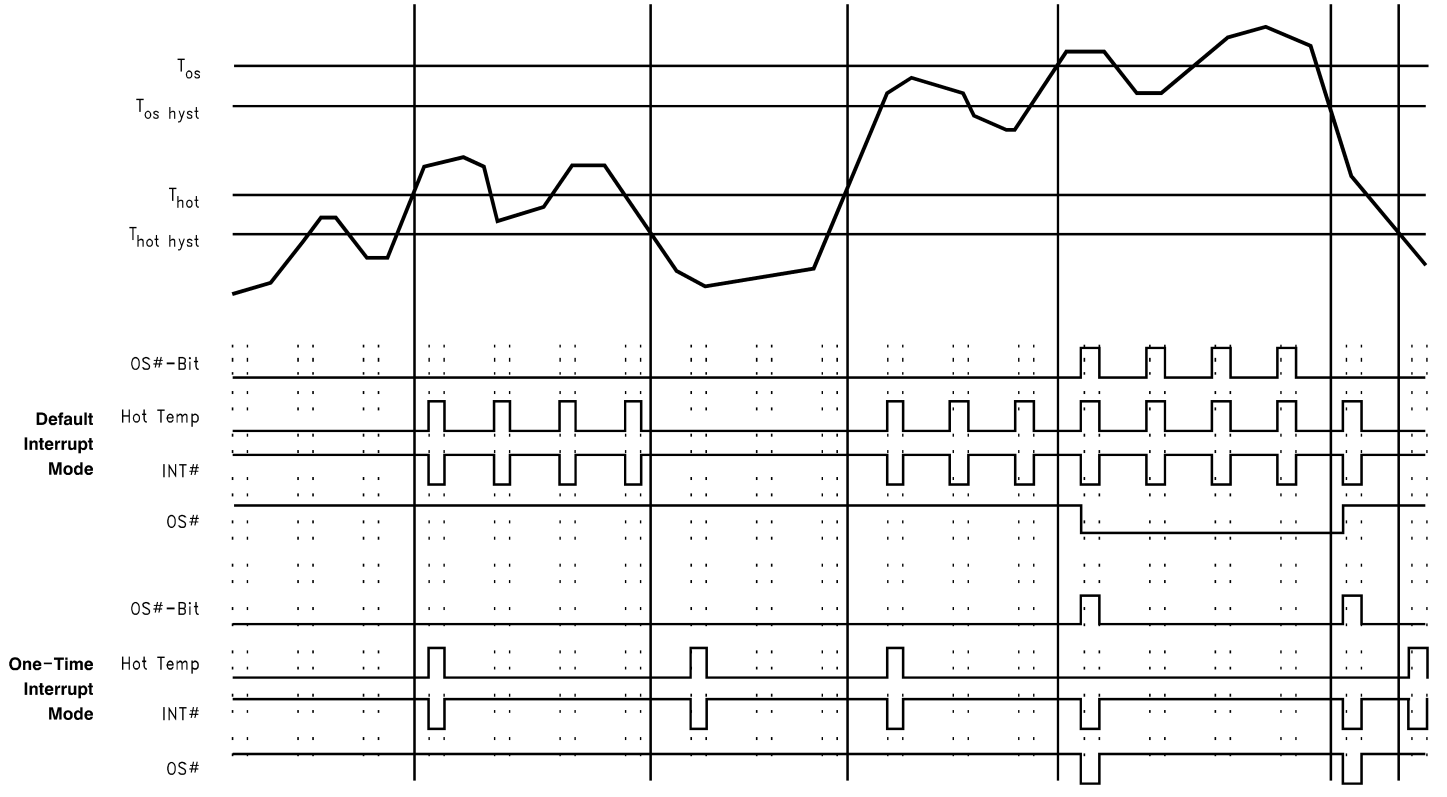
7.2 Temperature Interrupts

There are four Value RAM WATCHDOG limits for the Temperature reading that affect the $\overline{INT}$ and $\overline{OS}$ outputs of the LM80. They are: Hot Temperature Limit, Hot Temperature Hysteresis Limit, OS Limit, OS Hysteresis Limit. There are three interrupt modes of operation: "One-Time Interrupt" mode, "Default Interrupt" mode, and "Comparator Mode". The $\overline{OS}$ output of the LM80 can be programmed for "One-Time Interrupt" mode and "Comparator" mode. $\overline{INT}$ can be programmed for "Default Interrupt" mode and "One-Time" Interrupt.

"Default Interrupt mode" operates in the following way: Exceeding T_{hot} causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an Interrupt event has occurred by crossing T_{hot}, then reset, an Interrupt will occur again once the next temperature conversion has completed. The interrupts will continue to occur in this manner until the temperature goes below $T_{hot\ hyst}$, at which time the Interrupt output will automatically clear.

"One-Time Interrupt" mode operates in the following way: Exceeding T_{hot} causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an Interrupt event has occurred by crossing T_{hot}, then reset, an Interrupt will not occur again until the temperature goes below $T_{hot\ hyst}$.

"Comparator" mode operates in the following way: Exceeding T_{os} causes the $\overline{OS}$ output to go Low (default). $\overline{OS}$ will remain Low until the temperature goes below T_{os}. Once the temperature goes below T_{os}, OS will go High.



Temperature Interrupt Response Diagram. This diagram does not reflect all the possible variations in the operation of the $\overline{OS}$ and $\overline{INT}$ outputs nor the OS and Hot Temp bits. The interrupt outputs are cleared by reading the appropriate Interrupt Status Register.

8.0 THE LM80 INTERRUPT STRUCTURE

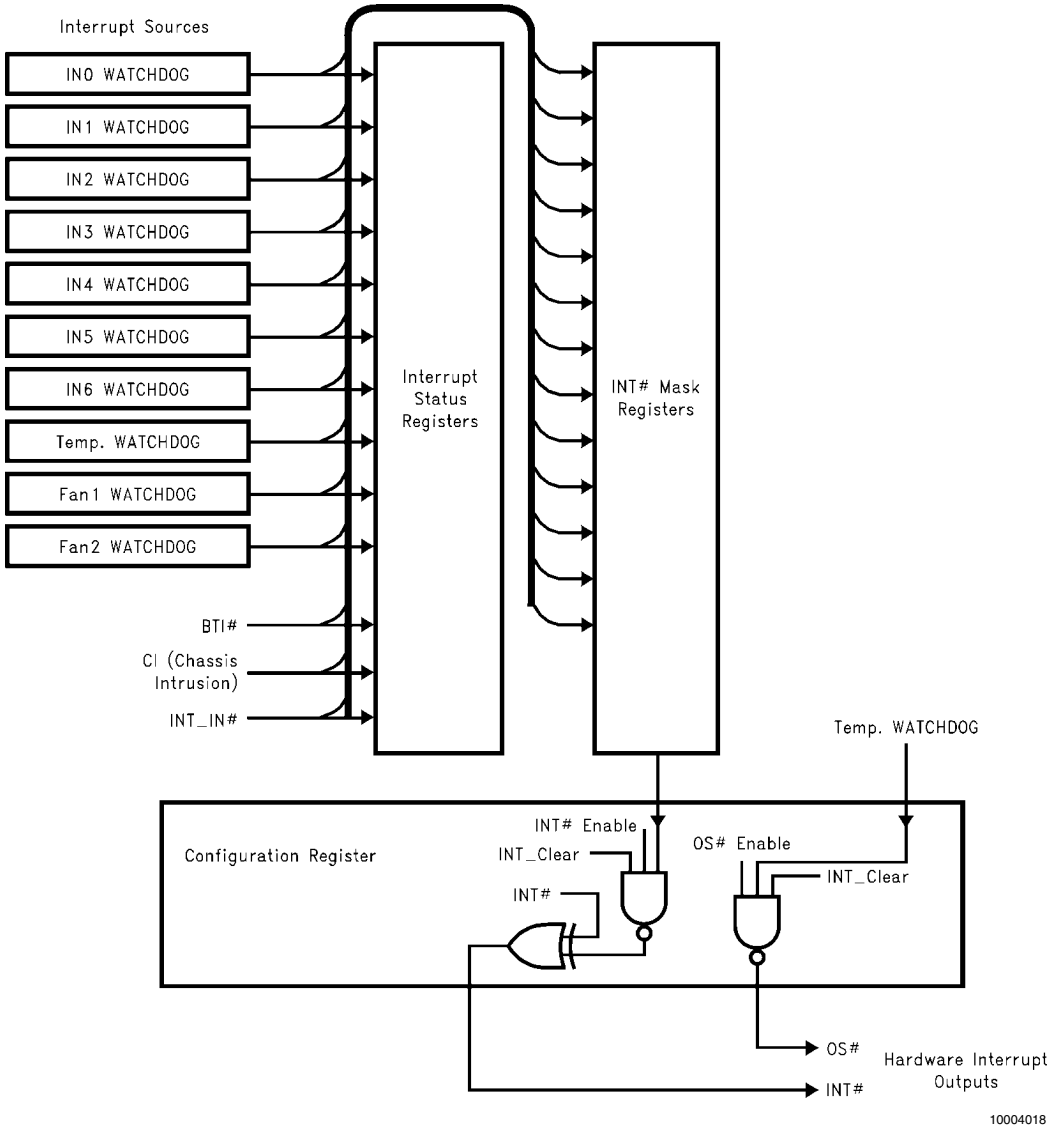


FIGURE 10. Interrupt Structure

Figure 10 depicts the Interrupt Structure of the LM80. The LM80 can generate Interrupts as a result of each of its internal WATCHDOG registers on the analog, temperature, and fan inputs.

8.1 Interrupt Inputs

External Interrupts can come from the following sources. While the label suggests a specific type or source of Interrupt, this label is not a restriction of its usage, and it could come from any desired source:

- **$\overline{\text{BTI}}$ -** This is an active low Interrupt intended to come from the O.S. output of LM75 temperature sensors. The LM75 O.S. output goes active when its temperature exceeds a programmed threshold. Up to 8 LM75's can be connected to a single Serial Bus bus with their O.S. output's wire or'd to the $\overline{\text{BTI}}$ input of the LM80. If the temperature of any LM75 exceeds its programmed limit, it drives $\overline{\text{BTI}}$ low. This generates an Interrupt to notify the host of a possible overtemperature condition. Provides an internal pull-up of 10 kΩ.
- **CI (Chassis Intrusion) -** This is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This could be accomplished mechanically, optically, or electrically, and circuitry external to the LM80 is expected to latch the event. The design of the LM80 allows this input to go high even with no power applied to the LM80, and no clamping or other interference with the line will occur. This line can also be pulled low for at least 10 ms by the LM80 to reset a typical Chassis Intrusion circuit. Accomplish this reset by setting Bit 5 of Configuration Register high. The bit in the Register is self-clearing.
- **$\overline{\text{INT_IN}}$ -** This active low Interrupt merely provides a way to chain the $\overline{\text{INT}}$ (Interrupt) from other devices through the LM80 to the processor.

8.2 Interrupt Outputs

All Interrupts are indicated in the two Interrupt Status Registers.

$\overline{\text{INT}}$ output has two mask registers, and individual masks for each Interrupt. As described in Section 3.3, this hardware Interrupt line can also be enabled/disabled in the Configuration Register. The Configuration Register is also used to set the mode of the $\overline{\text{INT}}$ Interrupt line.

$\overline{\text{OS}}$ is dedicated to the Temperature reading WATCHDOG. In the "Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register" the $\overline{\text{OS}}$ enable bit (Bit-6), must be set high and the $\overline{\text{RST}}$ enable bit (Bit -7) must be set low to enable the $\overline{\text{OS}}$ function on the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin. $\overline{\text{OS}}$ pin has two modes of operation: "One-Time Interrupt" and "Comparator". "One-Time Interrupt" mode is selected by taking bit-2 of the "$\overline{\text{OS}}$ Configuration/Temperature Resolution Register" high. If bit-2 is taken low "Comparator" mode is selected. Unlike the $\overline{\text{OS}}$ pin, the $\overline{\text{OS}}$ bit in "Interrupt Status Register 2" functions in "Default Interrupt" and "One-Time Interrupt" modes. The $\overline{\text{OS}}$ bit can be masked to $\overline{\text{INT}}$ pin by taking bit-5 in the "Interrupt Mask Register 2" low. A description of "Comparator", "Default Interrupt" and "One-Time Interrupt" modes can be found in Section 7.1.

8.3 Interrupt Clearing

Reading an Interrupt Status Register will output the contents of the Register, and reset the Register. A subsequent read done before the analog "round-robin" monitoring loop is complete will indicate a cleared Register. Allow at least 1.5 seconds to allow all Registers to be updated between reads. In summary, the Interrupt Status Register clears upon being read, and requires at least 1.5 seconds to be updated. When the Interrupt Status Register clears, the hardwire interrupt line will also clear until the Registers are updated by the monitoring loop. The hardware Interrupt lines are cleared with the INT_Clear bit, which is Bit 3 of the Configuration Register, without affecting the contents of the Interrupt ($\overline{\text{INT}}$) Status Registers. When this bit is high, the LM80 monitoring loop will stop. It will resume when the bit is low.

9.0 $\overline{\text{RST}}$ and $\overline{\text{GPO}}$ OUTPUTS

In PC applications the open drain $\overline{\text{GPO}}$ provides a gate drive signal to an external P-channel MOSFET power switch. This external MOSFET then would keep power turned on regardless of the state of front panel power switches when software power control is used. In any given application this signal is not limited to the function described by its label. For example, since the LM80 incorporates temperature sensing, the $\overline{\text{GPO}}$ output could also be utilized to control power to a cooling fan. Take $\overline{\text{GPO}}$ active low by setting Bit 6 in the Configuration Register low.

$\overline{\text{RST}}$ is intended to provide a master reset to devices connected to this line. The $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Control bit in Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register, Bit 7, must be set high to enable this function. Setting Bit 4 in the Configuration Register high outputs a least 10 ms low on this line, at the end of which Bit 4 in the Configuration Register automatically clears. Again, the label for this pin is only its suggested use. In applications where the $\overline{\text{RST}}$ capability is not needed it can be used for any type of digital control that requires a 10 ms active low open drain output.

10.0 NAND TREE TESTS

A NAND tree is provided in the LM80 for Automated Test Equipment (ATE) board level connectivity testing. If the user applies a logic zero to the $\overline{\text{NTEST_IN}}$/$\overline{\text{Reset_IN}}$ input pin, the device will be in the NAND tree test mode. A0/NTEST_OUT will become the NAND tree output pin. To perform a NAND tree test all pins included in the NAND tree should be driven to 1. Beginning with IN0 and working clockwise around the chip, each pin can be toggled and a resulting toggle can be observed on A0/NTEST_OUT. The following pins are excluded from the NAND tree test: GNDA (analog ground), GND (digital ground), V + (power supply), A0/NTEST_OUT, $\overline{\text{NTEST_IN}}$/$\overline{\text{Reset_IN}}$ and $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$. Allow for a typical propagation delay of 500 ns.

11.0 FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech

9730 Independence Ave.

Chatsworth, California 91311

818 341-3355

818 341-8207

Model Number	Frame Size	Airflow CFM
2408NL	2.36 in sq. X 0.79 in (60 mm sq. X 20 mm)	9-16
2410ML	2.36 in sq. X 0.98 in (60 mm sq. X 25 mm)	14-25
3108NL	3.15 in sq. X 0.79 in (80 mm sq. X 20 mm)	25-42
3110KL	3.15 in sq. X 0.98 in (80 mm sq. X 25 mm)	25-40

Mechatronics Inc.

P.O. Box 20

Mercer Island, WA 98040

800 453-45698

Various sizes available with tach output option.

Sanyo Denki America, Inc.

468 Amapola Ave.

Torrance, CA 90501

310 783-5400

Model Number	Frame Size	Airflow CFM
109P06XXY601	2.36 in sq. X 0.79 in (60 mm sq. X 20 mm)	11-15
109R06XXY401	2.36 in sq. X 0.98 in (60 mm sq. X 25 mm)	13-28
109P08XXY601	3.15 in sq. X 0.79 in (80 mm sq. X 20 mm)	23-30
109R08XXY401	3.15 in sq. X 0.98 in (80 mm sq. X 25 mm)	21-42

12.0 REGISTERS AND RAM

12.1 Address Register

The main register is the ADDRESS Register. The bit designations are as follows:

Bit	Name	Read/Write	Description
7-0	Address Pointer	Read/Write	Address of RAM and Registers. See the tables below for detail.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address Pointer (Power On default 00h)							
A7	A6	A5	A4	A3	A2	A1	A0

12.2 Address Pointer Index (A7–A0)

Registers and RAM	A6–A0 in Hex	Power On Value of Registers: <7:0> in Binary
Configuration Register	00h	0000 1000
Interrupt Status Register 1	01h	0000 0000
Interrupt Status Register 2	02h	0000 0000
Interrupt Mask Register 1	03h	0000 0000
Interrupt Mask Register 2	04h	0000 0000
Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$	05h	0001 0100
$\overline{\text{OS}}$ Configuration/Temperature Resolution Register	06h	0000 0001
Value RAM	20h–3Fh	

12.3 Configuration Register—Address 00h

Power on default <7:0> = 00001000 binary

Bit	Name	Read/Write	Description
0	Start	Read/Write	A one enables startup of monitoring operations, a zero puts the part in standby mode. **Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike “INT_Clear” bit.At start up, limit checking functions and scanning begin. Note, all limits should be set in the Value RAM before setting this bit HIGH.
1	$\overline{\text{INT}}$ Enable	Read/Write	A one enables the $\overline{\text{INT}}$ Interrupt output.
2	$\overline{\text{INT}}$ polarity select	Read/Write	A one selects an active high open source output while a zero selects an active low open drain output.
3	INT_Clear	Read/Write	A one disables the $\overline{\text{INT}}$ and $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
4	$\overline{\text{RESET}}$	Read/Write	A one outputs at least a 10 ms active low reset signal at $\overline{\text{RESET}}$, if <7> = 1 and <6> = 0 in the Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register. This bit is cleared once the pulse has gone inactive.
5	Chassis Clear	Read/Write	A one clears the CI (Chassis Intrusion) pin. This bit clears itself after the CI pins cleared.
6	$\overline{\text{GPO}}$	Read/Write	A one in this bit drives a one on $\overline{\text{GPO}}$ (General Purpose Output) pin.
7	INITIALIZATION	Read/Write	A one restores power on default value to the Configuration Register, Interrupt Status Registers, Interrupt Mask Registers, Fan Divisor/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$Register, and the $\overline{\text{OS}}$ Configuration/ Temperature Resolution Register. This bit clears itself since the power on default is zero.

12.4 Interrupt Status Register 1—Address 01h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	IN0	Read Only	A one indicates a High or Low limit has been exceeded.
1	IN1	Read Only	A one indicates a High or Low limit has been exceeded.
2	IN2	Read Only	A one indicates a High or Low limit has been exceeded.
3	IN3	Read Only	A one indicates a High or Low limit has been exceeded.
4	IN4	Read Only	A one indicates a High or Low limit has been exceeded.
5	IN5	Read Only	A one indicates a High or Low limit has been exceeded.
6	IN6	Read Only	A one indicates a High or Low limit has been exceeded.
7	$\overline{\text{INT_IN}}$	Read Only	A one indicates that a Low has been detected on the $\overline{\text{INT_IN}}$.

12.5 Interrupt Status Register 2—Address 02h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	Hot Temperature	Read Only	A one indicates a High or Low limit has been exceeded. Only “One-Time Interrupt” and “Default Interrupt” modes are supported. The mode is set by bit-6 of the Interrupt Mask Register 2.
1	$\overline{\text{BTI}}$	Read Only	A one indicates that an interrupt has occurred from the Board Temperature Interrupt ($\overline{\text{BTI}}$) input pin. $\overline{\text{BTI}}$ can be tied to the OS output of multiple LM75 chips.
2	FAN1	Read Only	A one indicates that a fan count limit has been exceeded.
3	FAN2	Read Only	A one indicates that a fan count limit has been exceeded.
4	CI (Chassis Intrusion)	Read Only	A one indicates CI (Chassis Intrusion) has gone high.
5	$\overline{\text{OS}}$ bit	Read Only	A one indicates a High or a Low $\overline{\text{OS}}$ Temperature limit has been exceed. Only “One-Time Interrupt” and “Default Interrupt” modes are supported (see Sections 7.2 and 8.2). The mode is set by bit-7 of the Interrupt Mask Register 2.
6	Reserved	Read Only	
7	Reserved	Read Only	

12.6 Interrupt Mask Register 1—Address 03h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	IN0	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	IN1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	IN2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
3	IN3	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
4	IN4	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	IN5	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	IN6	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
7	$\overline{\text{INT_IN}}$	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.

12.7 Interrupt Mask Register 2—Address 04h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	Hot Temperature	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	$\overline{\text{BTI}}$	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	FAN1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
3	FAN2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
4	CI (Chassis Intrusion)	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	$\overline{\text{OS}}$ bit	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	Hot Temperature Interrupt mode select	Read/Write	A zero selects the default interrupt mode which gives the user an interrupt if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the hysteresis limit. A one selects the one time interrupt mode which only gives the user one interrupt when it goes above the hot limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature goes below the hysteresis limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the hot limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done. (See *Figure 10* in Section 7.0)
7	$\overline{\text{OS}}$ bit Interrupt mode select	Read/Write	A zero selects the default interrupt mode which gives the user an interrupt if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the hysteresis limit. A one selects the one time interrupt mode which only gives the user one interrupt when it goes above the hot limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature goes below the hysteresis limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the hot limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done. (See Section*Figure 10* Section 7.0)

12.8 Fan Divisor Register/$\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$—Address 05h

Power on – <7:4> is 0101, and <3:0>is mapped to VID <3:0>

Bit	Name	Read/Write	Description
0	FAN1 Mode Select	Read/Write	A one selects the level sensitive input mode while a zero selects Fan count mode for the FAN1 input pin.
1	FAN2 Mode Select	Read/Write	A one selects the level sensitive input mode while a zero selects Fan count mode for the FAN2 input pin.
2-3	FAN1 RPM Control	Read/Write	FAN1 Speed Control. <3:2> = 00 - divide by 1; <3:2> = 01 - divide by 2; <3:2> = 10 - divide by 4; <3:2> = 11 - divide by 8. If level sensitive input is selected: >2< = 1 selects and active-low input (An interrupt will be generated if the FAN2 input is Low), >2< = 0 selects an active-high input (an interrupt will be generated if the FAN2 input is High).
4-5	FAN2 RPM Control	Read/Write	FAN2 Speed Control. <5:4> = 00 - divide by 1; <5:4> = 01 - divide by 2; <5:4> = 10 - divide by 4; <5:4> = 11 - divide by 8. If level sensitive input is selected: <2> = 1 selects and active-low input (An interrupt will be generated if the FAN2 input is Low), <2> = 0 selects an active-high input (an interrupt will be generated if the FAN2 input is High).
6	$\overline{\text{OS}}$ pin enable	Read/Write	A one enables $\overline{\text{OS}}$ mode on the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ output pin, while Bit 7 of this register is set to zero. If bits 6 and 7 of this register are set to zero the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin is disabled.
7	$\overline{\text{RST}}$ enable	Read/Write	A one sets the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin in the $\overline{\text{RST}}$ mode. In the $\overline{\text{RST}}$ mode, bit 7 of the Fan Divisor/ $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ Register has to be set to one. If bits 6 and 7 of this register are set to zero the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin is disabled.

12.9 $\overline{\text{OS}}$ Configuration/Temperature Resolution Register —Address 06h

Power on default Serial Bus address <7:0> = 0000 0001 binary

Bit	Name	Read/Write	Description
0	$\overline{\text{OS}}$ status	Read only	Status of the $\overline{\text{OS}}$.This bit mirrors the state of the $\overline{\text{RST_OUT}}$/$\overline{\text{OS}}$ pin when in the $\overline{\text{OS}}$ mode.
1	$\overline{\text{OS}}$ Polarity	Read/Write	A zero selects $\overline{\text{OS}}$ to be active-low, while a one selects $\overline{\text{OS}}$ to be active high. $\overline{\text{OS}}$ is an open-drain output.
2	$\overline{\text{OS}}$ mode select	Read/Write	A one selects the one time interrupt mode for $\overline{\text{OS}}$, while a zero selects comparator mode for $\overline{\text{OS}}$. (See in Section 7.0)
3	Temperature Resolution Control	Read/Write	A zero selects the default 8-bit plus sign resolution temperature conversions while a one selects 11-bit plus sign resolution temperature conversions. 8-bit plus sign conversions time is approximately 100 ms, while 11-bit plus sign conversion time is approximately 2 seconds.
4-7	Temp [3:0]	Read/Write	The lower nibble (4 LSBs) of the 11-bit plus sign temperature data. <4> = Temp [0] (nibble LSB, 0.0625°C), <5> = Temp [1], <6> = Temp [2], <7> = Temp 3 (nibble MSB, 0.5°C). For 8-bit plus sign temperature resolution, <7> = Temp [0] (LSB, 0.5°C) while <4:6> are undefined.

12.10 Value RAM—Address 20h–3Fh

Address A7–A0	Description
20h	IN0 reading
21h	IN1 reading
22h	IN2 reading
23h	IN3 reading
24h	IN4 reading
25h	IN5 reading
26h	IN6 reading
27h	Temperature reading
28h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	IN0 High Limit
2Bh	IN0 Low Limit
2Ch	IN1 High Limit
2Dh	IN1 Low Limit
2Eh	IN2 High Limit
2Fh	IN2 Low Limit
30h	IN3 High Limit
31h	IN3 Low Limit
32h	IN4 High Limit
33h	IN4 Low Limit
34h	IN5 High Limit
35h	IN5 Low Limit
36h	IN6 High Limit
37h	IN6 Low Limit
38h	Hot Temperature Limit (High)
39h	Hot Temperature Hysteresis Limit (Low)
3Ah	$\overline{OS}$ Temperature Limit (High)
3Bh	$\overline{OS}$ Temperature Hysteresis Limit (Low)
3Ch	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Eh-3Fh	Reserved

Note: Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will **never** be generated except the case when voltages go below the low limits.

For voltage input high limits, the device is doing a greater than comparison. For low limits, however, it is doing a less than or equal to comparison.

Typical Application

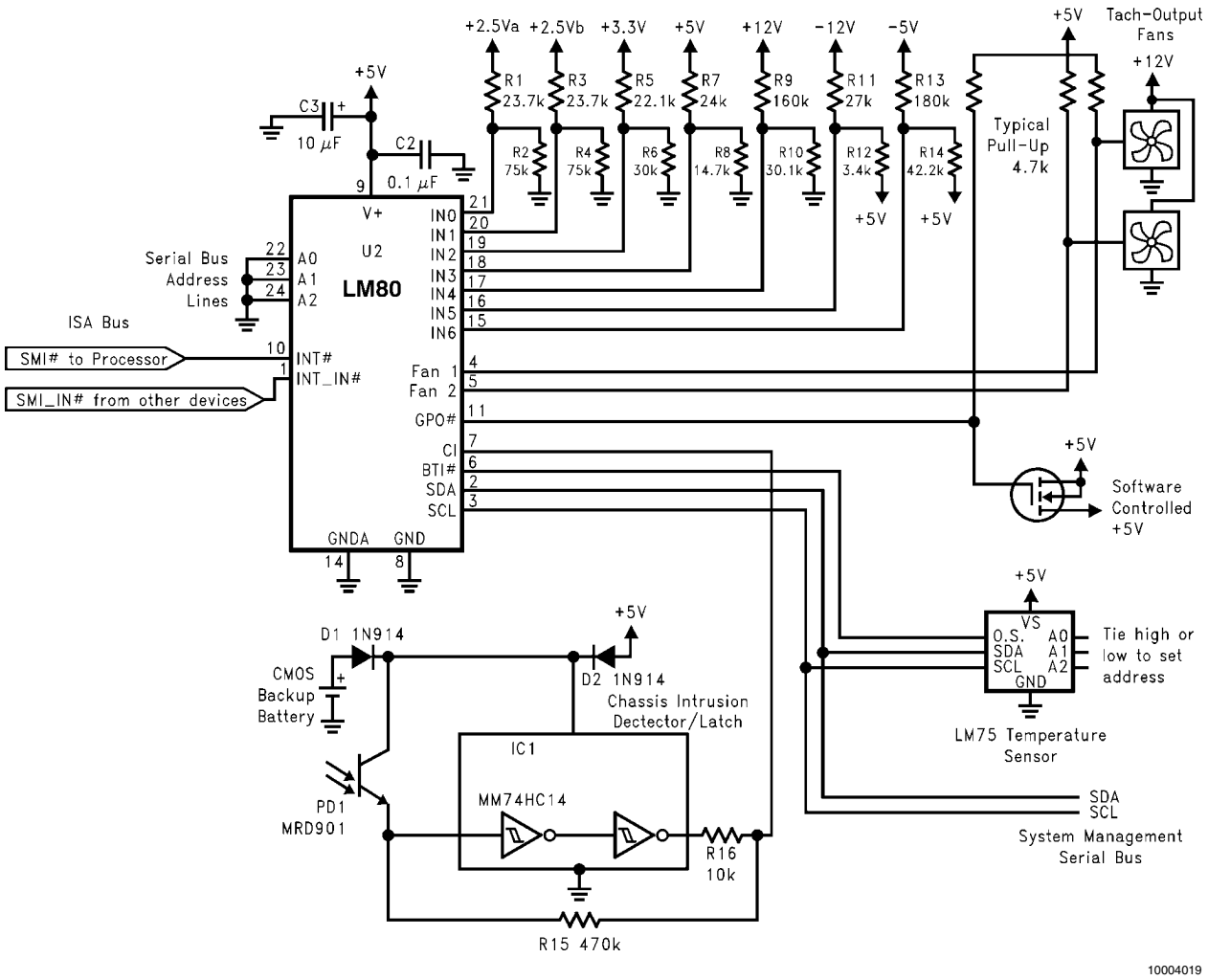
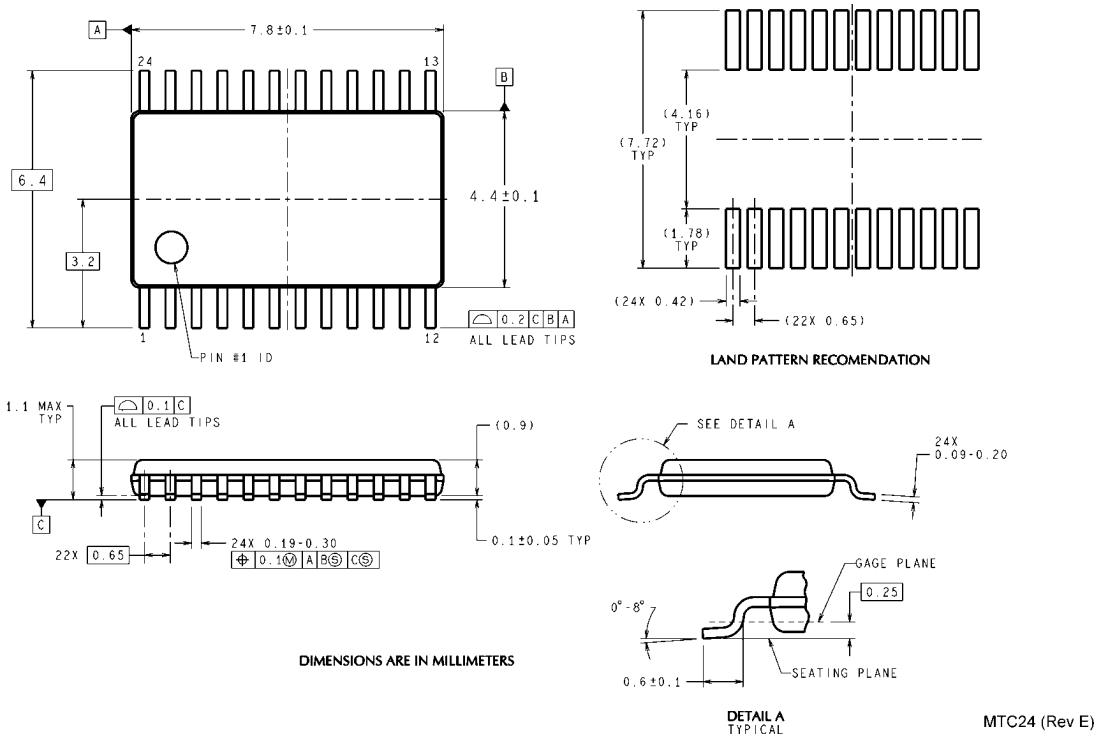


FIGURE 11. In this PC application the LM80 monitors temperature, fan speed for 2 fans, and 7 power supply voltages. It also monitors an optical chassis intrusion detector.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Molded Plastic TSSOP
Order Number LM80CIMT-3, LM80CIMTX-3, LM80CIMTX-5 or LM80CIMT-5
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Notes

Notes

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LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
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