

LP5907 Ultra Low-Noise, 250-mA Linear Regulator for RF and Analog Circuits - Requires No Bypass Capacitor

1 Features

- Input Voltage Range: 2.2 V to 5.5 V
- Output Voltage Range: 1.2 V to 4.5 V
- Output Current: 250 mA
- Stable with 1- μ F Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Remote Output Capacitor Placement
- Thermal-Overload and Short-Circuit Protection
- -40°C to 125°C Junction Temperature Range for Operation
- Low Output Voltage Noise: $< 10 \mu\text{V}_{\text{RMS}}$
- PSRR: 82 dB at 1 kHz
- Output Voltage Tolerance: $\pm 2\%$
- Virtually Zero IQ (Disabled): $< 1 \mu\text{A}$
- Very Low I_{Q} (Enabled): $12 \mu\text{A}$
- Start-up Time: 80 μs
- Low Dropout: 120 mV (typical)

2 Applications

- Cellular Phones
- PDA Handsets
- Wireless LAN Devices

3 Description

The LP5907 is a linear regulator capable of supplying 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

The device is designed to work with a 1- μ F input and a 1- μ F output ceramic capacitor (no separate noise bypass capacitor is required).

This device is available with fixed output voltages from 1.20 V to 4.50 V in 25-mV steps. Contact Texas Instruments Sales for specific voltage option needs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
LP5907	DSBGA (4)	0.675 mm x 0.675 mm (MAX)
	SOT-23 (5)	2.90 mm x 1.60 mm (NOM)
	X2SON (4)	1.00 mm x 1.00 mm (NOM)

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

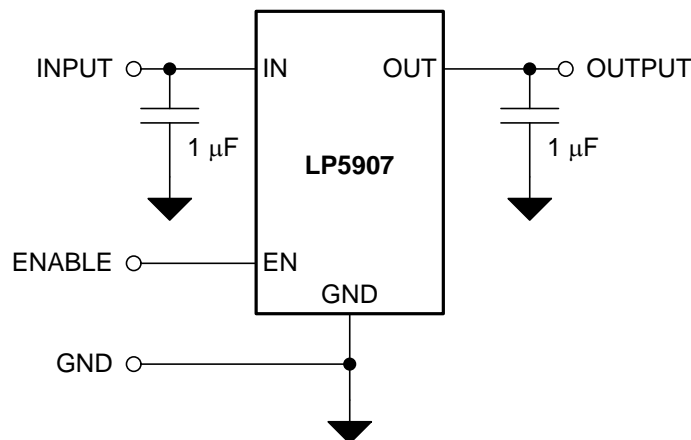


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4 Revision History

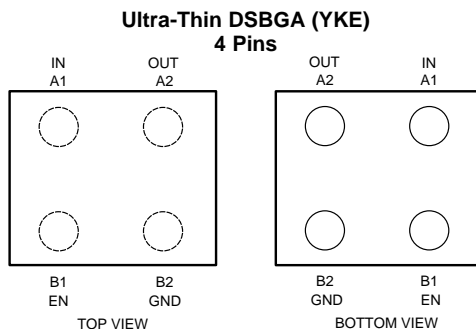
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (October 2013) to Revision H

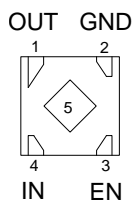
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- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section **1**

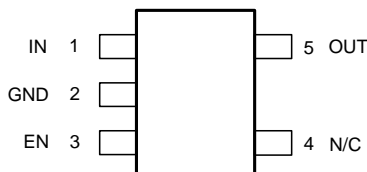
5 Pin Configuration and Functions



X2SON (DQN)
4 Pins
Bottom View



SOT-23 (DBV)
5 Pins
Top View



Pin Functions

NAME	PIN			I/O	DESCRIPTION
	DSBGA NUMBER	X2SON NUMBER	SOT-23 NUMBER		
IN	A1	4	1	I	Input voltage supply. A 1- μ F capacitor should be connected at this input.
OUT	A2	1	5	O	Regulated output voltage. A minimum 1- μ F low-ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 230- Ω (typical) pull-down resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
EN	B1	3	3	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 230- Ω pull-down resistor. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 1M- Ω pull-down resistor to hold the regulator off by default.
GND	B2	2	2	—	Common ground
N/C	N/A	N/A	4	—	No internal electrical connection.
Thermal Pad	N/A	5	N/A	—	Thermal pad for X2SON package, connect to GND or leave floating. Do not connect to any potential other than GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	-0.3	6	V
V _{OUT}	Output voltage	-0.3 to (V _{IN} + 0.3 V)	6	
V _{EN}	Enable input voltage	-0.3 to (V _{IN} + 0.3 V)	6	
	Continuous power dissipation ⁽⁴⁾	Internally Limited		W
T _{JMAX}	Junction temperature			150 °C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military or Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) All voltages are with respect to the GND pin.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 Handling Ratings

		MIN	MAX	UNIT	
T _{stg}	Storage temperature range	-65	150	°C	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	-2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	-1000	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{IN}	Input supply voltage	2.2	5.5	V
V _{EN}	Enable input voltage	0 to (V _{IN} + 0.3)	5.5	
I _{OUT}	Output current	0	250	mA
T _J	Junction temperature	-40	125	°C
T _A	Ambient temperature ⁽³⁾	-40	85	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}). See [Application Information](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP5907			UNIT
		SOT-23 (DBV)	X2SON (DQN)	DSBGA (YKE)	
		5 PINS	4 PINS	4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	193.4	216.1	206.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	102.1	161.7	1.5	
R _{θJB}	Junction-to-board thermal resistance	45.8	162.1	37.0	
ψ _{JT}	Junction-to-top characterization parameter	8.4	5.1	15.0	
ψ _{JB}	Junction-to-board characterization parameter	45.3	161.7	36.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

V_{IN} = V_{OUT(NOM)} + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 1 μF, unless otherwise stated.⁽¹⁾⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage	T _A = 25°C	2.2		5.5	V
ΔV _{OUT}	Output voltage tolerance	V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} ≥ 1.8 V	-2		2	%V _{OUT}
		V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} < 1.8 V	-3		3	
	Line regulation	V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA		0.02		%/V
	Load regulation	I _{OUT} = 1 mA to 250 mA		0.001		%/mA
I _{LOAD}	Load current	See ⁽⁴⁾	0		250	mA
	Maximum output current		250			
I _Q	Quiescent current ⁽⁵⁾	V _{EN} = 1.2 V, I _{OUT} = 0 mA		12	25	μA
		V _{EN} = 1.2 V, I _{OUT} = 250 mA		250	425	
		V _{EN} = 0.3 V (Disabled)		0.2	1	
I _G	Ground current ⁽⁶⁾	V _{EN} = 1.2 V, I _{OUT} = 0 mA		14		μA
V _{DO}	Dropout voltage ⁽⁷⁾	I _{OUT} = 100 mA		50		mV
		I _{OUT} = 250 mA (DSBGA)		120	200	
		I _{OUT} = 250 mA (SOT-23, X2SON packages)			250	
I _{SC}	Short circuit current limit	T _A = 25°C ⁽⁸⁾	250	500		mA
PSRR	Power supply rejection ratio ⁽⁹⁾	f = 100 Hz, I _{OUT} = 20 mA		90		dB
		f = 1 kHz, I _{OUT} = 20 mA		82		
		f = 10 kHz, I _{OUT} = 20 mA		65		
		f = 100 kHz, I _{OUT} = 20 mA		60		

(1) All voltages are with respect to the device GND terminal, unless otherwise stated.

(2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of -40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.

(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} - (R_{θJA} × P_{D-MAX}). See [Applications and Implementation](#).

(4) The device maintains a stable, regulated output voltage without a load current.

(5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.

(6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.

(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

(8) Short-circuit current (I_{SC}) for the LP5907 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.

(9) This specification is verified by design.

Electrical Characteristics (continued)

 $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise stated.⁽¹⁾⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
e_N	Output noise voltage ⁽⁹⁾	BW = 10 Hz to 100 kHz	$I_{OUT} = 1\text{ mA}$	10			μV_{RMS}
			$I_{OUT} = 250\text{ mA}$	6.5			
R_{AD}	Output Automatic Discharge pull-down resistance	$V_{EN} < V_{IL}$ (output disabled)		230			Ω
T_{SD}	Thermal shutdown	T_J rising		160			$^{\circ}\text{C}$
	Thermal hysteresis	T_J falling from shutdown		15			
LOGIC INPUT THRESHOLDS							
V_{IL}	Low input threshold	$V_{IN} = 2.2\text{ V to } 5.5\text{ V}$ V_{EN} falling until the output is disabled		0.4			V
V_{IH}	High input threshold	$V_{IN} = 2.2\text{ V to } 5.5\text{ V}$ V_{EN} rising until the output is enabled		1.2			V
I_{EN}	Input current at EN pin ⁽¹⁰⁾	$V_{EN} = 5.5\text{ V and } V_{IN} = 5.5\text{ V}$		5.5			μA
		$V_{EN} = 0\text{ V and } V_{IN} = 5.5\text{ V}$		0.001			
TRANSIENT CHARACTERISTICS							
ΔV_{OUT}	Line transient ⁽⁹⁾	$V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in 30 μs		-1			mV
		$V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in 30 μs		1			
	Load transient ⁽⁹⁾	$I_{OUT} = 1\text{ mA to } 250\text{ mA}$ in 10 μs		-40			mV
		$I_{OUT} = 250\text{ mA to } 1\text{ mA}$ in 10 μs		40			
	Overshoot on start-up ⁽⁹⁾	Stated as a percentage of $V_{OUT(NOM)}$		5%			
t_{ON}	Turnon time	From $V_{EN} > V_{IH}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$ $T_A = 25^{\circ}\text{C}$		80	150		μs

(10) There is a 1-M Ω resistor between EN and ground on the device.

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX	UNIT
C_{IN}	Input capacitance ⁽²⁾	Capacitance for stability	0.7	1		μF
C_{OUT}	Output capacitance ⁽²⁾		0.7	1	10	
ESR	Output/Input capacitance ⁽²⁾		5		500	m Ω

(1) The minimum capacitance should be greater than 0.5 μF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

(2) This specification is verified by design.

6.7 Typical Characteristics

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

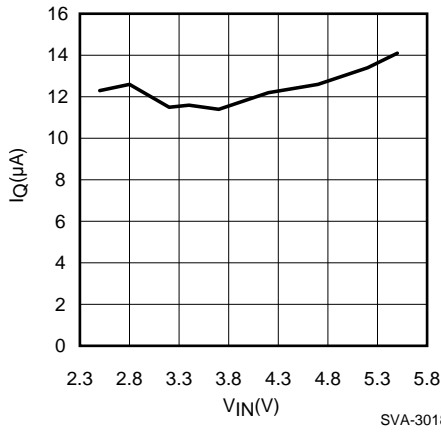


Figure 1. Quiescent Current vs Input Voltage

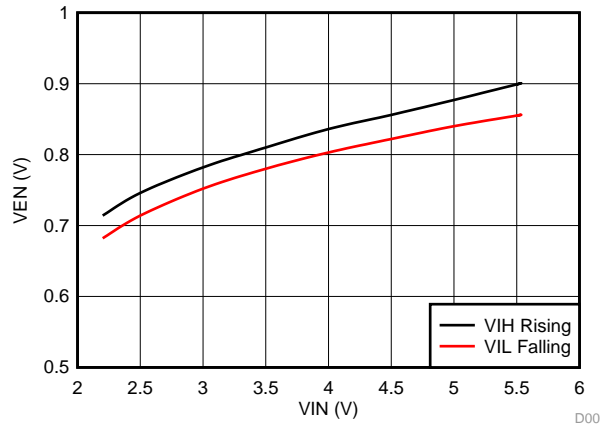


Figure 2. V_{EN} Thresholds vs V_{IN}

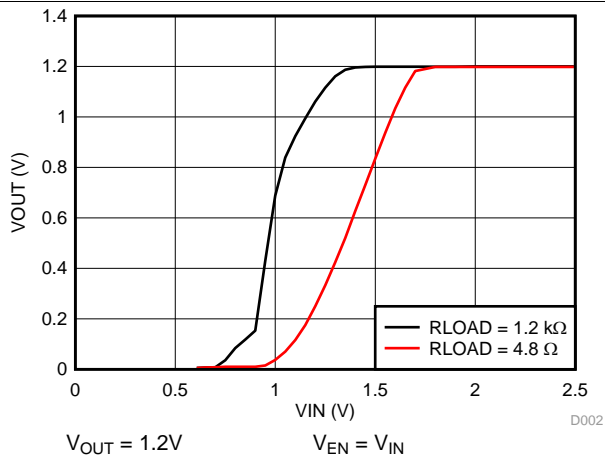


Figure 3. V_{OUT} vs V_{IN}

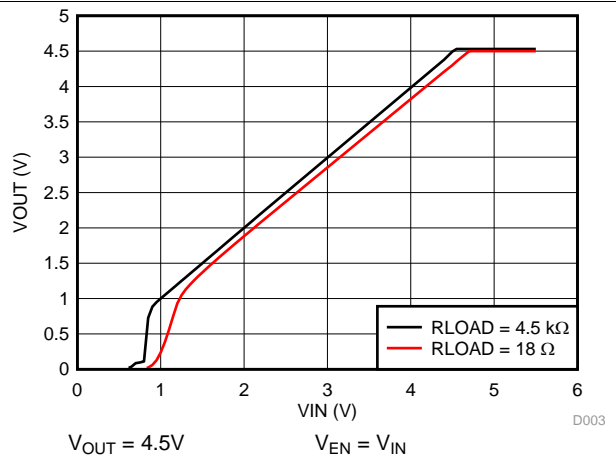


Figure 4. V_{OUT} vs V_{IN}

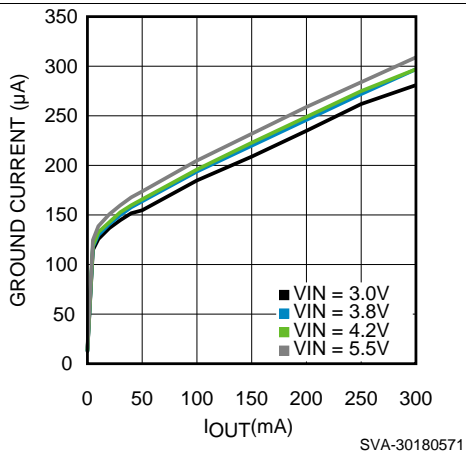


Figure 5. Ground Current vs Output Current

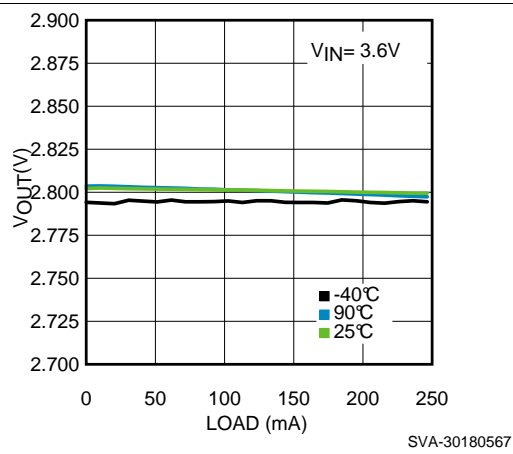


Figure 6. Load Regulation

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

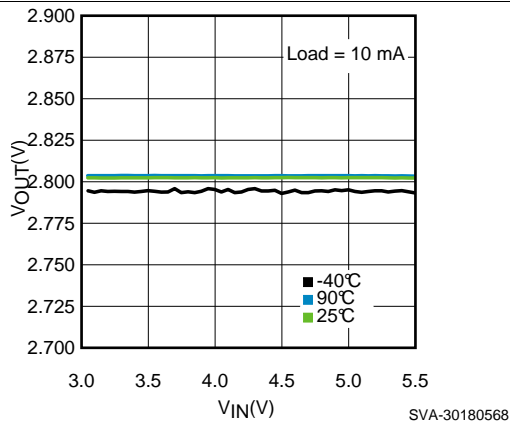


Figure 7. Line Regulation

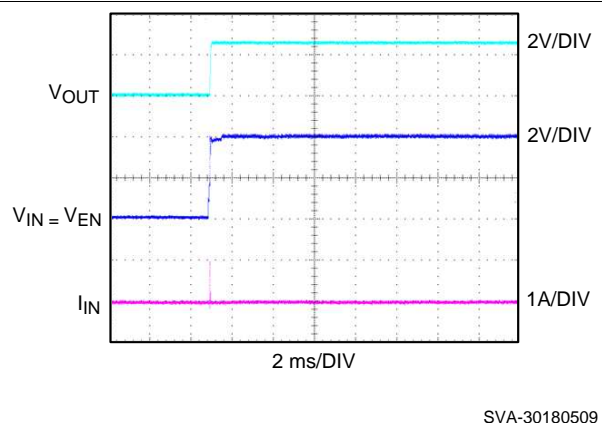


Figure 8. Inrush Current

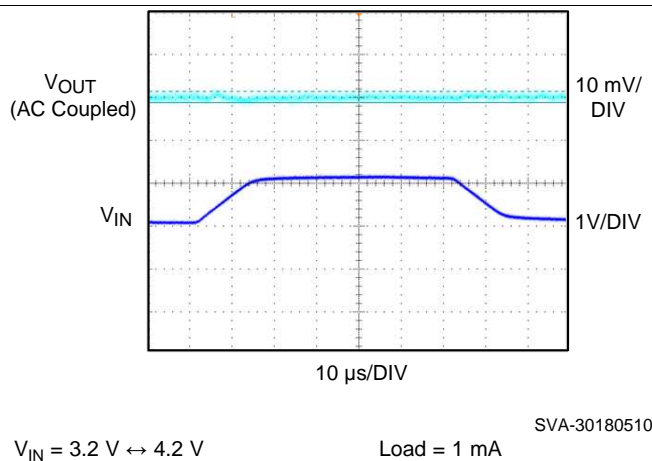


Figure 9. Line Transient

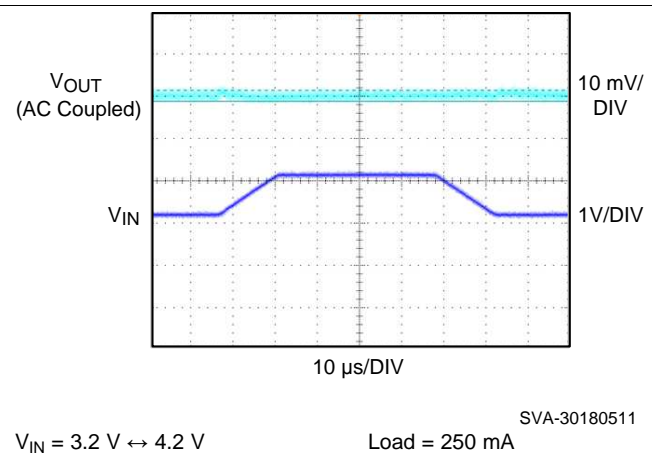


Figure 10. Line Transient

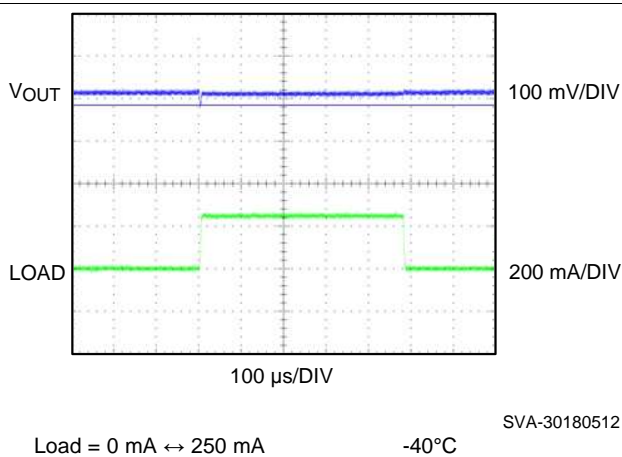


Figure 11. Load Transient

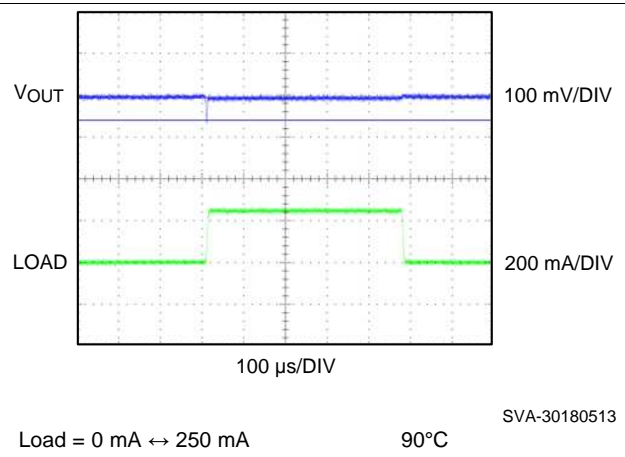
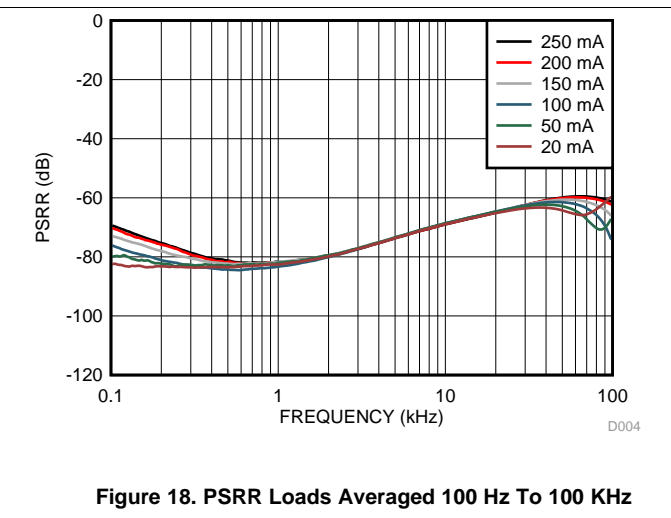
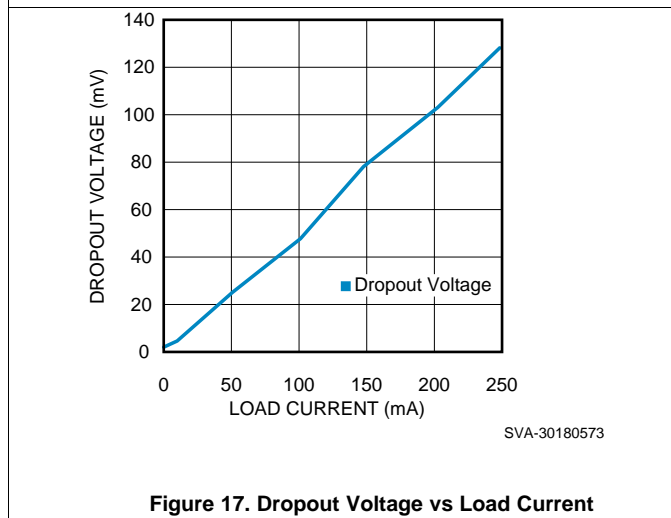
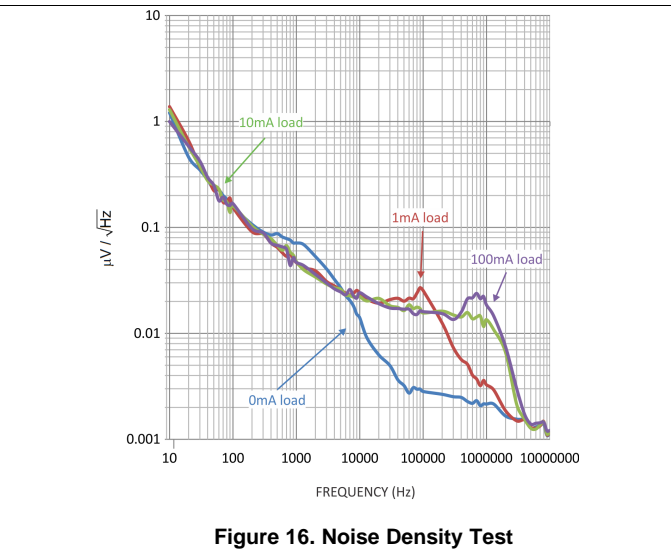
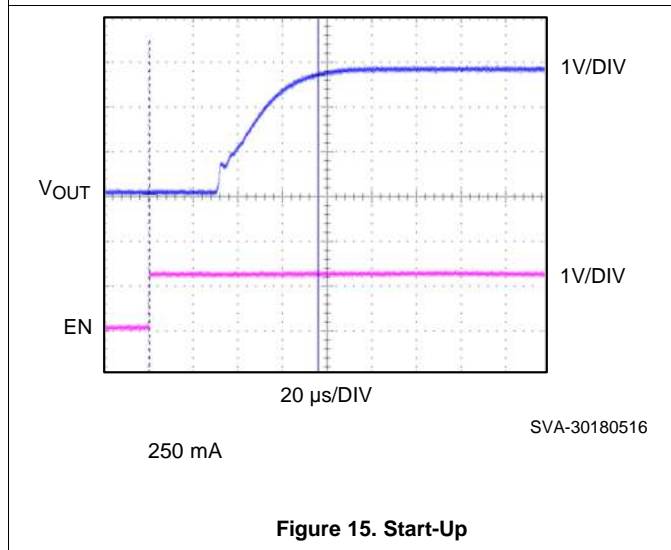
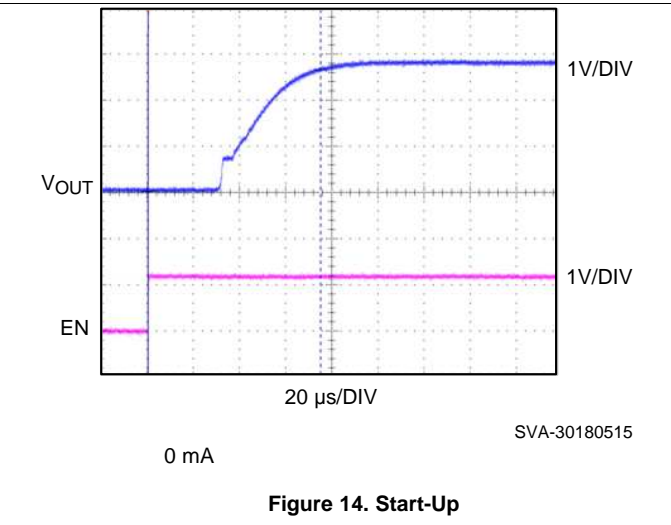
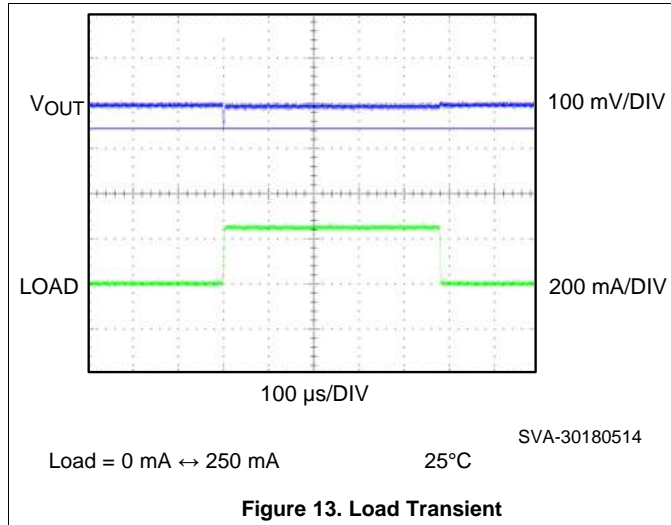


Figure 12. Load Transient

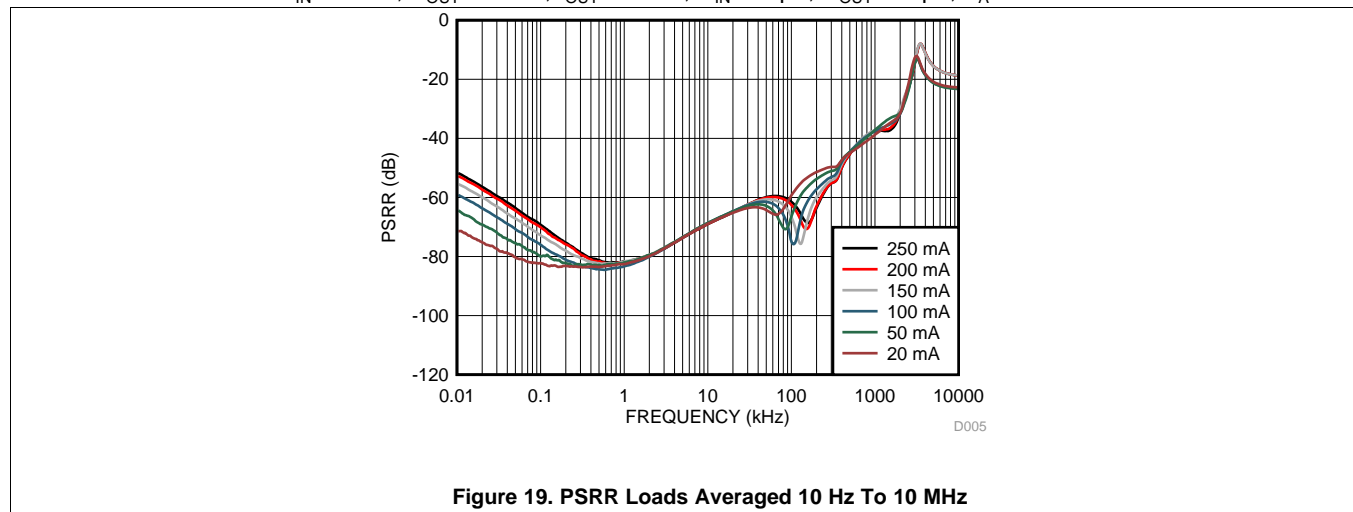
Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$



Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$



Feature Description (continued)

7.3.3 Output Automatic Discharge

The LP5907 output employs an internal 230- Ω (typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.4 Remote Output Capacitor Placement

The LP5907 requires at least a 1- μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

7.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5907 Enable (EN) pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230- Ω (typical) pull-down resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907 does not include any dedicated UVLO circuitry. The LP5907 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or ($V_{OUT} + V_{DO}$).

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5907 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 μ F. The LP5907 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of -40°C to 125°C .

8.2 Typical Application

Figure 20 shows the typical application circuit for the LP5907. Input and output capacitances may need to be increased above the 1 μ F minimum for some applications.

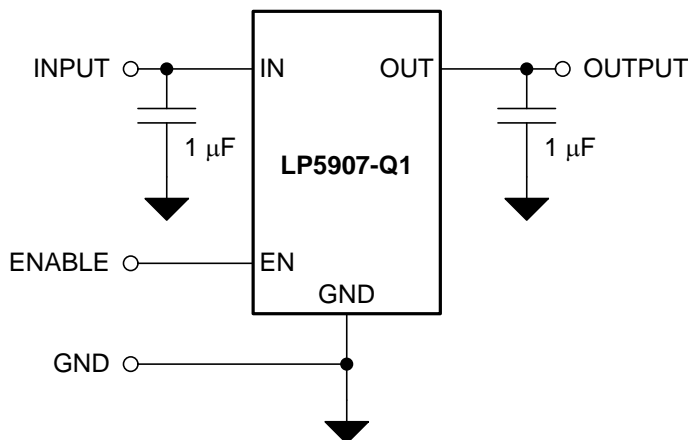


Figure 20. LP5907 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 V to 5.5 V
Output voltage	1.8 V
Output current	200 mA
Output capacitor range	0.7 μ F to 10 μ F
Input/Output capacitor ESR range	5 to 500 m Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using [Equation 1](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \tag{1}$$

The actual power being dissipated in the device can be represented by [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be derated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by [Equation 3](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (3)$$

Alternately, if T_{A-MAX} can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the ' $V_{IN} - V_{OUT}$ ' term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

Like most low-dropout regulators, the LP5907 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1 μF capacitor has to be connected between the LP5907 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1 μF .

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907, then it is recommended to increase the input capacitor to at least 10 μF . Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

8.2.2.4 Output Capacitor

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1 μF . A ceramic capacitor (dielectric types X5R or X7R) in the 1 μF to 10 μF range, and with ESR between 5 m Ω to 500 m Ω , is suitable in the LP5907 application circuit. For this device the output capacitor should be connected between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT} , but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 m Ω to 500 m Ω for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

8.2.2.5 Capacitor Characteristics

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 μF to 10 μF , ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 μF ceramic capacitor is in the range of 20 m Ω to 40 m Ω , which easily meets the ESR requirement for stability for the LP5907.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within $\pm 15\%$ over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 μF to 10 μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.6 Remote Capacitor Operation

The LP5907 requires at least a 1 μF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

8.2.2.7 No-Load Stability

The LP5907 remains stable, and in regulation, with no external load.

8.2.2.8 Enable Control

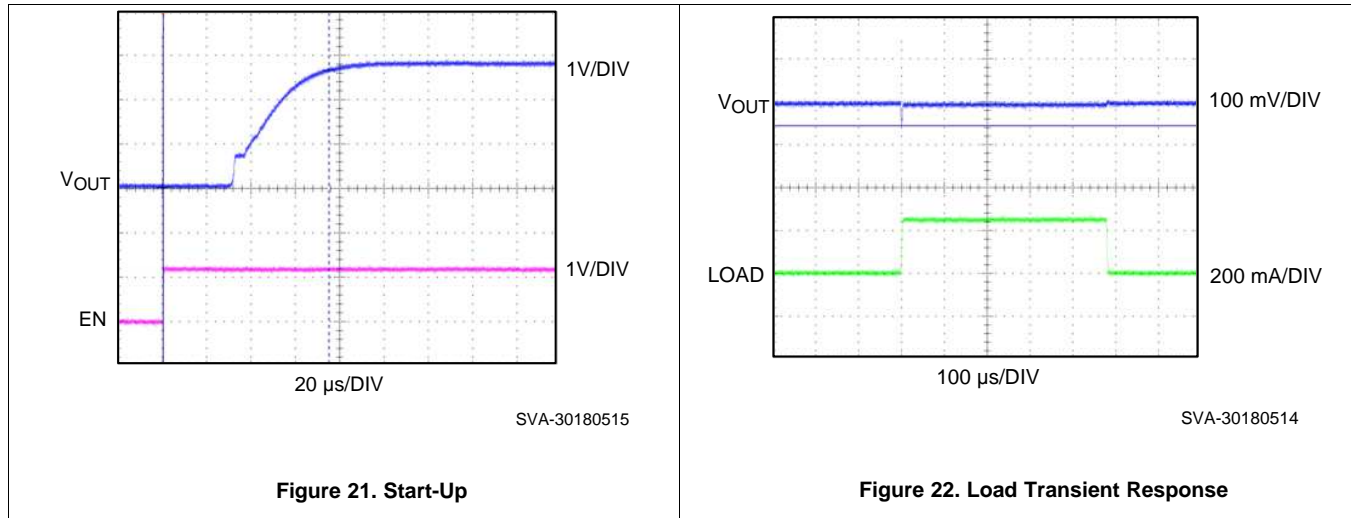
The LP5907 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 μA . Additionally, an output pull-down circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-M Ω pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the [Electrical Characteristics](#) under V_{IL} and V_{IH} .

8.2.3 Application Curves



9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5907 output voltage is well regulated and dynamic performance is optimum, the input supply should be at least $V_{OUT} + 1$ V. A minimum capacitor value of 1 μF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5907 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5907.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP5907 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Examples

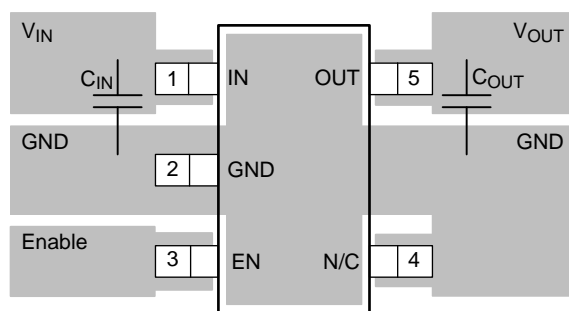


Figure 23. LP5907MF-x.x (SOT-23) Typical Layout

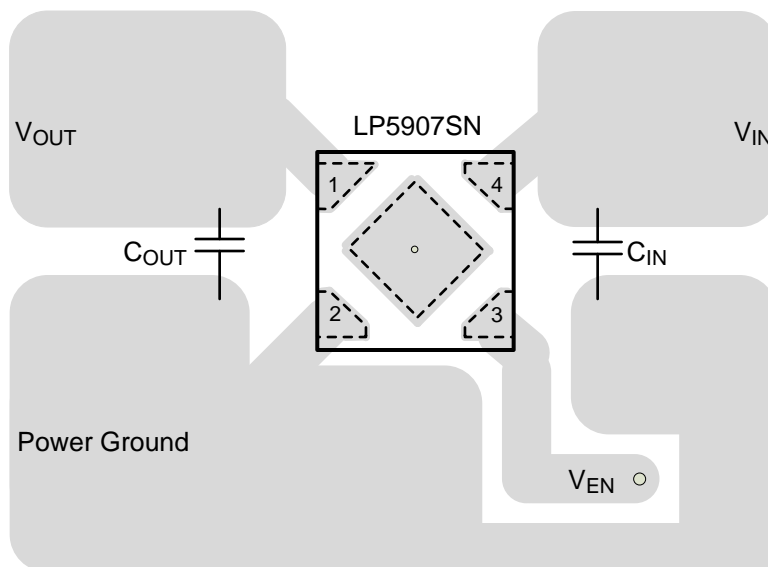


Figure 24. LP5907SN-xx (X2SON) Typical Layout

Layout Examples (continued)

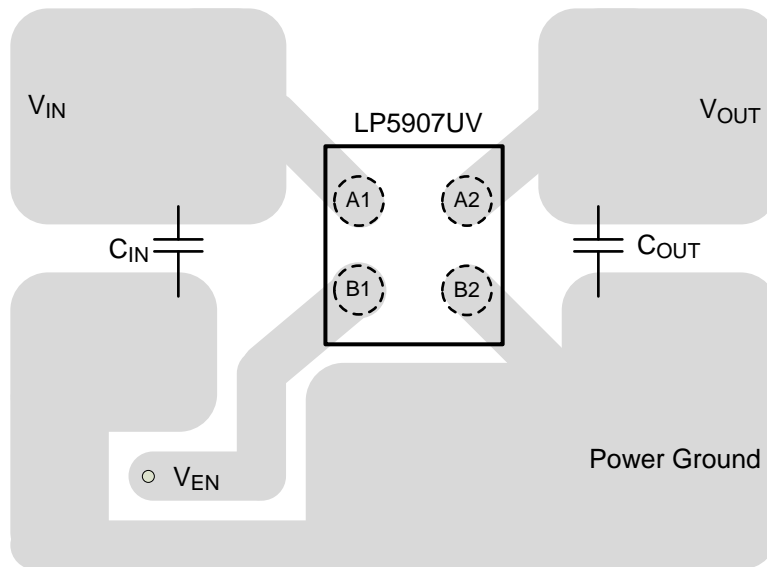


Figure 25. LP5907UV-x.x (DSBGA) Typical Layout

10.3 X2SON Mounting

The X2SON package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance. For more information, see the Application Report *QFN/SON PCB Attachment* ([SLUA271](#)).

10.4 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112, *DSBGA Wafer Level Chip Scale Package* ([SNVA009](#)). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.5 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* ([SNVA009](#)).

Texas Instruments Application Note *QFN/SON PCB Attachment* ([SLUA271](#))

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

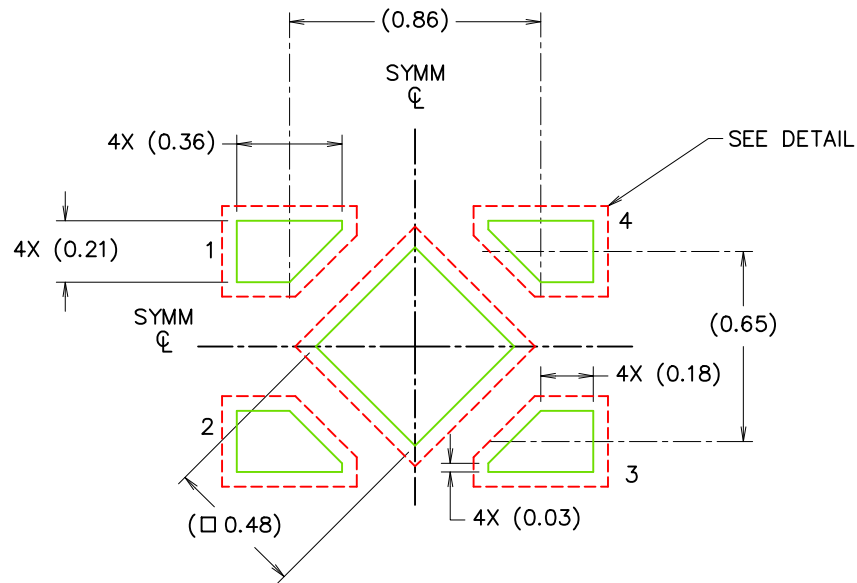
11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

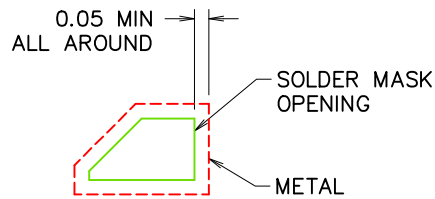
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



LAND PATTERN EXAMPLE
SCALE: 40X



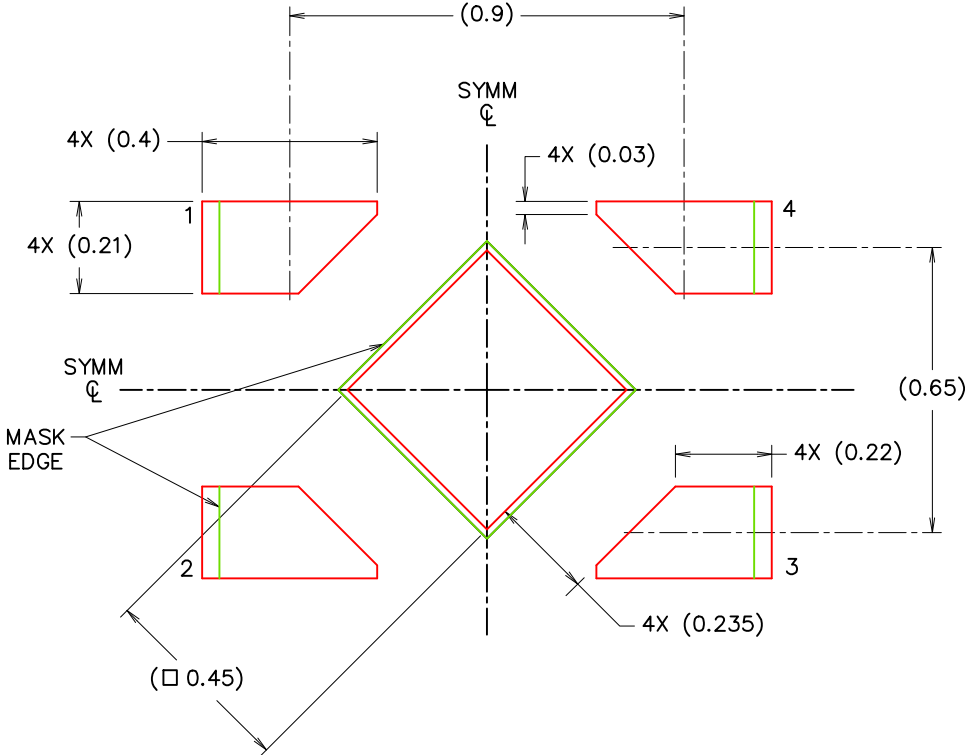
SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4215302/B 05/2014

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271) .



SOLDER PASTE EXAMPLE
 BASED ON 0.1mm THICK STENCIL
 EXPOSED PAD
 88% PRINTED SOLDER COVERAGE BY AREA
 SCALE: 60X

4215302/B 05/2014

NOTES: (continued)

- 5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907MFX-1.2	ACTIVE					TBD	Call TI	Call TI	-40 to 125		Samples
LP5907MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLTB	Samples
LP5907MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN8B	Samples
LP5907MFX-1.8	ACTIVE			5		TBD	Call TI	Call TI	-40 to 125		Samples
LP5907MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLUB	Samples
LP5907MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN7B	Samples
LP5907MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLYB	Samples
LP5907MFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN4B	Samples
LP5907MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLZB	Samples
LP5907MFX-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN5B	Samples
LP5907MFX-3.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN6B	Samples
LP5907MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLVB	Samples
LP5907MFX-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLXB	Samples
LP5907SNX-1.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF	Samples
LP5907SNX-1.8/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CG	Samples
LP5907SNX-2.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EP	Samples
LP5907SNX-2.5/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	F9	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907SNX-2.7/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH	Samples
LP5907SNX-2.75	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		
LP5907SNX-2.8/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
LP5907SNX-2.85/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
LP5907SNX-2.9/NOPB	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GV	
LP5907SNX-3.0/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
LP5907SNX-3.1/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
LP5907SNX-3.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM	Samples
LP5907SNX-3.3/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CN	Samples
LP5907SNX-4.0/NOPB	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GU	
LP5907SNX-4.5/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CO	Samples
LP5907UVE-1.2/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVE-1.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVE-2.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVE-2.85/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVE-3.0/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVE-3.1/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVE-3.2/NOPB	PREVIEW	DSBGA	YKE	4		Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907UVE-3.3/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVE-4.5/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX-1.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVX-1.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	Call TI SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVX-2.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
LP5907UVX-2.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVX-2.85/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	Call TI SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVX-3.0/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVX-3.1/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVX-3.2/NOPB	PREVIEW	DSBGA	YKE	4		Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	
LP5907UVX-3.3/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVX-4.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX19/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5907UVX37/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP5907 :

- Automotive: [LP5907-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	0	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.7	0.7	0.48	4.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.7	0.7	0.48	4.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	0	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.7	0.7	0.48	4.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

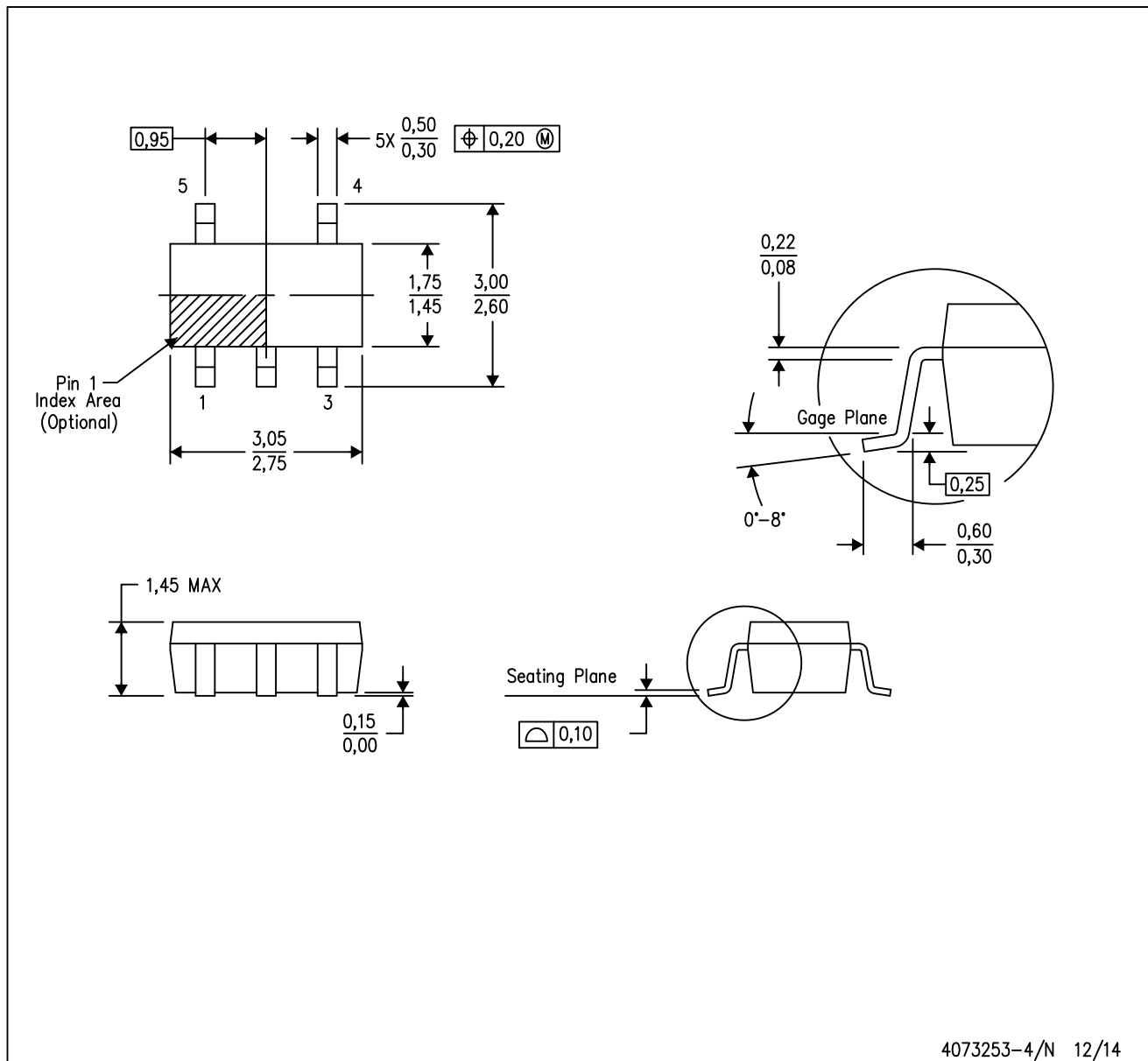

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	0	210.0	185.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	0	210.0	185.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

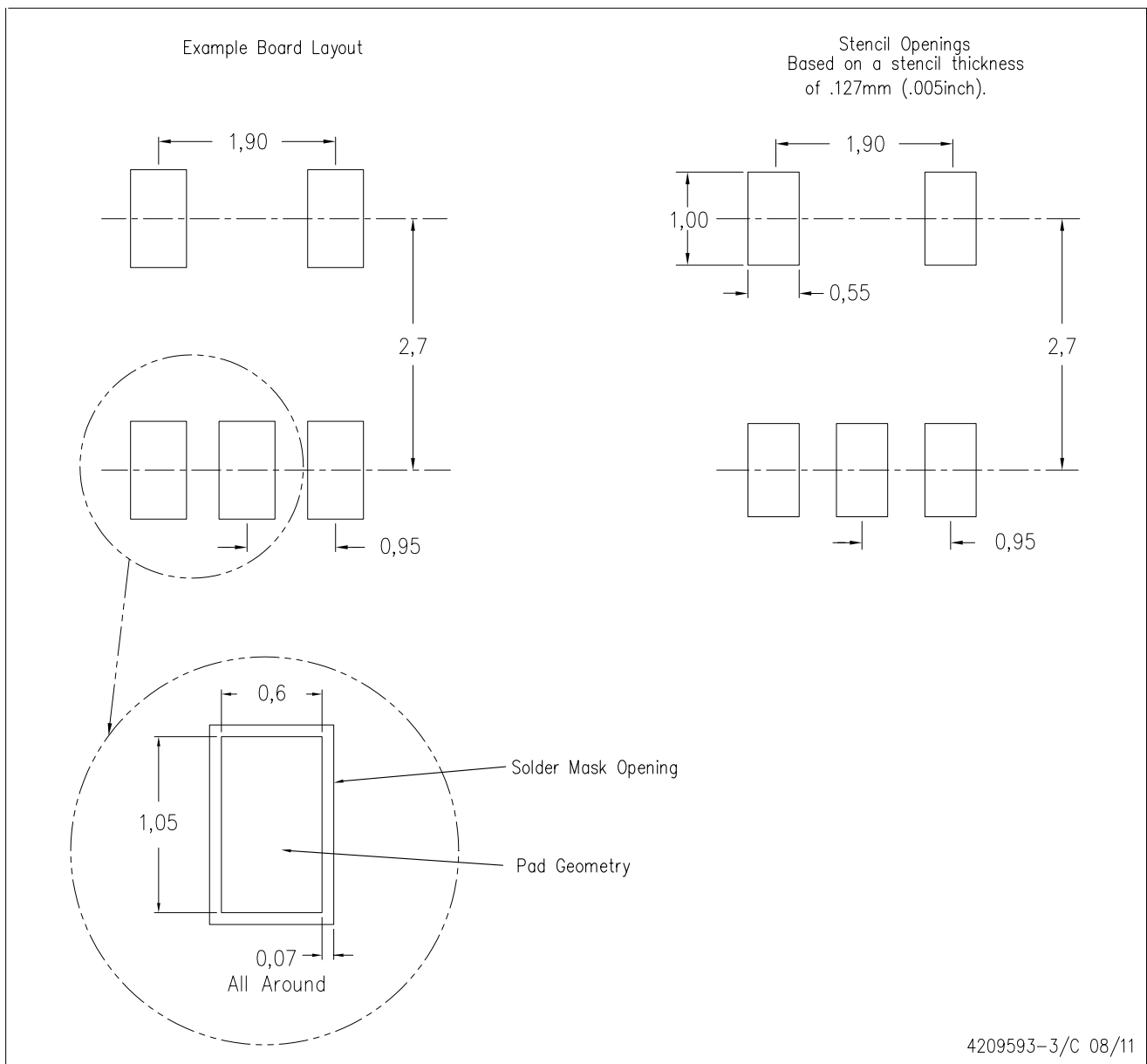
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

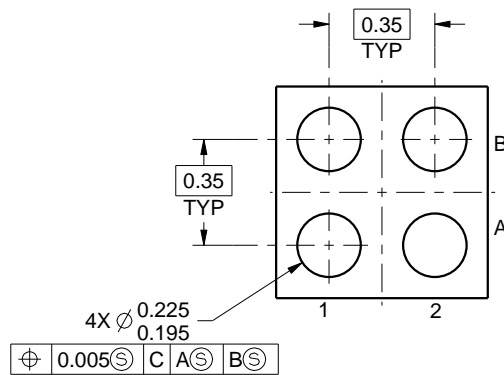
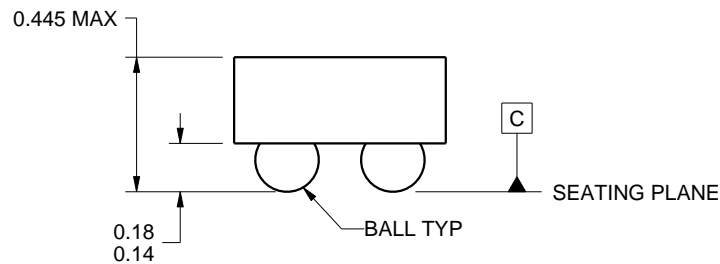
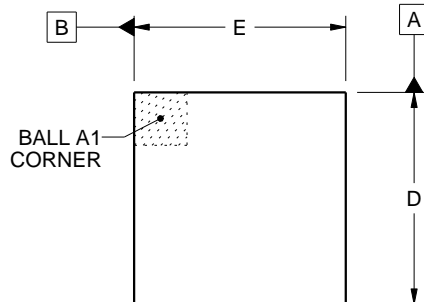


YKE0004

PACKAGE OUTLINE

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 0.675 mm, Min = 0.615 mm
E: Max = 0.675 mm, Min = 0.615 mm

4220102/A 11/2014

NOTES:

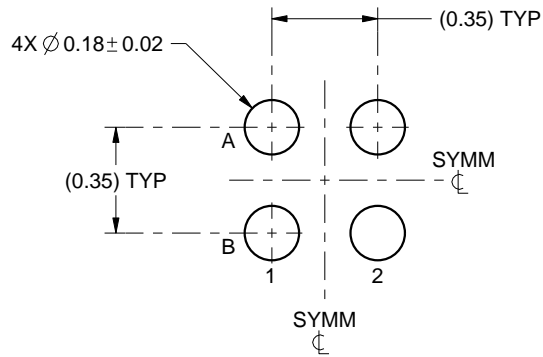
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

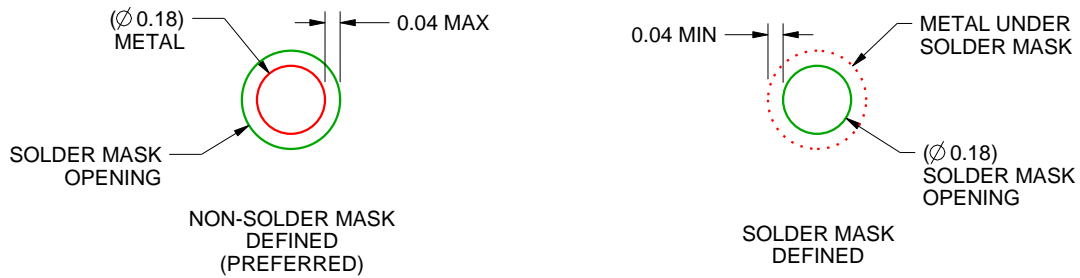
YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

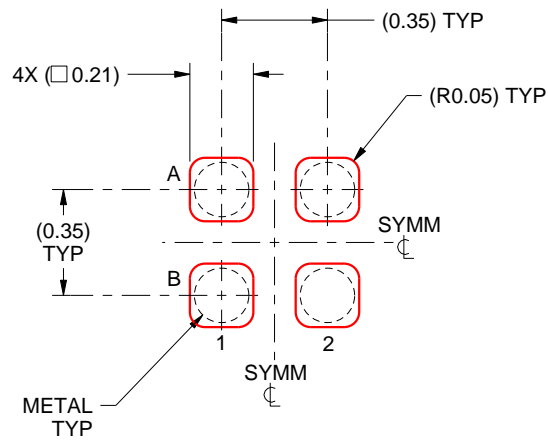
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

4220102/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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