

# LP2992 Micropower 250-mA Low-Noise Ultralow-Dropout Regulator in SOT-23 and WSON Packages Designed for Use with Very Low-ESR Output Capacitors

## 1 Features

- Input Voltage Range: 2.2 V to 16 V
- Output Voltage Range: 1.5 V to 5 V
- Wide Supply Voltage Range (16-V Maximum)
- Ultralow-Dropout Voltage
- Specified 250-mA Output Current
- Smallest Possible Size (SOT-23, WSON Package)
- Requires Minimum External Components
- Stable With Low-ESR Output Capacitor
- < 1- $\mu$ A Quiescent Current When Shut Down
- Low Ground Pin Current at All Loads
- Output Voltage Accuracy 1% (A Grade)
- High Peak Current Capability
- Low  $Z_{OUT}$ : 0.3- $\Omega$  Typical (10 Hz to 1 MHz)
- Overtemperature and Overcurrent Protection
- -40°C to 125°C Junction Temperature Range
- Custom Voltages Available

## 2 Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

## 3 Description

The LP2992 is a 250-mA, fixed-output voltage regulator designed to provide ultralow-dropout and low noise in battery powered applications.

Using an optimized Vertically Integrated PNP (VIP) process, the LP2992 delivers unequalled performance in all specifications critical to battery-powered designs:

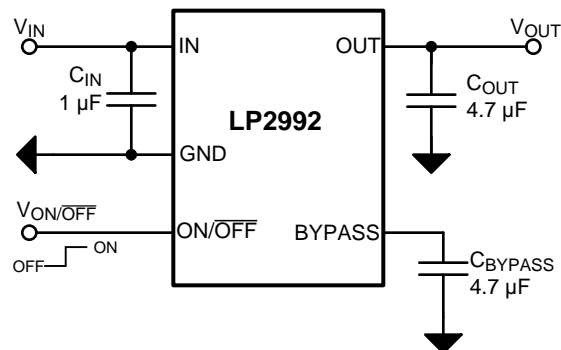
- Dropout voltage: Typically 450 mV at 250-mA load, and 5 mV at 1-mA load.
- Ground pin current: Typically 1500  $\mu$ A at 250-mA load, and 75  $\mu$ A at 1-mA load.
- Enhanced stability: The LP2992 is stable with output capacitor equivalent series resistance (ESR) as low as 5 m $\Omega$  which allows the use of ceramic capacitors on the output.
- Sleep mode: Less than 1- $\mu$ A quiescent current when ON/OFF pin is pulled low.
- Smallest possible size: SOT-23 and WSON packages use absolute minimum board space.
- Precision output: 1% tolerance output voltages available (A grade).
- Low noise: By adding a 10-nF bypass capacitor, output noise can be reduced to 30  $\mu$ V (typical).
- Multiple voltage options, from 1.5 V to 5 V, are available as standard products. Consult factory for custom voltages.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2992	WSON (6)	3.29 mm x 2.92 mm
	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



## Table of Contents

<b>1 Features</b> ..... 1 <b>2 Applications</b> ..... 1 <b>3 Description</b> ..... 1 <b>4 Revision History</b> ..... 2 <b>5 Pin Configuration and Functions</b> ..... 3 <b>6 Specifications</b> ..... 4 6.1 Absolute Maximum Ratings ..... 4 6.2 ESD Ratings..... 4 6.3 Recommended Operating Conditions ..... 4 6.4 Thermal Information ..... 4 6.5 Electrical Characteristics..... 5 6.6 Typical Characteristics ..... 7 <b>7 Detailed Description</b> ..... 13 7.1 Overview ..... 13 7.2 Functional Block Diagram ..... 13 7.3 Feature Description..... 13	7.4 Device Functional Modes..... 14 <b>8 Application and Implementation</b> ..... 15 8.1 Application Information..... 15 8.2 Typical Application ..... 15 <b>9 Power Supply Recommendations</b> ..... 19 <b>10 Layout</b> ..... 19 10.1 Layout Guidelines ..... 19 10.2 Layout Examples..... 19 10.3 WSON Mounting ..... 20 <b>11 Device and Documentation Support</b> ..... 21 11.1 Documentation Support ..... 21 11.2 Trademarks ..... 21 11.3 Electrostatic Discharge Caution..... 21 11.4 Glossary ..... 21 <b>12 Mechanical, Packaging, and Orderable Information</b> ..... 21
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## 4 Revision History

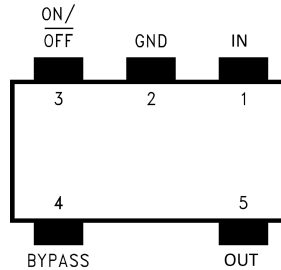
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March 2013) to Revision H	Page
<ul style="list-style-type: none"> <li>• Added <i>Device Information</i> and <i>ESD Ratings</i> tables, <i>Pin Configuration and Functions</i>, <i>Feature Description</i>, <i>Device Functional Modes</i>, <i>Application and Implementation</i>, <i>Power Supply Recommendations</i>, <i>Layout</i>, <i>Device and Documentation Support</i>, and <i>Mechanical, Packaging, and Orderable Information</i> sections; update <i>Thermal Values</i> and pin names ..... 1</li> </ul>	1

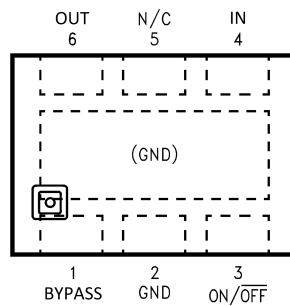
Changes from Revision F (March 2013) to Revision G	Page
<ul style="list-style-type: none"> <li>• Changed Changed layout of National Data Sheet to TI format ..... 1</li> </ul>	1

## 5 Pin Configuration and Functions

**SOT-23 (DBV) Package  
5 Pins  
Top View**



**WSO (NGD) Package  
6 Pins  
Top View**



### Pin Functions

PIN				I/O	DESCRIPTION
NAME	DBV	NAME	NGD		
BYPASS	4	BYPASS	1	I	Bypass capacitor for low-noise operation.
GND	2	GND	2	–	Ground.
IN	1	IN	4	I	Unregulated input voltage.
–	–	N/C	5	–	No internal connection. Connect to GND or leave open.
ON/OFF	3	ON/OFF	3	I	A low voltage on this pin disables the device, and the regulator enters a sleep mode. A high voltage on this pin enables the device.
OUT	5	OUT	6	O	Regulated output voltage. This pin requires an output capacitor to maintain stability. See the <a href="#">Detailed Design Procedure</a> section for output capacitor details.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
Lead temperature (soldering, 5 seconds)		260	°C
Power dissipation <sup>(3)</sup>	Internally Limited		
Input supply voltage (survival)	-0.3	16	V
Shutdown input voltage (survival)	-0.3	16	V
Output voltage (survival) <sup>(4)</sup>	-0.3	9	V
I <sub>OUT</sub> (survival)	Short-Circuit Protected		
Input-output voltage (survival) <sup>(5)</sup>	-0.3	16	V
Storage temperature, T <sub>stg</sub>	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military- or Aerospace-specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J(MAX)</sub>, the junction-to-ambient thermal resistance, R<sub>θJA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using:  

$$P_{(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$
 Where the value of R<sub>θJA</sub> for the SOT-23 package is 174.2°C/W in a typical PC board mounting and the WSON package is 72.3°C/W. Exceeding the maximum allowable dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
- If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2992 output must be diode-clamped to ground.
- The output PNP structure contains a diode between the IN to OUT pins that is normally reverse-biased. Reversing the polarity from V<sub>IN</sub> to V<sub>OUT</sub> will turn on this diode.

### 6.2 ESD Ratings

	VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V <sub>IN</sub> Input supply voltage	2.2 <sup>(1)</sup>	16	V
V <sub>ON/OFF</sub> ON/OFF input voltage	0	V <sub>IN</sub>	V
I <sub>OUT</sub> Output current		250	mA
T <sub>J</sub> Operating junction temperature	-40	125	°C

- Recommended minimum V<sub>IN</sub> is the greater of 2.2 V or V<sub>OUT</sub> + rated dropout voltage (maximum) for operating load current.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LP2992		UNIT
	DBV	NGD	
	5 PINS	6 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	174.2	72.3	°C/W
R <sub>θJC(top)</sub> Junction-to-case (top) thermal resistance	76.3	81.6	
R <sub>θJB</sub> Junction-to-board thermal resistance	30.9	39.5	
ψ <sub>JT</sub> Junction-to-top characterization parameter	2.8	2.0	
ψ <sub>JB</sub> Junction-to-board characterization parameter	30.4	39.2	
R <sub>θJC(bot)</sub> Junction-to-case (bottom) thermal resistance	n/a	11.6	

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Unless otherwise specified:  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $V_{ON/OFF} = 2\text{ V}$ . MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range unless otherwise noted; typical limits apply for  $T_A = T_J = 25^\circ\text{C}$ .

PARAMETER	TEST CONDITIONS	TYP	LP2992AI-X.X <sup>(1)</sup>		LP2992I-X.X <sup>(1)</sup>		UNIT
			MIN	MAX	MIN	MAX	
$\Delta V_{OUT}$ Output voltage tolerance	$I_L = 1\text{ mA}$ , $T_J = 25^\circ\text{C}$		-1	1	-1.5	1.5	% $V_{NOM}$
	$1\text{ mA} \leq I_L \leq 50\text{ mA}$ , $T_J = 25^\circ\text{C}$		-1.5	1.5	-2.5	2.5	
	$1\text{ mA} \leq I_L \leq 50\text{ mA}$		-2.5	2.5	-3.5	3.5	
	$1\text{ mA} \leq I_L \leq 250\text{ mA}$ , $T_J = 25^\circ\text{C}$		-3.5	3.5	-4	4	
	$1\text{ mA} \leq I_L \leq 250\text{ mA}$		-4.5	4.5	-5	5	
$\Delta V_{OUT}/\Delta V_{IN}$ Output voltage line regulation	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$ $T_J = 25^\circ\text{C}$	0.007		0.014		0.014	% $V$
	$V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 16\text{ V}$			0.032		0.032	
$V_{IN(min)}$ Minimum input voltage required to maintain output regulation		2.05		2.2		2.2	V
$V_{IN} - V_{OUT}$ Dropout voltage <sup>(2)</sup>	$I_L = 0\text{ mA}$ , $T_J = 25^\circ\text{C}$	0.5		2.5		2.5	mV
	$I_L = 0\text{ mA}$			4		4	
	$I_L = 1\text{ mA}$ , $T_J = 25^\circ\text{C}$	5		9		9	
	$I_L = 1\text{ mA}$			12		12	
	$I_L = 50\text{ mA}$ , $T_J = 25^\circ\text{C}$	100		125		125	
	$I_L = 50\text{ mA}$			180		180	
	$I_L = 150\text{ mA}$ , $T_J = 25^\circ\text{C}$	260		325		325	
	$I_L = 150\text{ mA}$			470		470	
	$I_L = 250\text{ mA}$ , $T_J = 25^\circ\text{C}$	450		575		575	
$I_L = 250\text{ mA}$			850		850		
$I_{GND}$ Ground pin current	$I_L = 0\text{ mA}$ , $T_J = 25^\circ\text{C}$	65		95		95	$\mu\text{A}$
	$I_L = 0\text{ mA}$			125		125	
	$I_L = 1\text{ mA}$ , $T_J = 25^\circ\text{C}$	75		110		110	
	$I_L = 1\text{ mA}$			170		170	
	$I_L = 50\text{ mA}$ , $T_J = 25^\circ\text{C}$	350		600		600	
	$I_L = 50\text{ mA}$			1000		1000	
	$I_L = 150\text{ mA}$ , $T_J = 25^\circ\text{C}$	850		1500		1500	
	$I_L = 150\text{ mA}$			2500		2500	
	$I_L = 250\text{ mA}$ , $T_J = 25^\circ\text{C}$	1500		2300		2300	
	$I_L = 250\text{ mA}$			4000		4000	
	$V_{ON/OFF} < 0.3\text{ V}$ , $T_J = 25^\circ\text{C}$	0.01		0.8		0.8	
$V_{ON/OFF} < 0.15\text{ V}$	0.05		2		2		
$V_{ON/OFF}$ ON/OFF input voltage <sup>(3)</sup>	High = O/P ON	1.4	1.6		1.6		V
	Low = O/P OFF	0.55		0.15		0.15	
$I_{ON/OFF}$ ON/OFF input current	$V_{ON/OFF} = 0$	0.01		-2		-2	$\mu\text{A}$
	$V_{ON/OFF} = 5\text{ V}$	5		15		15	
$e_n$ Output noise voltage (RMS)	Bandwidth = 300 Hz to 50 kHz $C_{OUT} = 10\text{ }\mu\text{F}$ $C_{BYPASS} = 10\text{ nF}$	30					$\mu\text{V}$
$\Delta V_{OUT}/\Delta V_{IN}$ Ripple rejection	$f = 1\text{ kHz}$ , $C_{BYPASS} = 10\text{ nF}$ $C_{OUT} = 10\text{ }\mu\text{F}$	45					dB

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
- (2)  $V_{IN}$  must be the greater of 2.2 V or  $V_{OUT(NOM)} +$  dropout voltage to maintain output regulation. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below the value measured with a 1-V differential.
- (3) The ON/OFF input must be properly driven to prevent possible mis-operation. For details, see [Operation with ON/OFF Control](#).

## Electrical Characteristics (continued)

Unless otherwise specified:  $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$ ,  $I_L = 1\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $V_{ON/OFF} = 2\text{ V}$ . MIN (minimum) and MAX (maximum) limits apply over the recommended operating temperature range unless otherwise noted; typical limits apply for  $T_A = T_J = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	TYP	LP2992AI-X.X <sup>(1)</sup>		LP2992I-X.X <sup>(1)</sup>		UNIT
				MIN	MAX	MIN	MAX	
$I_O(\text{SC})$	Short-circuit current	$R_L = 0$ (steady state) <sup>(4)</sup>	400					mA
$I_O(\text{PK})$	Peak output current	$V_{OUT} \geq V_{O(NOM)} - 5\%$	350					mA

(4) The LP2992 has thermal foldback current limiting which allows a high peak current when  $V_{OUT} > 0.5\text{ V}$ , and then reduces the maximum output current as  $V_{OUT}$  is forced to ground (see [Typical Characteristics](#) curves).

## 6.6 Typical Characteristics

Unless otherwise specified:  $C_{IN} = 1 \mu\text{F}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $V_{IN} = V_{OUT(NOM)} + 1 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , ON/OFF pin is tied to the IN pin.

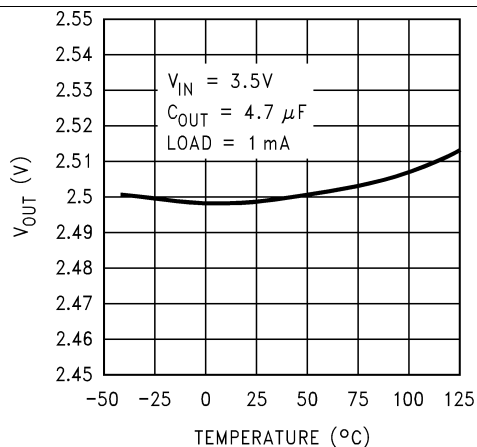


Figure 1.  $V_{OUT}$  vs Temperature

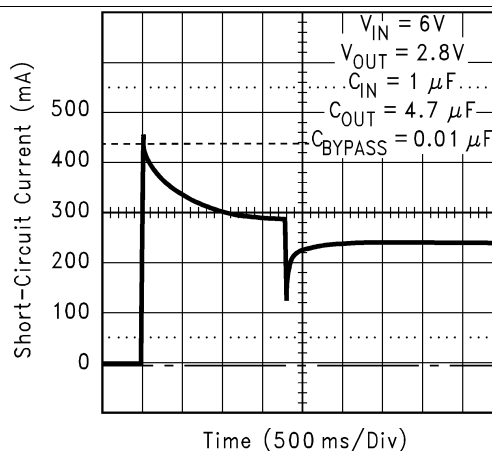


Figure 2. Short-Circuit Current

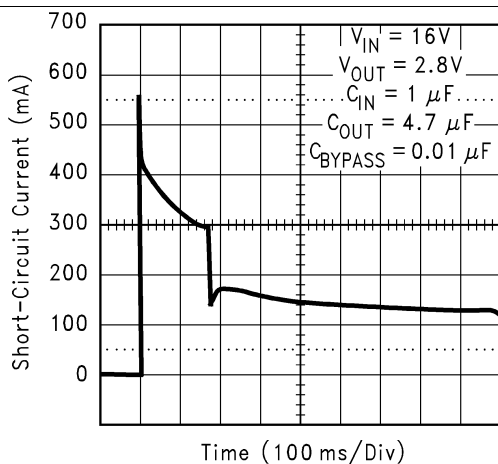


Figure 3. Short-Circuit Current

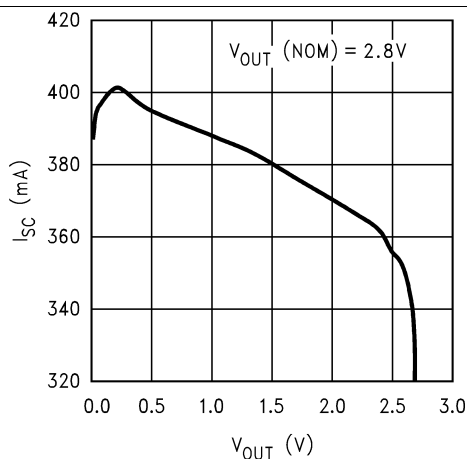


Figure 4. Short-Circuit Current vs Output Voltage

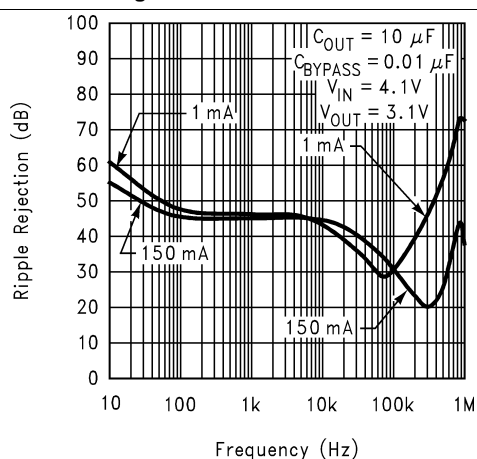


Figure 5. Ripple Rejection

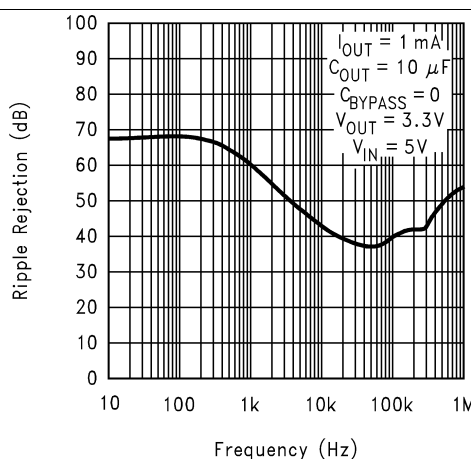


Figure 6. Ripple Rejection

### Typical Characteristics (continued)

Unless otherwise specified:  $C_{IN} = 1 \mu\text{F}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $V_{IN} = V_{OUT(NOM)} + 1 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , ON/OFF pin is tied to the IN pin.

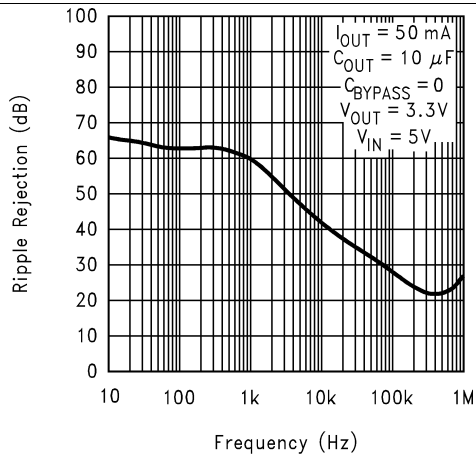


Figure 7. Ripple Rejection

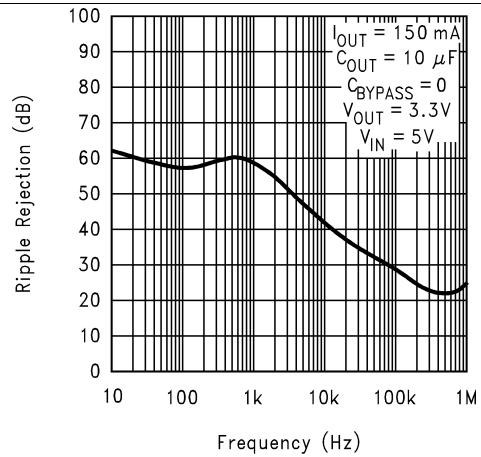


Figure 8. Ripple Rejection

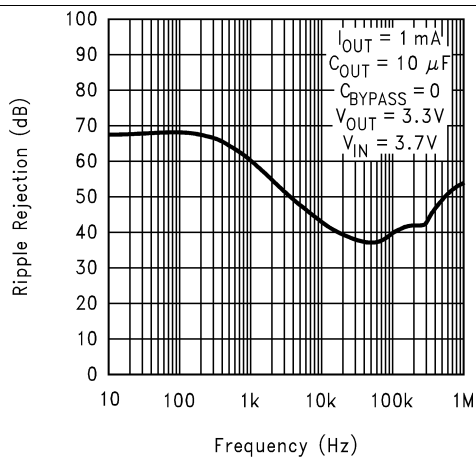


Figure 9. Ripple Rejection

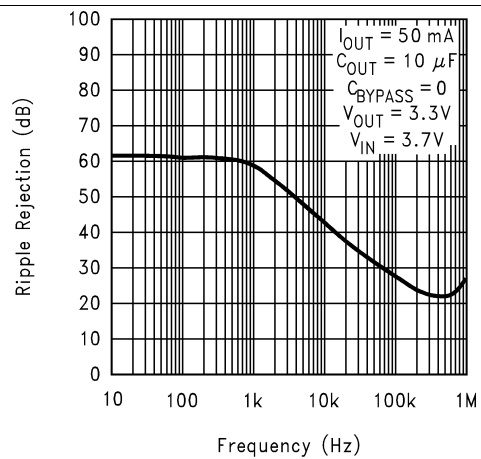


Figure 10. Ripple Rejection

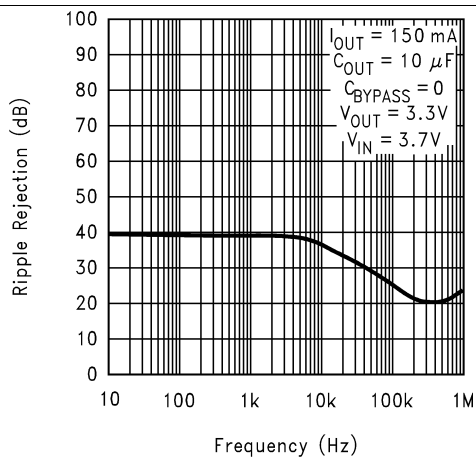


Figure 11. Ripple Rejection

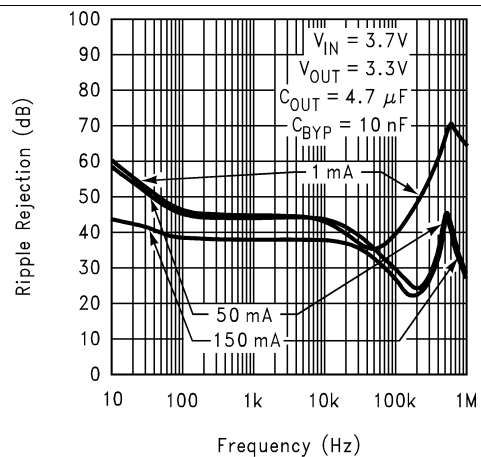


Figure 12. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified:  $C_{IN} = 1 \mu F$ ,  $C_{OUT} = 4.7 \mu F$ ,  $V_{IN} = V_{OUT(NOM)} + 1 V$ ,  $T_A = 25^\circ C$ , ON/OFF pin is tied to the IN pin.

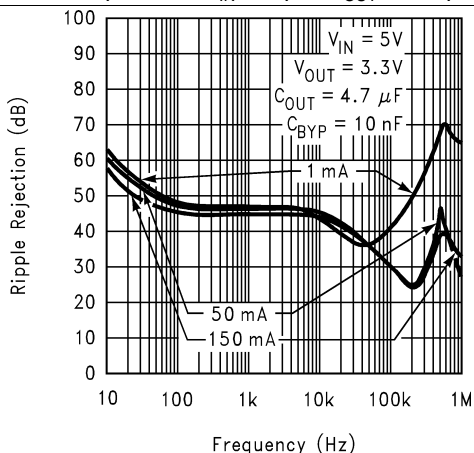


Figure 13. Ripple Rejection

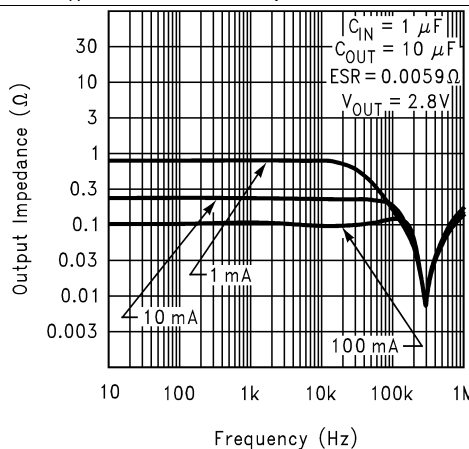


Figure 14. Output Impedance vs Frequency

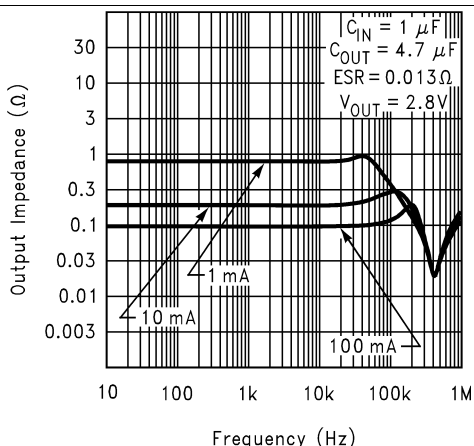


Figure 15. Output Impedance vs Frequency

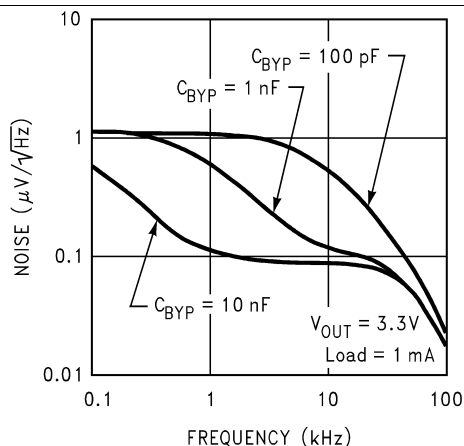


Figure 16. Output Noise Density

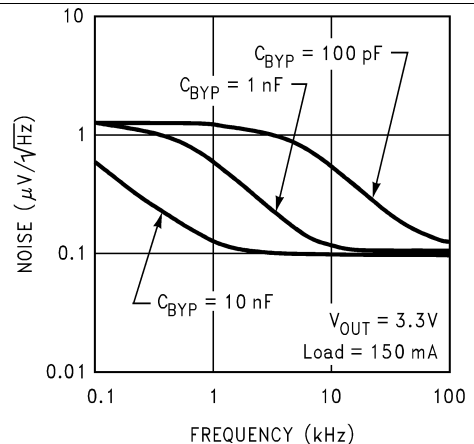


Figure 17. Output Noise Density

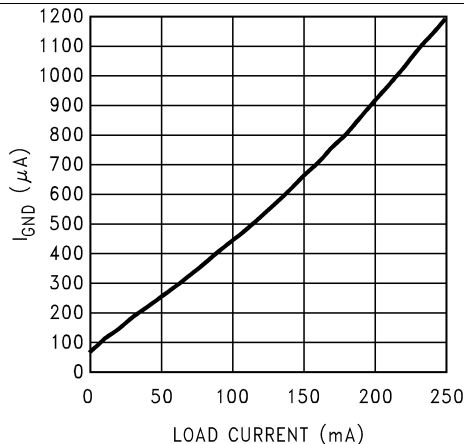
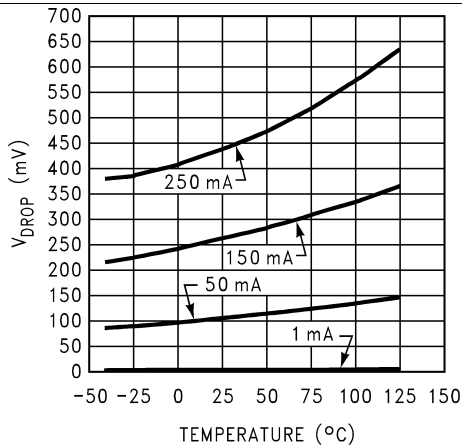


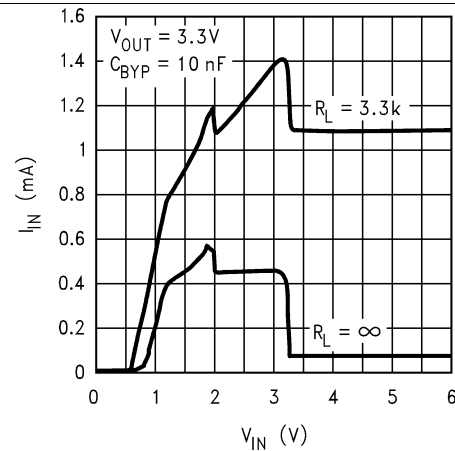
Figure 18. GND Pin vs Load Current

**Typical Characteristics (continued)**

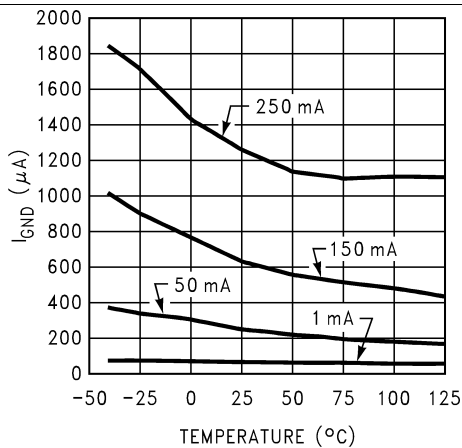
Unless otherwise specified:  $C_{IN} = 1 \mu F$ ,  $C_{OUT} = 4.7 \mu F$ ,  $V_{IN} = V_{OUT(NOM)} + 1 V$ ,  $T_A = 25^\circ C$ , ON/OFF pin is tied to the IN pin.



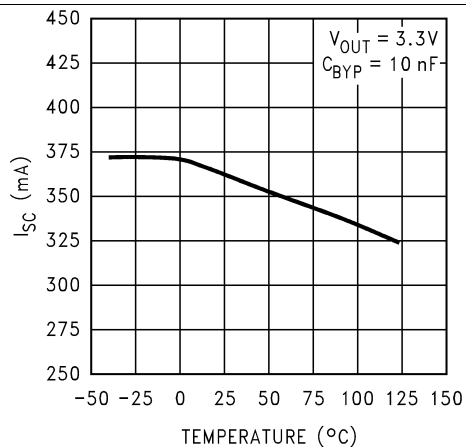
**Figure 19. Dropout Voltage vs Temperature**



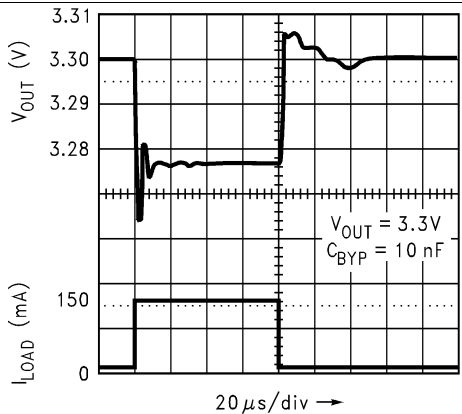
**Figure 20. Input Current vs Pin**



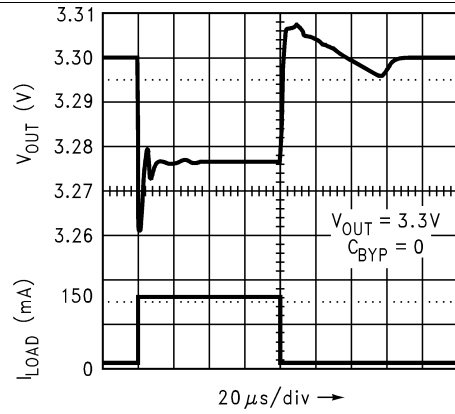
**Figure 21. I<sub>GND</sub> vs Load and Temperature**



**Figure 22. Instantaneous Short-Circuit Current**



**Figure 23. Load Transient Response**



**Figure 24. Load Transient Response**

Typical Characteristics (continued)

Unless otherwise specified:  $C_{IN} = 1 \mu F$ ,  $C_{OUT} = 4.7 \mu F$ ,  $V_{IN} = V_{OUT(NOM)} + 1 V$ ,  $T_A = 25^\circ C$ , ON/OFF pin is tied to the IN pin.

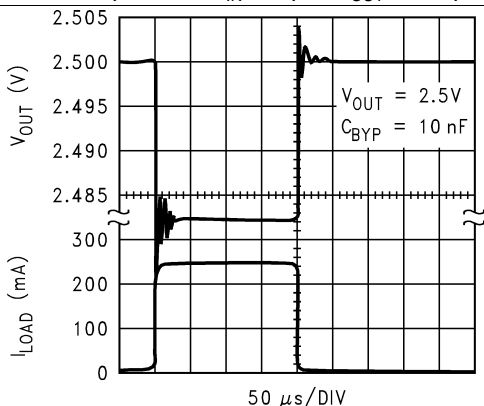


Figure 25. Load Transient Response

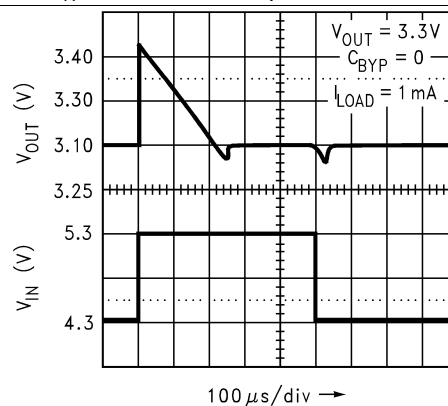


Figure 26. Line Transient Response

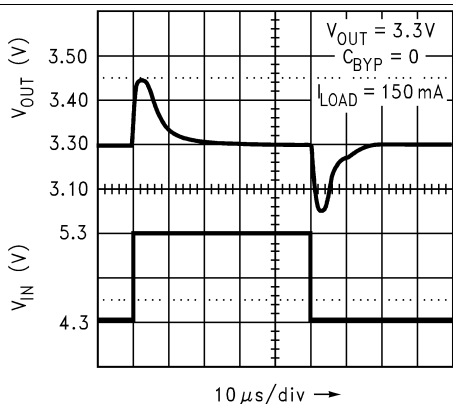


Figure 27. Line Transient Response

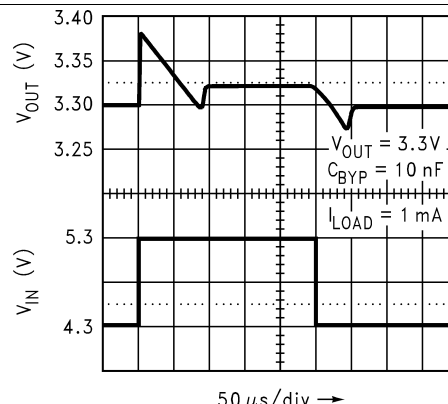


Figure 28. Line Transient Response

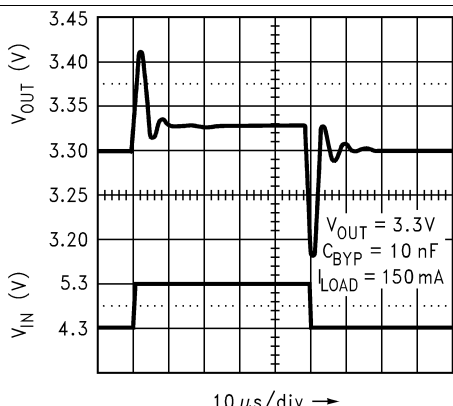


Figure 29. Line Transient Response

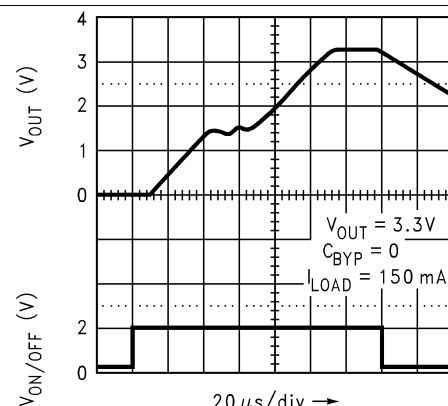
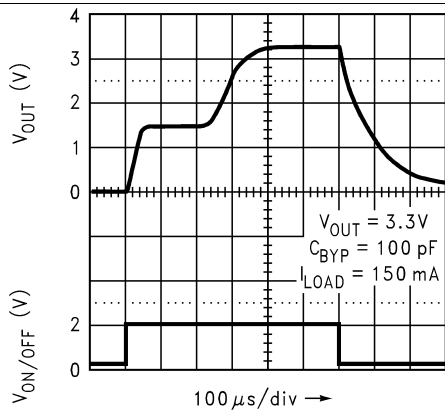
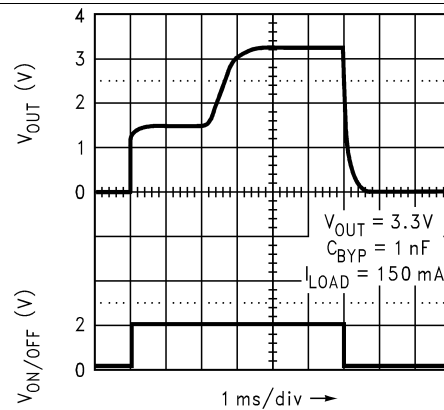
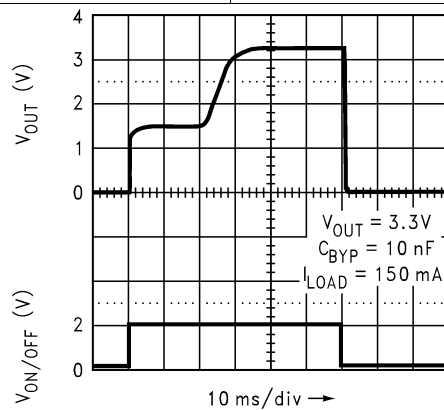


Figure 30. Turn-On Time

**Typical Characteristics (continued)**

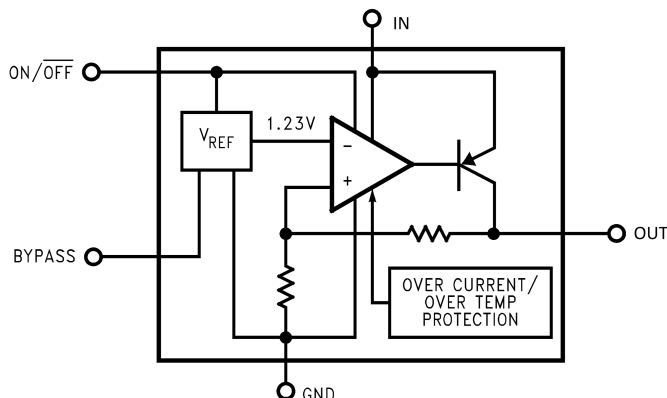
 Unless otherwise specified:  $C_{IN} = 1 \mu\text{F}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $V_{IN} = V_{OUT(NOM)} + 1 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , ON/OFF pin is tied to the IN pin.

**Figure 31. Turn-On Time**

**Figure 32. Turn-On Time**

**Figure 33. Turn-On Time**

## 7 Detailed Description

### 7.1 Overview

The LP2992 family of fixed-output, ultralow-dropout, and low-noise regulators offer exceptional and cost-effective performance for battery-powered applications. Available in output voltages from 1.5 V to 5 V, the family has an output tolerance of 1% for the A version and capable of delivering 250-mA continuous load current. Using an optimized VIP (Vertically Integrated PNP) process, the LP2992 delivers unequalled performance. The dropout voltage and the ground pin current with 250 mA of load current are typically 450 mV and 1500  $\mu$ A, respectively.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Sleep Mode

When the ON/OFF pin is pulled low, the LP2992 enters a sleep mode, and less than 1- $\mu$ A quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

#### 7.3.2 Low Ground Current

The LP2992 uses a vertical PNP process which allows for quiescent currents which are considerably lower than those associated with traditional lateral PNP regulators, typically 1500  $\mu$ A at 250-mA load and 75  $\mu$ A at 1-mA load.

#### 7.3.3 Low Noise

The LP2992 includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in a noise analysis. Further noise reduction can be achieved by adding an external bypass capacitor between the BYPASS pin and the GND pin. For more detailed information on noise reduction using the BYPASS pin, see [Noise Bypass Capacitor](#).

#### 7.3.4 Enhanced Stability

The LP2992 is designed specifically to work with ceramic output capacitors using circuitry that allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 m $\Omega$ . For output capacitor requirements, see [Output Capacitor](#).

#### 7.3.5 Overcurrent Protection

The internal current-limit circuit is used to protect the LDO against high-current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when the output impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

## Feature Description (continued)

The LP2992 is featured with the foldback current limit that allows a high peak current when  $V_{OUT} > 0.5\text{ V}$ , and then reduces the maximum output current as  $V_{OUT}$  is forced to ground.

### 7.3.6 Overtemperature Protection

The LP2992 is designed with the thermal shutdown circuitry to turn off the output when excessive heat is dissipated in the LDO. The internal protection circuitry of the LP2992 is designed to protect against thermal overload conditions. Continuously running the device into thermal shutdown degrades its reliability.

## 7.4 Device Functional Modes

### 7.4.1 Operation with $V_{OUT(TARGET)} + 0.9\text{ V} \geq V_{IN} \geq 16\text{ V}$

The LP2992 operates if the input voltage is equal to or exceeds  $V_{OUT(TARGET)} + 0.9\text{ V}$ . At input voltages below the minimum  $V_{IN}$  requirement, the device does not operate correctly and output voltage may not reach a target value.

### 7.4.2 Operation with $\overline{\text{ON/OFF}}$ Control

If the voltage on the  $\overline{\text{ON/OFF}}$  pin is less than  $0.15\text{ V}$ , the device is disabled and, in this shutdown state, current does not exceed  $2\text{ }\mu\text{A}$ . Raising the voltage at the  $\overline{\text{ON/OFF}}$  pin above  $1.6\text{ V}$  initiates the start-up sequence of the device. If this feature is not to be used, the  $\overline{\text{ON/OFF}}$  input should be tied to  $V_{IN}$  to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the  $\overline{\text{ON/OFF}}$  input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the [Electrical Characteristics](#) section under  $V_{\overline{\text{ON/OFF}}}$ . To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the  $\overline{\text{ON/OFF}}$  input must have a slew rate which is  $\geq 40\text{ mV}/\mu\text{s}$ .

#### CAUTION

The regulator output voltage can not be ensured if a slow-moving ac (or dc) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification  $V_{\overline{\text{ON/OFF}}}$  (see [Electrical Characteristics](#)).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

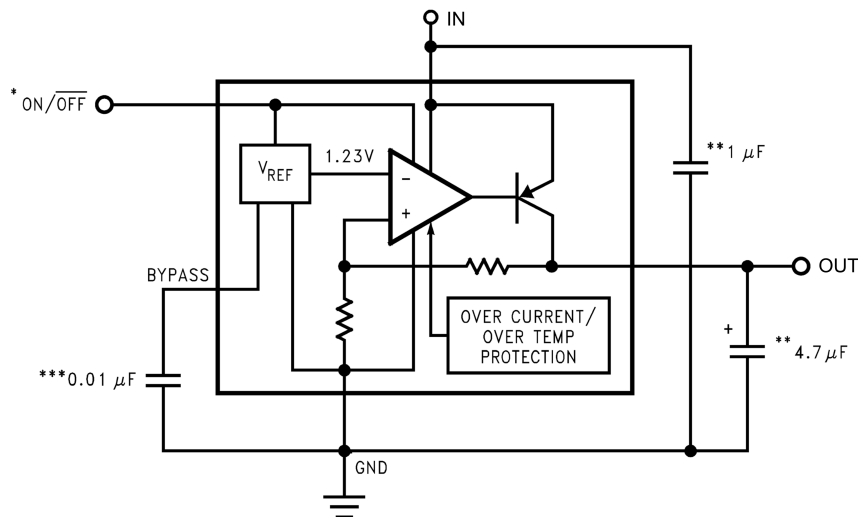
### 8.1 Application Information

The LP2992 is a 250-mA, fixed-output voltage regulator designed to provide ultralow-dropout and low noise in battery powered applications. The device is stable with output capacitor equivalent series resistance (ESR) as low as 5 mΩ which allows the use of ceramic capacitors on the output.

At 250-mA loading, the dropout voltage of the LP2992 is 850 mV maximum over temperature; thus, 1000-mV headroom is sufficient for operation over input and output voltage accuracy. The efficiency of the LP2992 in this configuration is  $V_{OUT}/V_{IN} = 76.7\%$ . To achieve the smallest form factor, the SOT-23 package is selected.

Input and output capacitors are selected in accordance with [Capacitor Characteristics](#). Ceramic capacitance of 1 μF for the input and that of 4.7 μF for the output are selected. With efficiency of 76.7% and a 250-mA load current, the internal power dissipation is 250 mW, which corresponds to 43.55°C junction temperature rise for the SOT-23 package. To minimize noise, a bypass capacitor ( $C_{BYPASS}$ ) of 0.01 μF is selected.

### 8.2 Typical Application



\*ON/OFF input must be actively terminated. Tie to the IN pin if this function is not to be used.

\*\*Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see [Output Capacitor](#)).

\*\*\*Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see [Capacitor Characteristics](#)).

Figure 34. Basic Application Circuit

#### 8.2.1 Design Requirements

DESIGN PARAMETER	VALUE
Input voltage	4.3 V
Output voltage	3.3 V
Output current	150 mA (maximum) 1 mA (minimum)
Output capacitor range	4.7 μF

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 External Capacitors

Like any low-dropout regulator, the LP2992 requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

#### 8.2.2.1.1 Input Capacitor

An input capacitor whose capacitance is  $\geq 1 \mu\text{F}$  is required between the LP2992 input and ground (the amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

#### NOTE

Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be  $\geq 1 \mu\text{F}$  over the entire operating temperature range.

#### 8.2.2.1.2 Output Capacitor

The LP2992 is designed specifically to work with ceramic output capacitors, using circuitry that allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 m $\Omega$ . It may also be possible to use Tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see [Figure 35](#)).

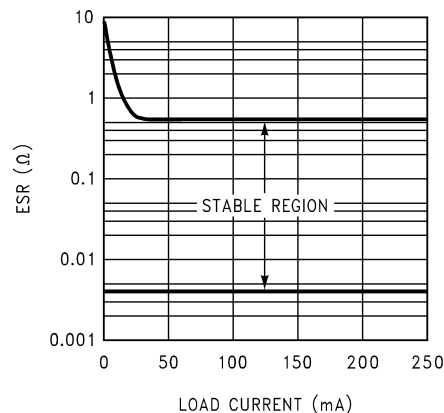


Figure 35. Stable ESR Range vs Load Current

The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

The LP2992 requires a minimum of 4.7  $\mu\text{F}$  on the output (output capacitor size can be increased without limit).

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. It should be noted that ceramic capacitors can exhibit large changes in capacitance with temperature (see [Capacitor Characteristics](#)).

The output capacitor must be located not more than 1 cm from the output pin and returned to a clean analog ground.

#### 8.2.2.1.3 Noise Bypass Capacitor

Connecting a 10-nF capacitor to the BYPASS pin significantly reduces noise on the regulator output. It should be noted that the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, dc leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10-nF polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

#### 8.2.2.2 Capacitor Characteristics

The LP2992 was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the 2.2- $\mu$ F to 10- $\mu$ F range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 4.7- $\mu$ F ceramic capacitor is in the range of 5 m $\Omega$  to 10 m $\Omega$ , which easily meets the ESR limits required for stability by the LP2992.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Most large value ceramic capacitors ( $\geq 2.2 \mu\text{F}$ ) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 4.7- $\mu$ F capacitor were used on the output because it will drop down to approximately 2.3  $\mu$ F at high ambient temperatures (which could cause the LP2992 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 10  $\mu$ F must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within  $\pm 15\%$ . Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

##### 8.2.2.2.1 Tantalum

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1- $\mu$ F to 4.7- $\mu$ F range.

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

It should also be noted that the ESR of a typical Tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

#### 8.2.2.3 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2992 has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into  $V_{\text{IN}}$  (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$  (cathode on  $V_{\text{IN}}$ , anode on  $V_{\text{OUT}}$ ), to limit the reverse voltage across the LP2992 to 0.3 V (see [Absolute Maximum Ratings](#)).

### 8.2.3 Application Curves

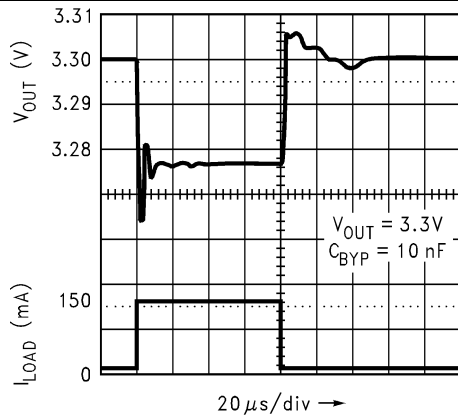


Figure 36. Load Transient Response

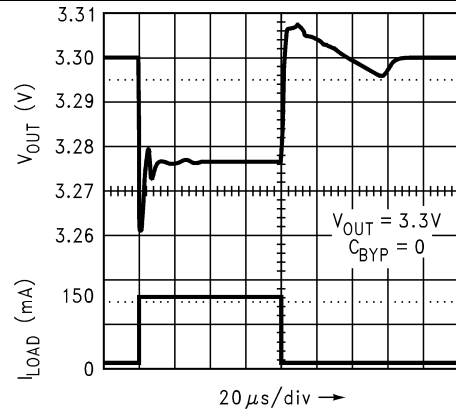


Figure 37. Load Transient Response

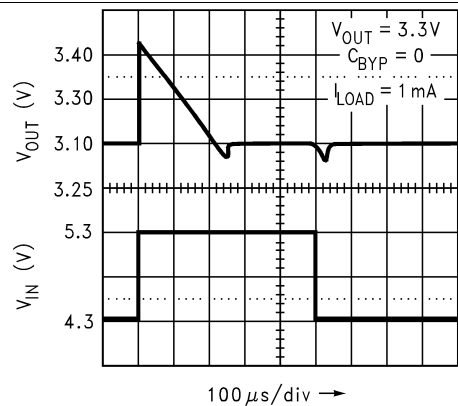


Figure 38. Line Transient Response

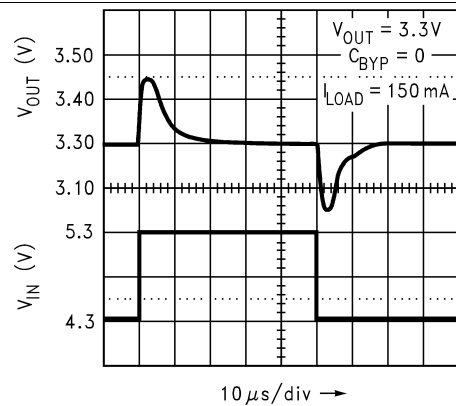


Figure 39. Line Transient Response

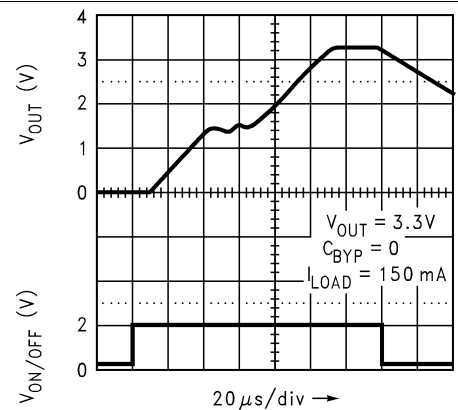


Figure 40. Turn-On Time

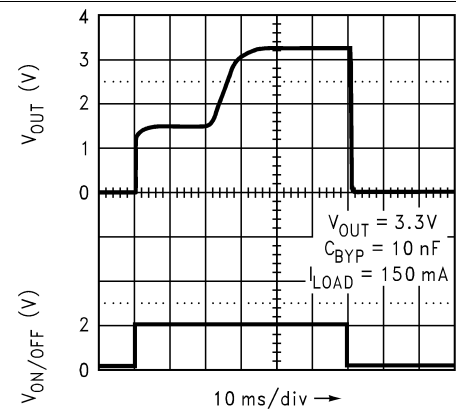


Figure 41. Turn-On Time

## 9 Power Supply Recommendations

The LP2992 is designed to operate from an input voltage supply range between 2.2 V and 16 V. The input voltage range provides the adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

## 10 Layout

### 10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

### 10.2 Layout Examples

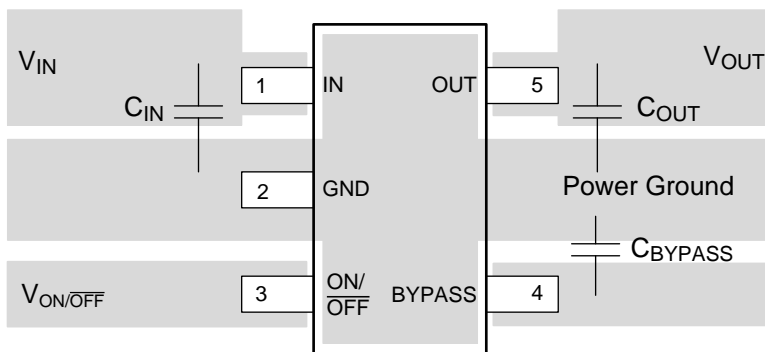


Figure 42. LP2992 SOT-23 Package Typical Layout

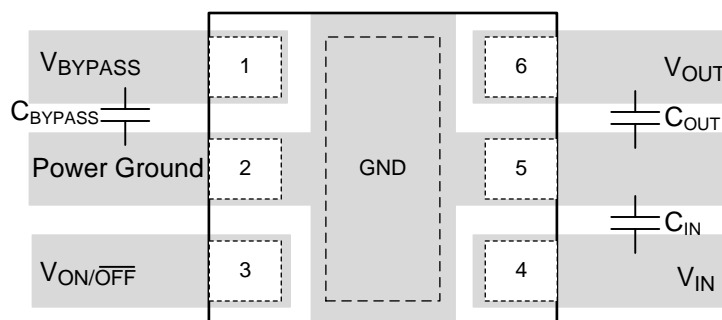


Figure 43. LP2992 WSON Package Typical Layout

### 10.3 WSON Mounting

The WSON package requires specific mounting techniques which are detailed in Application Note 1187 *Leadless Leadframe Package (LLP) (SNOA401)*. Referring to the section *PCB Design Recommendations*, it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area.

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

Application Note AN-1187 *Leadless Leadframe Package (LLP)* ([SNOA401](#)).

### 11.2 Trademarks

All trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992AILD-1.5/NOPB	ACTIVE	WSON	NGD	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L011A	<a href="#">Samples</a>
LP2992AILD-1.8/NOPB	ACTIVE	WSON	NGD	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L012A	<a href="#">Samples</a>
LP2992AILD-3.3/NOPB	ACTIVE	WSON	NGD	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L014A	<a href="#">Samples</a>
LP2992AILD-5.0/NOPB	ACTIVE	WSON	NGD	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L015A	<a href="#">Samples</a>
LP2992AILD-1.8/NOPB	ACTIVE	WSON	NGD	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L012A	<a href="#">Samples</a>
LP2992AILD-3.3/NOPB	ACTIVE	WSON	NGD	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L014A	<a href="#">Samples</a>
LP2992AILD-5.0/NOPB	ACTIVE	WSON	NGD	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L015A	<a href="#">Samples</a>
LP2992AIM5-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFBA	<a href="#">Samples</a>
LP2992AIM5-1.8	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFCA	
LP2992AIM5-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFCA	<a href="#">Samples</a>
LP2992AIM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFDA	
LP2992AIM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFDA	<a href="#">Samples</a>
LP2992AIM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFEA	
LP2992AIM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFEA	<a href="#">Samples</a>
LP2992AIM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFFA	
LP2992AIM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFFA	<a href="#">Samples</a>
LP2992AIM5X-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFBA	<a href="#">Samples</a>
LP2992AIM5X-1.8	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	LFCA	
LP2992AIM5X-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFCA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992AIM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFDA	<a href="#">Samples</a>
LP2992AIM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFEA	<a href="#">Samples</a>
LP2992AIM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFFA	<a href="#">Samples</a>
LP2992ILD-1.8/NOPB	ACTIVE	WSO	NGD	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L012A B	<a href="#">Samples</a>
LP2992ILD-2.5/NOPB	ACTIVE	WSO	NGD	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L013A B	<a href="#">Samples</a>
LP2992ILD-3.3/NOPB	ACTIVE	WSO	NGD	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L014A B	<a href="#">Samples</a>
LP2992ILD-5.0/NOPB	ACTIVE	WSO	NGD	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L015A B	<a href="#">Samples</a>
LP2992ILD-1.5/NOPB	ACTIVE	WSO	NGD	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L011A B	<a href="#">Samples</a>
LP2992ILD-1.8/NOPB	ACTIVE	WSO	NGD	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L012A B	<a href="#">Samples</a>
LP2992ILD-3.3/NOPB	ACTIVE	WSO	NGD	6	4500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-3-260C-168 HR	-40 to 125	L014A B	<a href="#">Samples</a>
LP2992ILD-5.0/NOPB	ACTIVE	WSO	NGD	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L015A B	<a href="#">Samples</a>
LP2992IM5-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFBB	<a href="#">Samples</a>
LP2992IM5-1.8	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFGB	
LP2992IM5-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFGB	<a href="#">Samples</a>
LP2992IM5-2.5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFDB	
LP2992IM5-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFDB	<a href="#">Samples</a>
LP2992IM5-3.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LF8B	
LP2992IM5-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LF8B	<a href="#">Samples</a>
LP2992IM5-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFEB	
LP2992IM5-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFEB	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2992IM5-5.0	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LFFB	
LP2992IM5-5.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFFB	<a href="#">Samples</a>
LP2992IM5X-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFBB	<a href="#">Samples</a>
LP2992IM5X-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFDB	<a href="#">Samples</a>
LP2992IM5X-2.5	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	LFDB	
LP2992IM5X-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFDB	<a href="#">Samples</a>
LP2992IM5X-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFEB	<a href="#">Samples</a>
LP2992IM5X-5.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFFB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2992AILD-1.5/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-1.8/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-3.3/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-5.0/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-1.8/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-3.3/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AILD-5.0/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992AIM5-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-1.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-1.8	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2992AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992ILD-1.8/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-2.5/NOPB	WSON	NGD	6	1000	178.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-3.3/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-5.0/NOPB	WSON	NGD	6	1000	180.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-1.5/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-1.8/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-3.3/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992ILD-5.0/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP2992IM5-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-1.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-2.5	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2992IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2992AILD-1.5/NOPB	WSON	NGD	6	1000	213.0	191.0	55.0
LP2992AILD-1.8/NOPB	WSON	NGD	6	1000	195.0	200.0	45.0
LP2992AILD-3.3/NOPB	WSON	NGD	6	1000	195.0	200.0	45.0
LP2992AILD-5.0/NOPB	WSON	NGD	6	1000	195.0	200.0	45.0
LP2992AILD-1.8/NOPB	WSON	NGD	6	4500	367.0	367.0	35.0
LP2992AILD-3.3/NOPB	WSON	NGD	6	4500	370.0	355.0	55.0
LP2992AILD-5.0/NOPB	WSON	NGD	6	4500	370.0	355.0	55.0
LP2992AIM5-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-1.8	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992AIM5X-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-1.8	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2992AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992ILD-1.8/NOPB	WSON	NGD	6	1000	195.0	200.0	45.0
LP2992ILD-2.5/NOPB	WSON	NGD	6	1000	213.0	191.0	55.0
LP2992ILD-3.3/NOPB	WSON	NGD	6	1000	195.0	200.0	45.0
LP2992ILD-5.0/NOPB	WSON	NGD	6	1000	195.0	200.0	45.0
LP2992ILD-1.5/NOPB	WSON	NGD	6	4500	370.0	355.0	55.0
LP2992ILD-1.8/NOPB	WSON	NGD	6	4500	367.0	367.0	35.0
LP2992ILD-3.3/NOPB	WSON	NGD	6	4500	370.0	355.0	55.0
LP2992ILD-5.0/NOPB	WSON	NGD	6	4500	367.0	367.0	35.0
LP2992IM5-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-1.8	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2992IM5X-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-2.5	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2992IM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

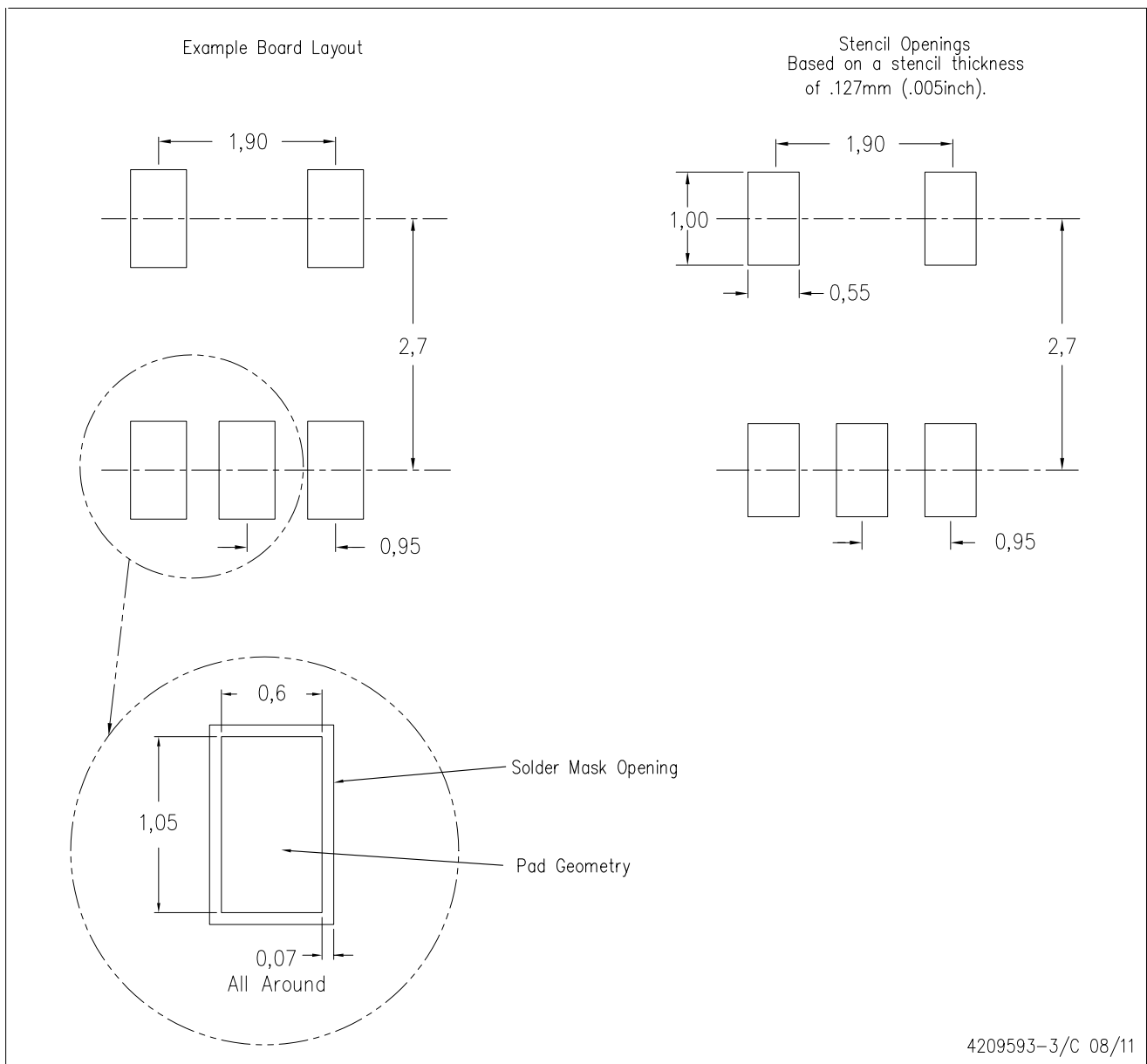
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

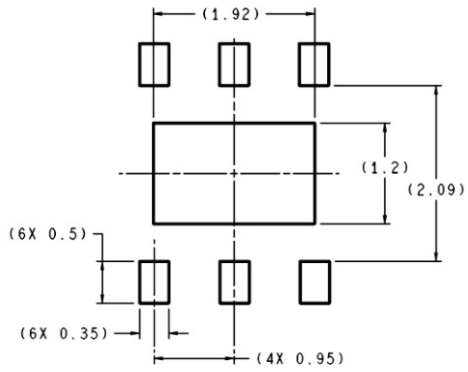
DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

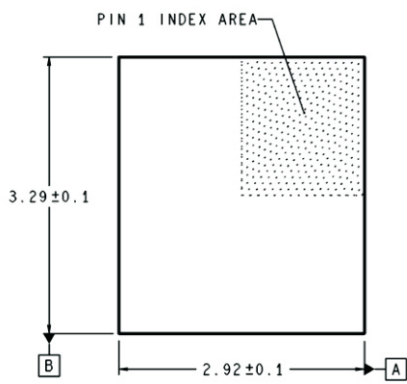


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

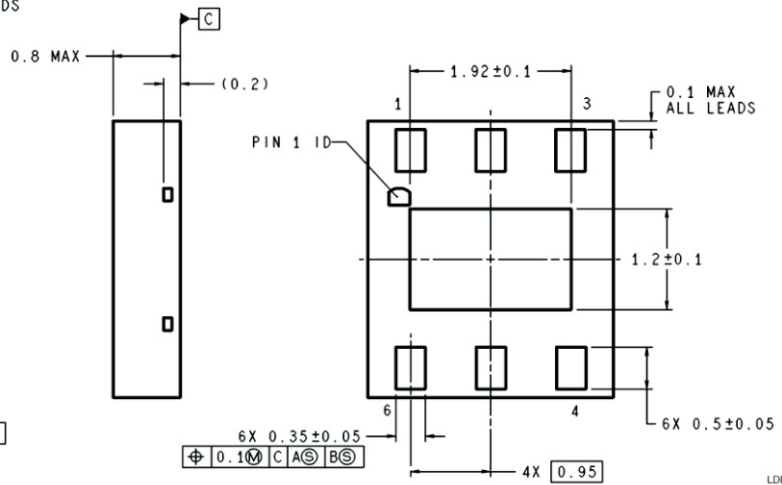
NGD0006A



RECOMMENDED LAND PATTERN  
1:1 RATIO WITH PKG SOLDER PADS



DIMENSIONS ARE IN MILLIMETERS



LDE06A (Rev A)

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