

具有 3.0V-14.5V 输入，采用四方扁平无引线 (QFN) 封装的 30A SIMPLE SWITCHER® 电源模块

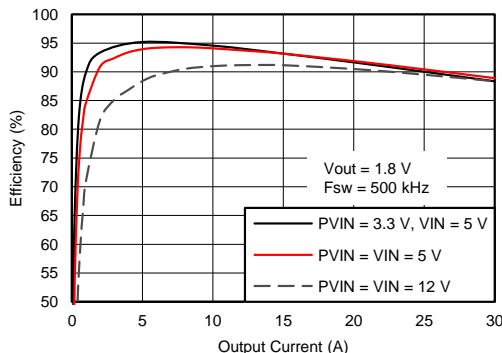
 查询样片: [LMZ31530](#)

特性

- 完全集成的电源解决方案；尺寸小于离散设计
- **15mm × 16mm × 5.8mm** 封装尺寸
 - 与 **LMZ31520** 引脚兼容
- 超快速负载阶跃响应
- 效率高达 **96%**
- 宽输出电压调节
0.6V 至 3.6V，基准精度为 **1%**
- 可选分离电源轨可实现低至 **3.0V** 的输入电压
- 可调开关频率；
(**300kHz 至 850kHz**)
- 可选缓启动
- 可调过流限制
- 电源正常输出
- 输出电压排序
- 过热保护
- 预偏置输出启动
- 运行温度范围: **-40°C 至 85°C**
- 增强的散热性能: **8.6°C/W**
- 符合 **EN55022 A** 类辐射标准
 - 集成屏蔽电感器

应用范围

- 宽带和通信基础设施
- 数字信号处理器 (**DSP**) 和现场可编程门阵列 (**FPGA**) 负载点应用
- 高密度电源系统

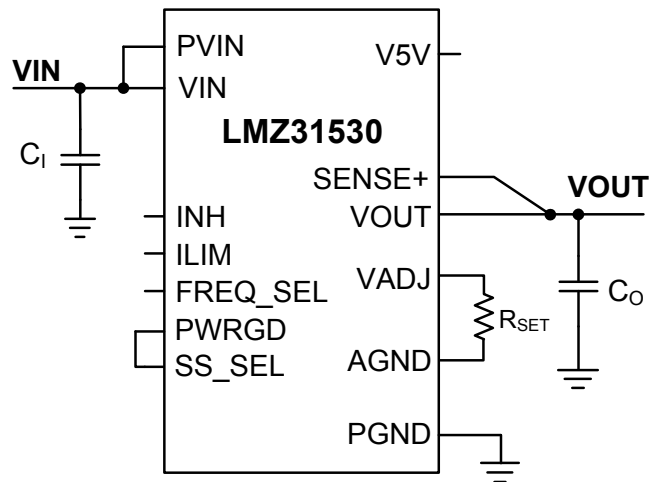


说明

LMZ31530 SIMPLE SWITCHER® 电源模块是一款易于使用的集成式电源解决方案，此方案在一个半高的 QFN 封装内组合了一个带有功率金属氧化物半导体场效应管 (MOSFET) 的 30A 直流/直流转换器、一个屏蔽电感器以及无源元件。这个整体电源解决方案仅需三个外部元件，并免除了环路补偿和磁性部件选择过程。

15mm x 16mm x 5.8mm QFN 封装可以很轻松地焊接到一个印刷电路板上，并且可实现一个紧凑的负载点设计。可实现 **95%** 以上的效率，具有超快速负载阶跃响应，以及热阻抗为 **8.6°C/W** 的出色功率耗散能力。LMZ31530 提供离散负载点设计的灵活性和特性集，并且非常适合为广泛的集成电路 (IC) 和系统供电。先进的封装技术可提供与标准 QFN 贴装和测试技术兼容的稳健耐用且可靠的电源解决方案。

简化的应用



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

is a trademark of ~ Texas Instruments.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating temperature range (unless otherwise noted)		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN, PVIN	-0.3	20	V
	INH, VADJ, PWRGD, PWRGD_PU, ILIM, FREQ_SEL, SS_SEL, V5V	-0.3	7	V
Output Voltage	PH	-1	25	V
	PH 10ns Transient	-2	27	
	VOUT	-0.3	6	V
V _{DIFF} (GND to exposed thermal pad)			±200	mV
Operating Junction Temperature		-40	125 ⁽²⁾	°C
Storage Temperature		-55	150	°C
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		250	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) See the temperature derating curves in the Typical Characteristics section for thermal information.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)		MIN	MAX	UNIT
PV _{IN}	Input Switching Voltage	3.0	14.5	V
V _{IN}	Input Bias Voltage	4.5	14.5	V
V _{OUT}	Output Voltage	0.6	3.6	V
f _{SW}	Switching Frequency	300	850	kHz

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾			LMZ31530	UNIT
			RLG	
			72 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	Natural Convection	8.6	°C/W
$\theta_{JA(100LFM)}$	Junction-to-ambient thermal resistance ⁽³⁾	100 LFM	7.8	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾		1.6	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾		4.2	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance, θ_{JA} , applies to devices soldered directly to a 100 mm x 100 mm, 6-layer PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA} .
- (3) The junction-to-ambient thermal resistance, θ_{JA} , applies to devices soldered directly to a 100 mm x 100 mm, 6-layer PCB with 1 oz. copper and 100 LFM forced air cooling. Additional airflow reduces θ_{JA} .
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

PACKAGE SPECIFICATIONS

LMZ31530		UNIT
Weight		4.96 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, $T_A = 40^\circ\text{C}$, ground benign	26.5 Mhrs

ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to 85°C , $P_{VIN} = V_{IN} = 12\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 30\text{ A}$

$C_{IN} = 2 \times 22\ \mu\text{F}$ ceramic & $330\ \mu\text{F}$ bulk, $C_{OUT} = 4 \times 100\ \mu\text{F}$ ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current			0		30	A
V_{IN}	Input bias voltage range	Over I_{OUT} range		4.5		14.5	V
P_{VIN}	Input switching voltage range	Over I_{OUT} range		3.0 ⁽¹⁾		14.5	V
UVLO	VIN Undervoltage lockout	VIN Increasing		4.0	4.2	4.33	V
		Hysteresis		0.25			
$V_{OUT(adjust)}$	Output voltage adjust range	Over I_{OUT} range		0.6		3.6	V
V_{OUT}	Set-point voltage tolerance					$\pm 1.0\%$ ⁽²⁾	
	Temperature variation	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$				$\pm 0.25\%$	
	Load regulation	Over I_{OUT} range				+0.4%	
	Total output voltage variation	Includes set-point, load, and temperature variation				$\pm 2.0\%$ ⁽²⁾	
Line regulation		$P_{VIN} \pm 10\%$				$\pm 0.1\%$	
		Over P_{VIN} range				$\pm 0.7\%$	
η	Efficiency	$P_{VIN} = V_{IN} = 12\text{ V}$ $I_O = 15\text{ A}$	$V_{OUT} = 3.3\text{ V}$, $f_{SW} = 500\text{kHz}$			94	%
			$V_{OUT} = 1.8\text{ V}$, $f_{SW} = 500\text{kHz}$			92	
			$V_{OUT} = 1.2\text{ V}$, $f_{SW} = 500\text{kHz}$			88	
			$V_{OUT} = 0.9\text{ V}$, $f_{SW} = 500\text{kHz}$			86	
			$V_{OUT} = 0.6\text{ V}$, $f_{SW} = 500\text{kHz}$			82	
		$P_{VIN} = V_{IN} = 5\text{ V}$ $I_O = 15\text{ A}$	$V_{OUT} = 3.3\text{ V}$, $f_{SW} = 500\text{kHz}$			96	%
			$V_{OUT} = 1.8\text{ V}$, $f_{SW} = 500\text{kHz}$			94	
			$V_{OUT} = 1.2\text{ V}$, $f_{SW} = 500\text{kHz}$			91	
			$V_{OUT} = 0.9\text{ V}$, $f_{SW} = 500\text{kHz}$			88	
			$V_{OUT} = 0.6\text{ V}$, $f_{SW} = 500\text{kHz}$			85	
Output voltage ripple	20 MHz bandwidth				1%	V_{OUT}	
I_{LIM}	Current limit threshold					40	A
Transient response	2.5 A/ μs load step from 25 to 75% $I_{OUT(max)}$	Recovery time				30	μs
		VOUT over/undershoot				30	mV
V_{INH}	Inhibit Control	Inhibit High Voltage		1.8		Open ⁽³⁾	V
		Inhibit Low Voltage		-0.3		0.6	V
$I_{IN(stby)}$	VIN standby current	INH pin to AGND	$V_{IN} = 5\text{ V}$	0.5	0.7	mA	
			$V_{IN} = 12\text{ V}$	1.2	1.5	mA	
Power Good	PWRGD Thresholds	V_{OUT} rising	Good			95	%
			Fault			115	
		V_{OUT} falling	Fault			90	
			Good			110	
PWRGD Low Voltage	$I(PWRGD) = 2\text{ mA}$				0.2	0.3	V
f_{SW}	Switching frequency	FREQ_SEL pin OPEN, $I_{OUT} = 10\text{ A}$		470	520	570	kHz
f_{SEL}	Frequency Select ⁽⁴⁾	66 k Ω resistor between FREQ_SEL pin and PGND				300	kHz
		FREQ_SEL pin connected to V5V (pin 61)				850	kHz
Thermal Shutdown	Thermal Shutdown	Thermal shutdown				145	$^\circ\text{C}$
		Thermal shutdown hysteresis				10	$^\circ\text{C}$
C_{IN}	External input capacitance	Ceramic		44 ⁽⁵⁾	94	μF	
		Non-ceramic					330

(1) The minimum PVIN voltage is 3.0V or ($V_{OUT} + 1.1\text{V}$), whichever is greater. See [VIN and PVIN Input Voltage](#) for more details.

(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.

(3) This pin has an internal pull-up. If this pin is left open circuit, the device operates when a valid input voltage is applied. A small, low-leakage (<300nA) MOSFET is recommended for control.

(4) See the [Frequency Select](#) section for more information on selecting the frequency.

(5) A minimum of 44 μF ($2 \times 22\ \mu\text{F}$) of external ceramic capacitance is required across the input (P_{VIN}/V_{IN} and PGND connected) for proper operation. Locate the capacitor close to the device. See [Table 3](#) for more details. When operating with split VIN and PVIN rails, place 4.7 μF of ceramic capacitance directly at the VIN pin to PGND.

ELECTRICAL CHARACTERISTICS (continued)

T_A = -40°C to 85°C, P_{VIN} = V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 30A

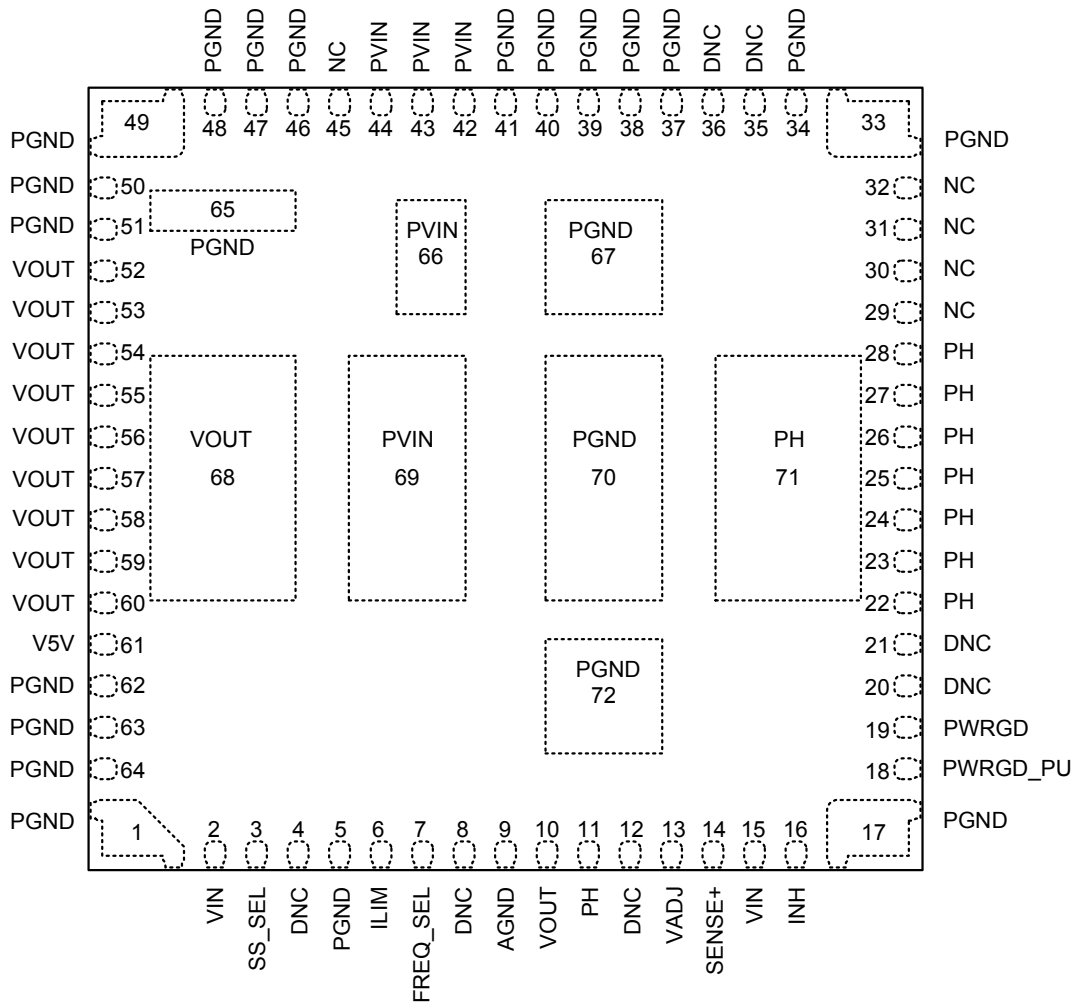
C_{IN} = 2x 22 μF ceramic & 330 μF bulk, C_{OUT} = 4x 100 μF ceramic (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{OUT}	External output capacitance	100 ⁽⁶⁾	400	5000	μF

(6) A minimum of 100 μF of ceramic capacitance is required at the output. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients and reduces ripple. See Table 3 for more details.

DEVICE INFORMATION

**RLG PACKAGE
(TOP VIEW)**



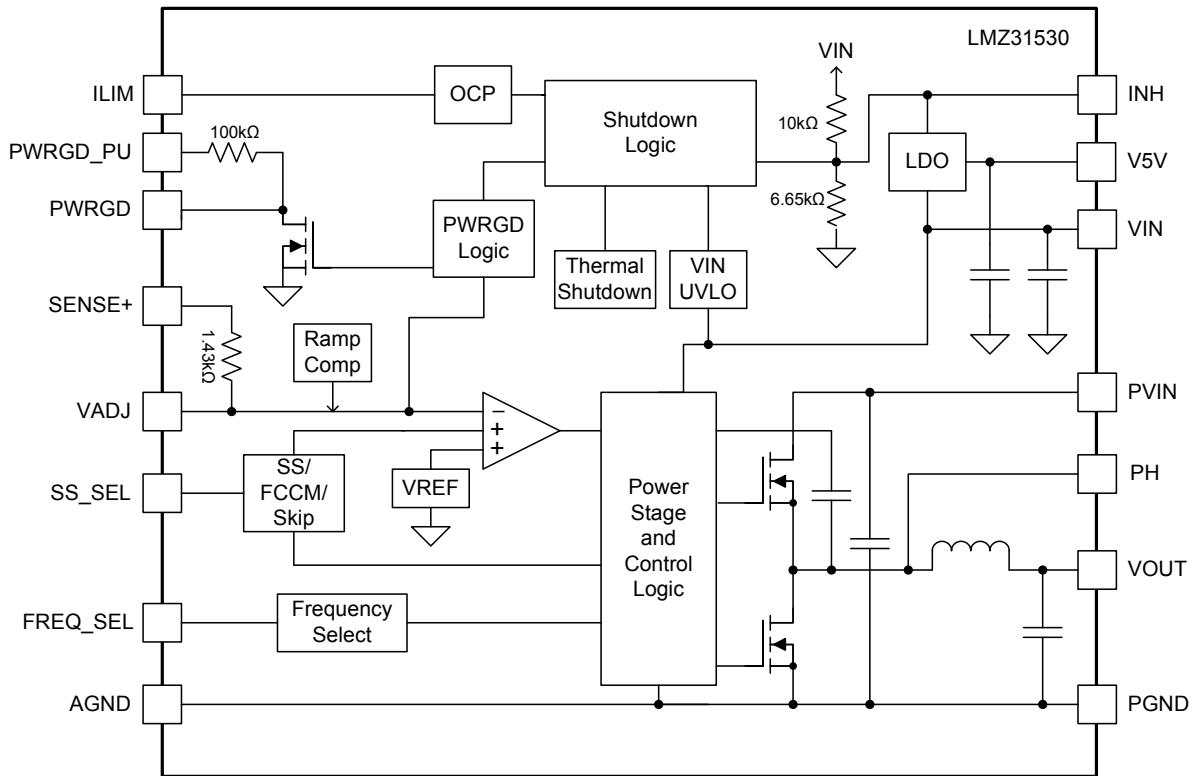
PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	9	This pin is connected internally to the power ground of the device. This pin should only be used as the zero volt ground reference for connecting the voltage setting resistor (R_{SET}). Do not connect AGND to PGND. See Layout Recommendations.
DNC	4	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	8	
	12	
	20	
	21	
	35	
	36	
FREQ_SEL	7	Frequency Select pin. Leave this pin open (floating) to select 500 kHz (typ) operating frequency. Connect this pin to V5V pin to select 850 kHz (typ) operating frequency. Connect a 66 k Ω resistor between this pin and PGND to select 300 kHz (typ) operating frequency. See Table 2 for more info.
ILIM	6	Current limit setting pin. Connecting a resistor between this pin and PGND sets the current limit. When left open, refer to the Electrical Characterization table for current limit value.
INH	16	Inhibit pin. Use an open drain or open collector logic device to ground this pin to control the INH function.
NC	29	Not Connected. These pins are internally isolated from any signal and all other pins. Each pin must be soldered to a pad on the PCB. These pins can be left isolated, connected to one another, or connected to any signal on the PCB.
	30	
	31	
	32	
	45	
PGND	1	This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. Pads 65, 67, 70, and 72 should be connected to PCB ground planes using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the device.
	5	
	17	
	33	
	34	
	37	
	38	
	39	
	40	
	41	
	46	
	47	
	48	
	49	
	50	
	51	
62		
63		
64		
65		
67		
70		
72		

PIN DESCRIPTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
PH	11	Phase switch node. Do not place any external component on these pins or tie them to a pin of another function. Connect these pins using a copper area beneath pad 71.
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	71	
PVIN	42	Input switching voltage pin. This pin supplies voltage to the power switches of the converter.
	43	
	44	
	66	
	69	
PWRGD	19	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately $\pm 6\%$ out of regulation.
PWRGD_PU	18	Power Good pull-up pin. This pin is connected to a 100k Ω resistor which is tied to the PWRGD pin internally. Connect this pin to V5V or to any voltage between 1.3V and 6.5V.
SENSE+	14	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins.
SS_SEL	3	Slow-start select pin. Connect a resistor between this pin and PWRGD (or PGND) to select the slow-start time. See the SS_SEL section of the datasheet for slow-start times and corresponding resistor values. Connect the SS_SEL pin to PGND to select Auto-skip Eco-mode or to the PWRGD pin (pin 19) to select FCCM.
V5V	61	5V regulator pin. This regulator supplies the internal circuitry.
VADJ	13	Output voltage adjust pin. Connecting a resistor between this pin and AGND sets the output voltage.
VIN	2	Input bias voltage pins. Supplies the control circuitry of the power converter.
	15	
VOUT	10	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND.
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
68		

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS (PVIN = VIN = 12 V) (1) (2)

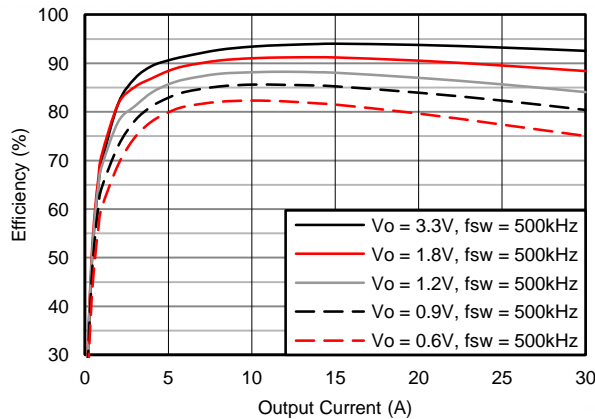


Figure 1. Efficiency vs. Output Current

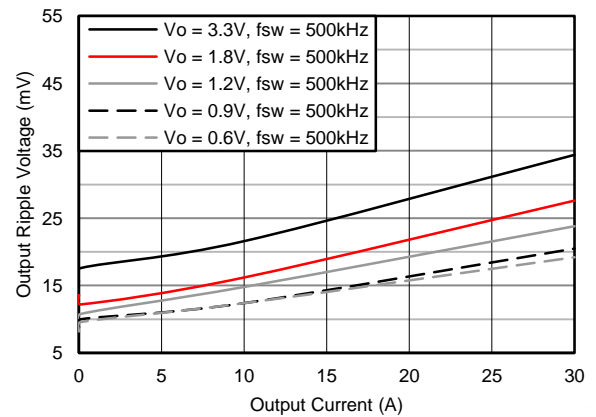


Figure 2. Voltage Ripple vs. Output Current

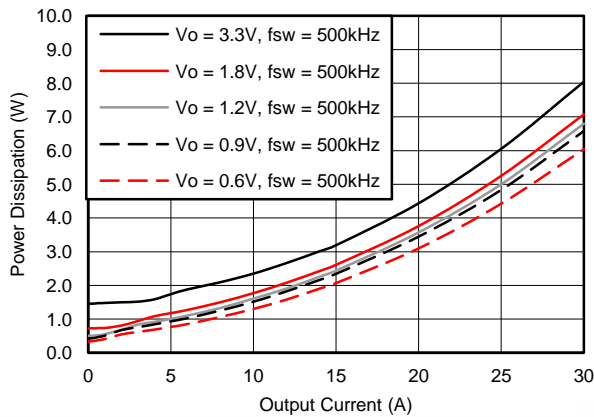


Figure 3. Power Dissipation vs. Output Current

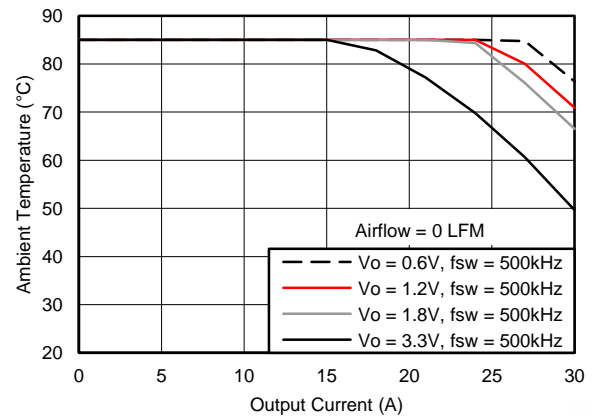


Figure 4. Safe Operating Area (0 LFM)

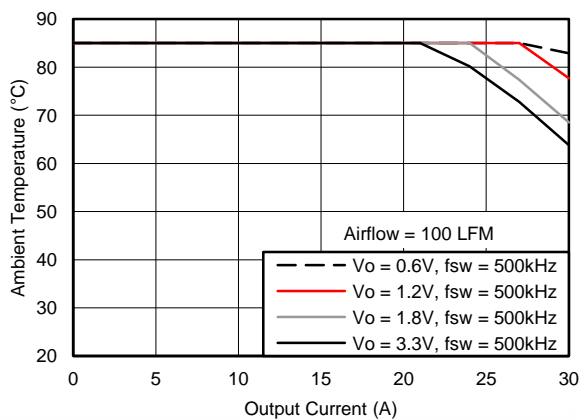


Figure 5. Safe Operating Area (100 LFM)

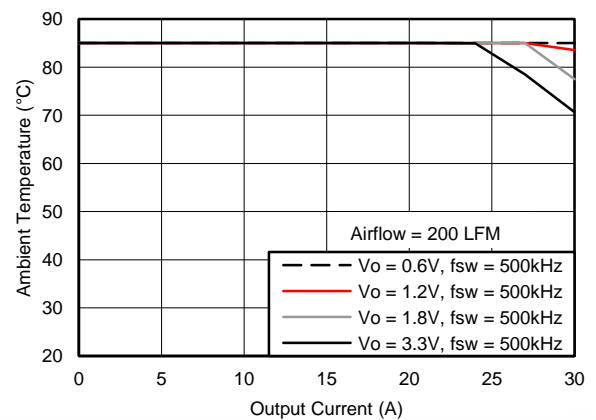


Figure 6. Safe Operating Area (200 LFM)

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 1](#), [Figure 2](#), and [Figure 3](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm six-layer PCB with 1 oz. copper. Applies to [Figure 4](#), [Figure 5](#), and [Figure 6](#).

TYPICAL CHARACTERISTICS (P_{VIN} = V_{IN} = 5 V) ⁽¹⁾ ⁽²⁾

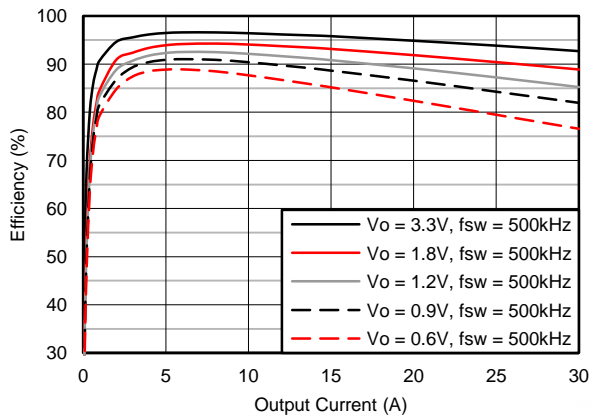


Figure 7. Efficiency vs. Output Current

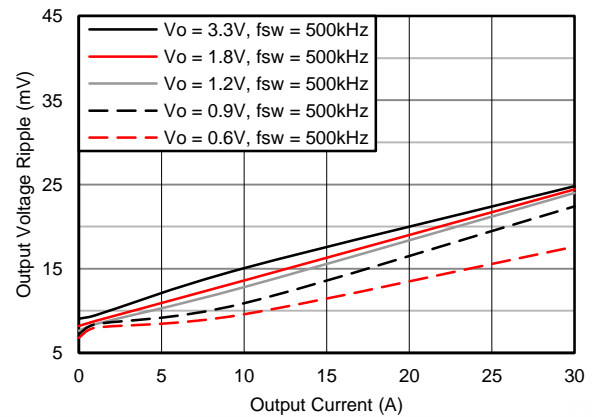


Figure 8. Voltage Ripple vs. Output Current

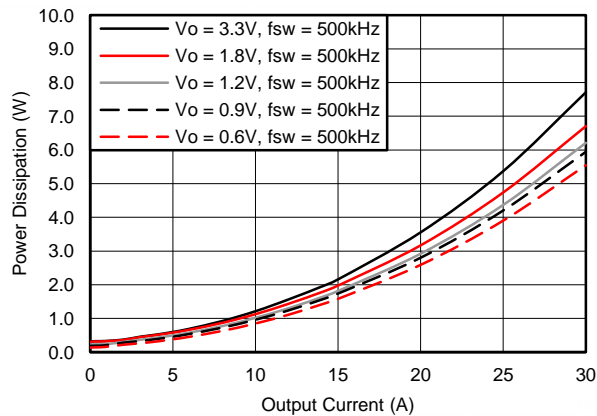


Figure 9. Power Dissipation vs. Output Current

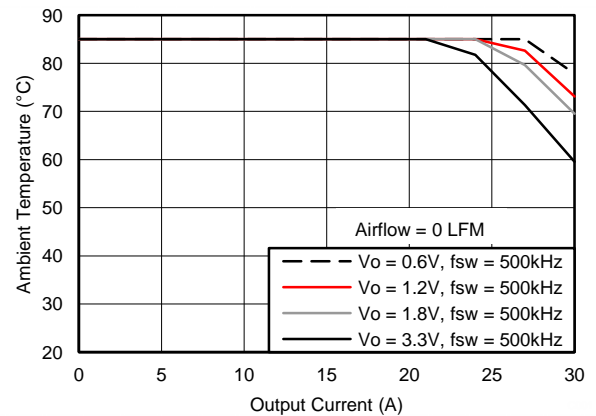


Figure 10. Safe Operating Area (0 LFM)

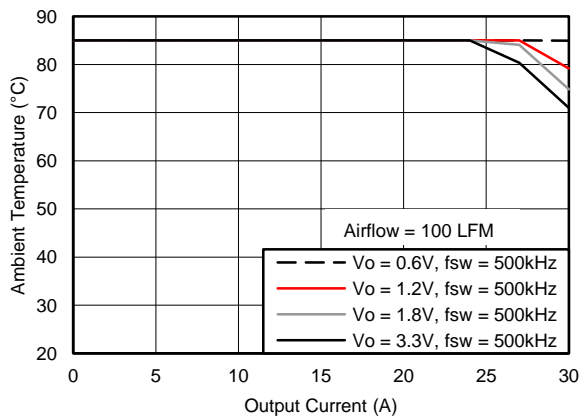


Figure 11. Safe Operating Area (100 LFM)

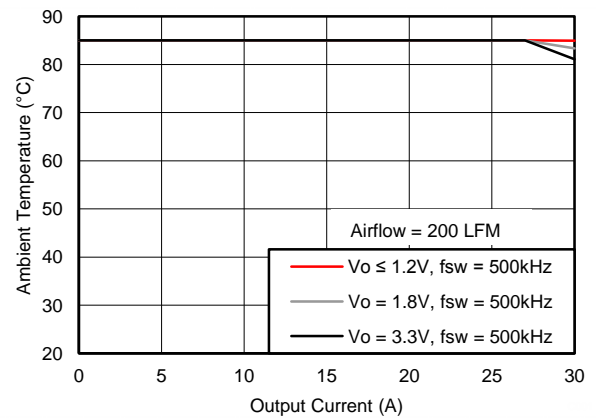


Figure 12. Safe Operating Area (200 LFM)

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 7](#), [Figure 8](#), and [Figure 9](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm six-layer PCB with 1 oz. copper. Applies to [Figure 10](#), [Figure 11](#), and [Figure 12](#).

APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

The V_{ADJ} control sets the output voltage of the LMZ31530. The output voltage adjustment range is from 0.6V to 3.6V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, and the connection of SENSE+ to V_{OUT}. The R_{SET} resistor must be connected directly between the V_{ADJ} (pin 13) and AGND (pin 9). The SENSE+ pin (pin 14) must be connected to V_{OUT} either at the load for improved regulation or at V_{OUT} of the device.

The LMZ31530 relies on a precision trimmed 0.6 V reference for the feedback voltage regulation and operates by regulating the valley of the voltage ripple appearing at the V_{ADJ} pin. The voltage ripple is a function of the input voltage and the output voltage, therefore the R_{SET} resistor will change based on the input voltage. [Table 1](#) gives the calculated external R_{SET} resistor for a number of common bus voltages for P_{VIN} of 12 V, 5 V, and 3.3 V. The recommended switching frequency is 500 kHz which can be configured by leaving the FREQ_SEL pin open. To adjust the frequency, see [Table 2](#).

Table 1. R_{SET} Resistor Values

V _{OUT} (V)	R _{SET} (Ω)			V _{OUT} (V)	R _{SET} (Ω)		
	P _{VIN} = 12 V	P _{VIN} = 5 V	P _{VIN} = 3.3 V		P _{VIN} = 12 V	P _{VIN} = 5 V	P _{VIN} = 3.3 V
0.60	open	open	open	2.15	566	563	560
0.65	18787	18681	18588	2.20	548	545	542
0.70	9024	8993	8966	2.25	532	528	525
0.75	5939	5923	5908	2.30	516	513	510
0.80	4427	4416	4406	2.35	502	498	495
0.85	3529	3521	3513	2.40	488	484	481
0.90	2934	2927	2921	2.45	475	471	468
0.95	2511	2505	2500	2.50	462	459	456
1.00	2195	2190	2185	2.55	451	447	444
1.05	1950	1945	1941	2.60	439	436	433
1.10	1754	1749	1745	2.65	429	425	422
1.15	1594	1589	1586	2.70	419	415	412
1.20	1460	1456	1453	2.75	409	405	402
1.25	1348	1344	1341	2.80	400	396	393
1.30	1251	1248	1244	2.85	391	387	384
1.35	1168	1164	1161	2.90	382	379	375
1.40	1095	1091	1088	2.95	374	370	367
1.45	1031	1027	1024	3.00	367	363	359
1.50	973	970	968	3.05	359	355	352
1.55	922	919	916	3.10	352	348	345
1.60	876	873	870	3.15	345	341	338
1.65	834	831	828	3.20	339	335	331
1.70	797	793	790	3.25	332	328	325
1.75	762	759	756	3.30	326	322	318
1.80	730	727	724	3.35	320	316	312
1.85	701	698	695	3.40	315	310	307
1.90	674	671	668	3.45	309	305	301
1.95	650	646	643	3.50	304	300	296
2.00	626	623	620	3.55	299	294	291
2.05	605	602	599	3.60	294	289	286
2.10	585	581	578				

Frequency Select

The LMZ31530 switching frequency can be selected from several values as shown in Table 2. To select a switching frequency, a resistor (R_{FREQ}) must be connected between the FREQ_SEL pin and either PGND or V5V (pin 61) as shown in Table 2. For all output voltages, the recommended switching frequency is 500 kHz which can be configured by leaving the FREQ_SEL pin open. Table 2 also shows the output voltage range for each frequency.

Table 2. Frequency Selection

Frequency Select (kHz)	R_{FREQ} (k Ω)	Connect To	V_{OUT} RANGE (V)	
			MIN	MAX
300	66	PGND	0.6	3.6
400	498	PGND	0.6	3.6
500	open	-	0.6	3.6
650	745	V5V	0.8	3.6
750	188	V5V	1.0	3.6
850	short	V5V	1.2	3.6

CAPACITOR RECOMMENDATIONS FOR THE LMZ31530 POWER SUPPLY

Capacitor Technologies

Electrolytic, Polymer-Electrolytic Capacitors

Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz. When using electrolytic capacitors, high-quality, polymer-electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Panasonic OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size.

Ceramic Capacitors

The performance of ceramic capacitors is most effective above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Panasonic POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Input Capacitor

The LMZ31530 requires a minimum input capacitance of 44 μF of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The input RMS ripple current is a function of the output current and the duty cycle for any application. The input capacitor must be rated for the application's RMS ripple current. Table 3 includes a preferred list of capacitors by vendor.

Output Capacitor

The required output capacitance of the LMZ31530 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 100 μF of ceramic type. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 3 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 4 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 3 includes a preferred list of capacitors by vendor.

Table 3. Recommended Input/Output Capacitors⁽¹⁾

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (μF)	ESR ⁽²⁾ (mΩ)
Murata	X5R	GRM32ER61E226K	25	22	2
TDK	X5R	C3216X5R1E476M	25	47	2
TDK	X5R	C3216X5R1C476M	16	47	2
Murata	X5R	GRM32ER61C476M	16	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Panasonic	EEH-ZA	EEH-ZA1E101XP	25	100	30
Kemet	T520	T520V107M010ASE025	10	100	25
Panasonic	POSCAP	6TPE100MI	6.3	100	25
Panasonic	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Panasonic	POSCAP	2TPF330M6	2.0	330	6
Panasonic	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**

Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.

(2) Maximum ESR @ 100kHz, 25°C.

Transient Response

The LMZ31530 is designed to have an ultra-fast load step response with minimal output capacitance. [Table 4](#) shows the voltage deviation and recovery time for several different transient conditions. Several waveforms are shown in [Transient Waveforms](#)⁽³⁾.

Table 4. Output Voltage Transient Response

C_{IN1} = 3 x 47 μF CERAMIC						
V _{OUT} (V)	V _{IN} (V)	C _{OUT1} Ceramic	C _{OUT2} BULK	VOLTAGE DEVIATION (mV)		RECOVERY TIME (μs)
				10 A LOAD STEP, (1 A/μs)	15 A LOAD STEP, (1 A/μs)	
0.6	5	500 μF	-	15	18	35
	12	500 μF	-	15	20	35
0.9	5	500 μF	-	15	18	40
		500 μF	470 μF	12	15	40
	12	500 μF	-	20	25	40
		500 μF	470 μF	16	22	40
1.2	5	500 μF	-	20	25	40
		500 μF	330 μF	15	22	40
	12	500 μF	-	20	25	40
		500 μF	330 μF	16	24	40
1.8	5	500 μF	-	20	30	40
		500 μF	330 μF	16	25	40
	12	500 μF	-	20	30	40
		500 μF	330 μF	16	25	45
3.3	5	500 μF	-	25	40	50
	12	500 μF	-	25	35	50

(3) Device configured for FCCM mode of operation, (pin 3 connected to pin 19).

Transient Waveforms ⁽¹⁾

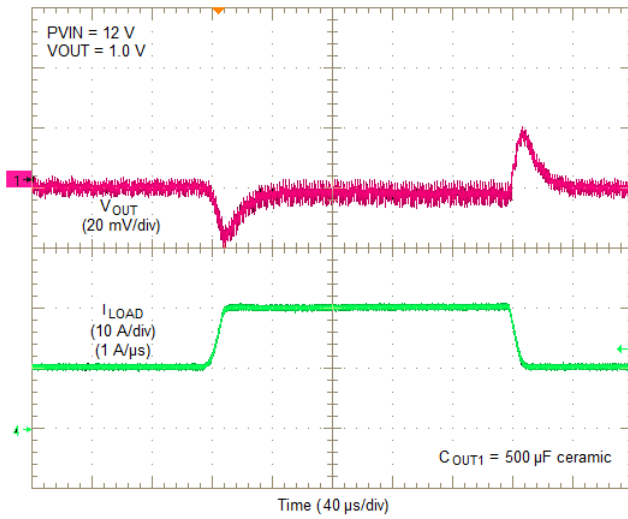


Figure 13. $PV_{IN} = 12V$, $V_{OUT} = 1.0V$, 10A Load Step

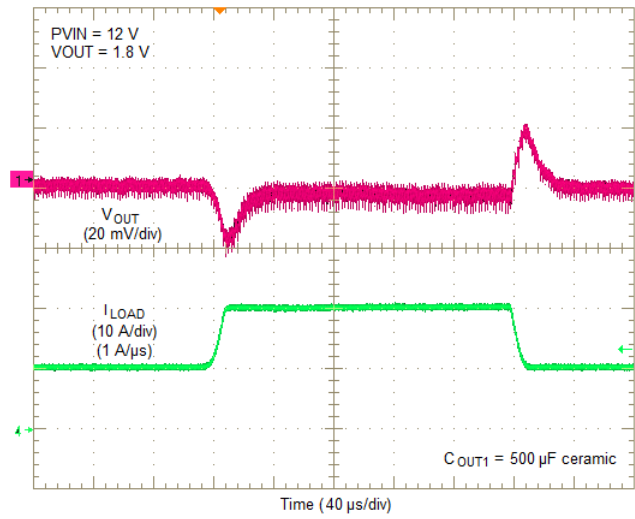


Figure 14. $PV_{IN} = 12V$, $V_{OUT} = 1.8V$, 10A Load Step

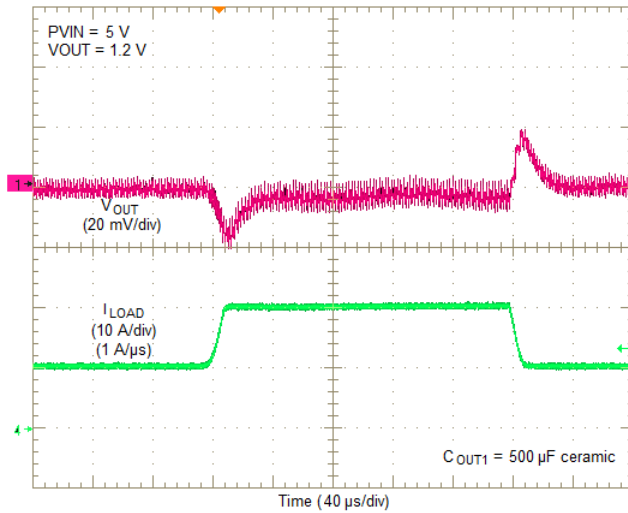


Figure 15. $PV_{IN} = 5V$, $V_{OUT} = 1.2V$, 10A Load Step

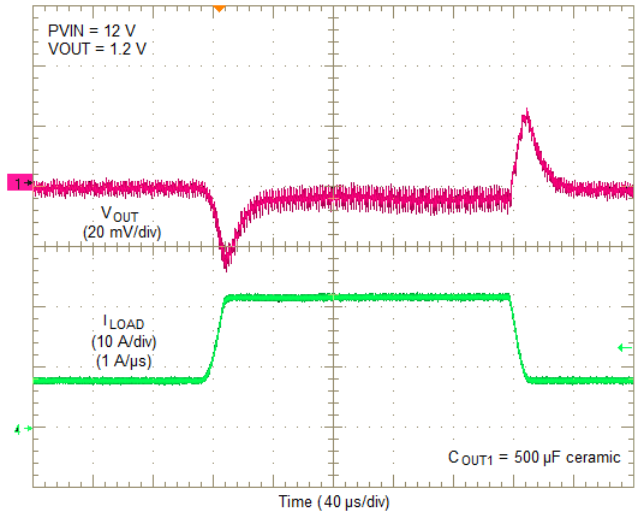


Figure 16. $PV_{IN} = 12V$, $V_{OUT} = 1.2V$, 5A Load Step

(1) Device configured for FCCM mode of operation, (pin 3 connected to pin 19).

Application Schematics

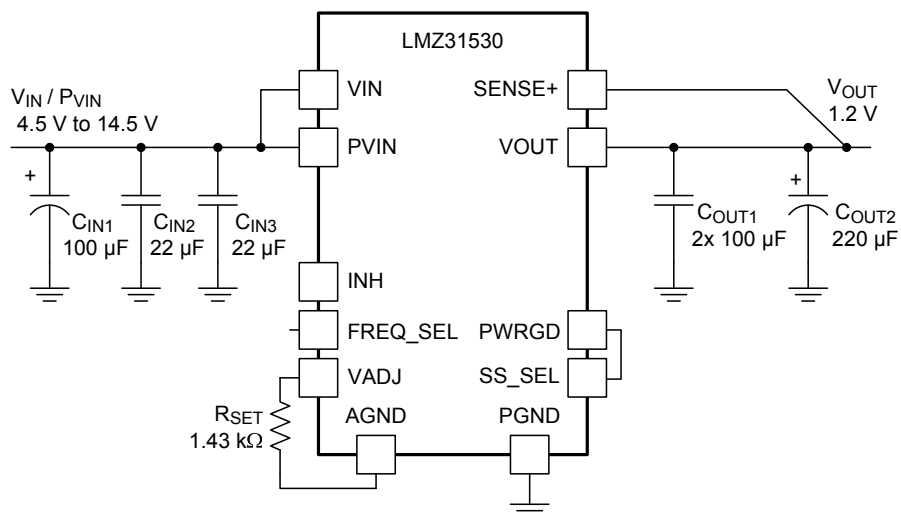


Figure 17. Typical Schematic
PVIN = VIN = 4.5 V to 14.5 V, VOUT = 1.2 V

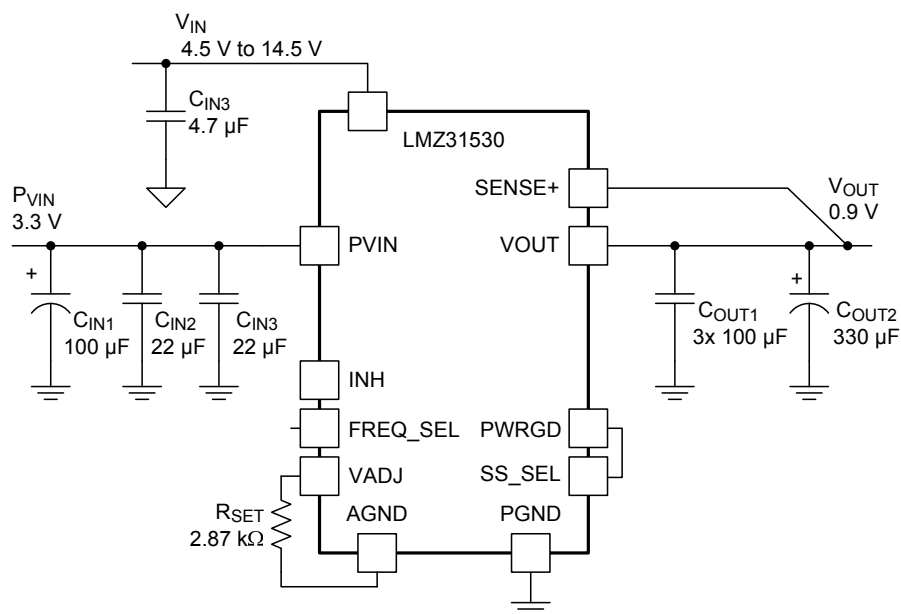


Figure 18. Typical Schematic
PVIN = 3.3 V, VIN = 4.5 V to 14.5 V, VOUT = 0.9 V

VIN and PVIN Input Voltage

The LMZ31530 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 14.5 V. If using the VIN pin separately from the PVIN pin, the VIN pin must be greater than 4.5 V, and the PVIN pin can range from as low as 3.0 V to 14.5 V. When operating from a split rail, it is recommended to supply VIN from 5 V to 12 V, for best performance.

3.3 V PVIN Operation

Applications operating from a PVIN of 3.3 V must provide at least 4.5 V for VIN. It is recommended to supply VIN from 5 V to 12 V, for best performance. See application note, [SNVA692](#) for help creating 5 V from 3.3 V using a small, simple charge pump device.

Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 90% and 115% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 k Ω and 100 k Ω to a voltage source that is less than 7 V. An internal 100 k Ω pull-up resistor is provided internal to the device between the PWRGD pin (pin 19) and PWRGD_PU pin (pin 18). The PWRGD_PU pin can be connected to a voltage source less than 7 V or connected directly to V5V (pin 61), which is an internal 5V regulator. The PWRGD pin is in a defined state once VIN is greater than 1.0 V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 90% or greater than 115% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted or the INH pin is pulled low.

Slow Start (SS_SEL)

Connecting the SS_SEL pin to PWRGD or PGND sets the slow start interval of approximately 0.7 ms. The connection to either PWRGD or PGND determines the mode of the LMZ31530 as described in [Auto-Skip Eco-Mode™ / Forced Continuous Conduction Mode](#). Adding a resistor between SS_SEL pin and PWRGD or PGND increases the slow start time. Increasing the slow start time will reduce inrush current. [Table 5](#) shows a resistor connected between SS_SEL pin and PWRGD to select FCCM and [Figure 20](#) shows a resistor between SS_SEL pin and PGND to select Auto-skip mode. See [Table 5](#) below for SS resistor values and timing interval.

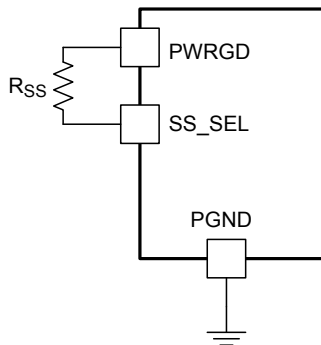


Figure 19. Slow-Start Resistor (R_{SS}) in FCCM

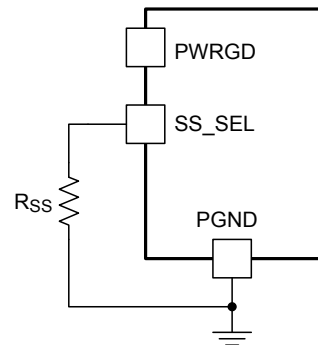


Figure 20. Slow-Start Resistor (R_{SS}) in Auto-skip Mode

Table 5. Slow-Start Resistor Values and Slow-Start Time

R_{SS} (k Ω)	short	61.9	161	436
SS Time (msec)	0.7	1.4	2.8	5.6

Auto-Skip Eco-Mode™ / Forced Continuous Conduction Mode

Auto-skip Eco-mode or Forced Continuous Conduction Mode (FCCM) can be selected using the SS_SEL pin (pin 3). Connect the SS_SEL pin to PGND to select Auto-skip Eco-mode or to the PWRGD pin to select FCCM.

In Auto-skip Eco-mode, the LMZ31530 automatically reduces the switching frequency at light load conditions to maintain high efficiency. In FCCM, the controller keeps continuous conduction mode in light load condition and the switching frequency is kept almost constant over the entire load range. Transient performance is best in FCCM.

Power-Up Characteristics

When configured as shown in the front page schematic, the LMZ31530 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. Figure 21 shows the start-up waveforms for a LMZ31530, operating from a 12-V input (PVIN=VIN) and with the output voltage adjusted to 1.8 V. Figure 22 shows the start-up waveforms for a LMZ31530 starting up into a pre-biased output voltage. The waveforms were measured with a 15-A constant current load.

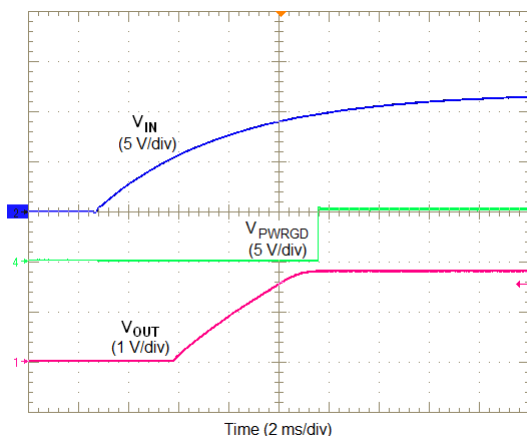


Figure 21. Start-Up Waveforms

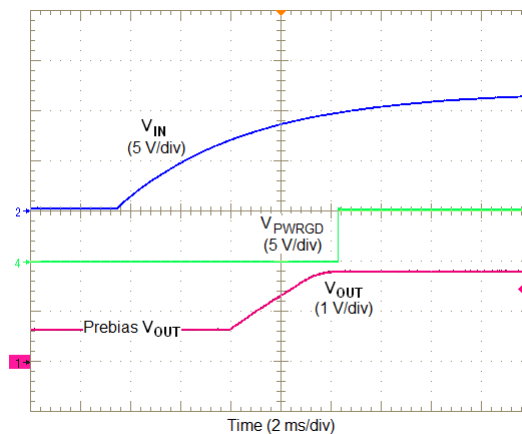


Figure 22. Start-up into Pre-bias

Pre-Biased Start-Up

The LMZ31530 has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During pre-biased startup, the low-side MOSFET does not turn on until the high-side MOSFET has started switching. The high-side MOSFET does not start switching until the slow start voltage exceeds the voltage on the VADJ pin. Refer to Figure 22.

Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 23 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 24. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 25. The waveforms were measured with a 12-A constant resistance load.

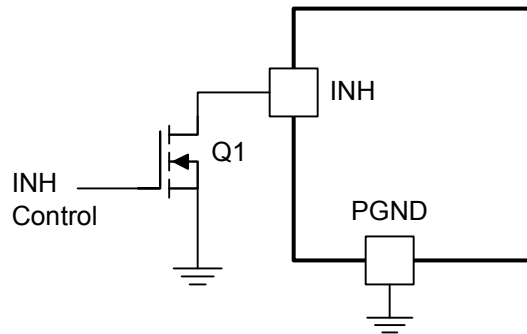


Figure 23. Typical Inhibit Control

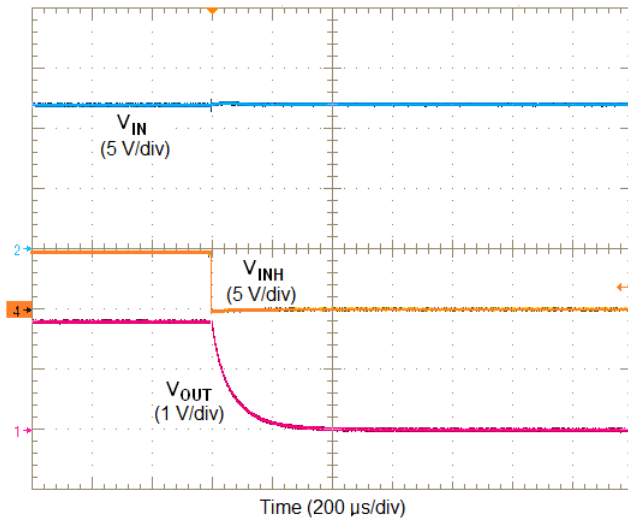


Figure 24. Inhibit Turn-Off

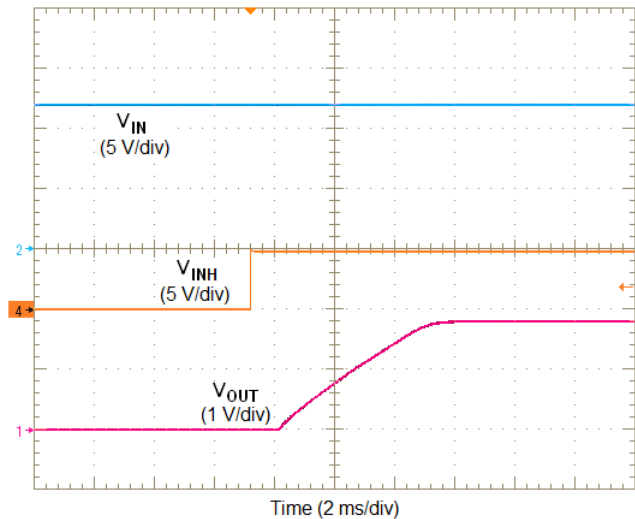


Figure 25. Inhibit Turn-On

Overcurrent Protection

For protection against load faults, the LMZ31530 incorporates cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period in that the inductor current is larger than the overcurrent trip level. In cycle-by-cycle mode, applying a load that exceeds the regulator's overcurrent threshold limits the output current and reduces the output voltage as shown in Figure 26. If the overcurrent condition remains and the output voltage drops below 70% of the set-point, the LMZ31530 shuts down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in Figure 26. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 27.

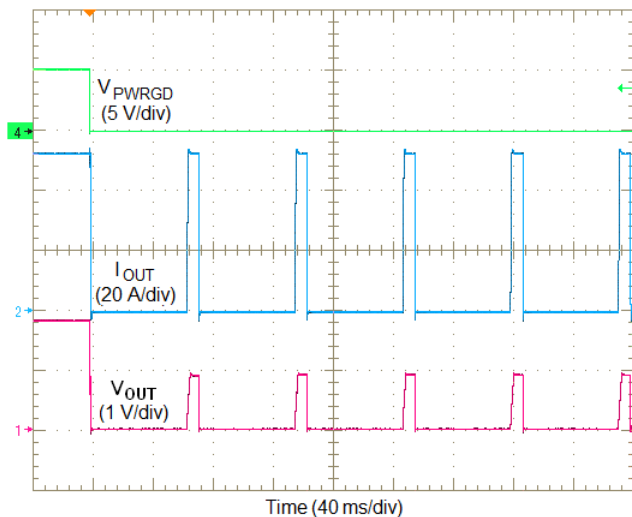


Figure 26. Overcurrent Limiting (Hiccup)

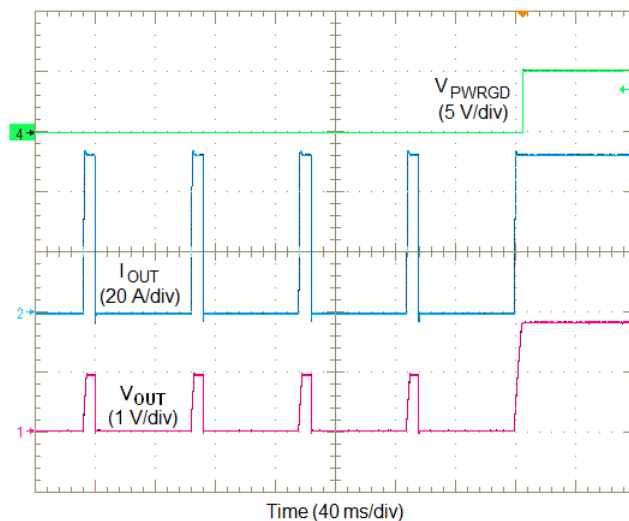


Figure 27. Removal of Overcurrent (Hiccup)

Current Limit (ILIM) Adjust

The current limit of this device can be adjusted lower by connecting a resistor, R_{ILIM} , between the ILIM pin (pin 6) and PGND. To adjust the typical current limit threshold, as listed in the electrical characteristics table, refer to Table 6.

Table 6. Current Limit Adjust Resistor

Current Limit Reduction	$R_{ILIM}(k\Omega)$
10 %	825
20 %	487
30 %	324

Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 145°C typically. The device reinitiates the power up sequence when the junction temperature drops below 135°C typically.

Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. [Figure 28](#) thru [Figure 33](#), shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. AGND should only be used as the return for R_{SET} .
- Place R_{SET} , R_{FREQ} , and R_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

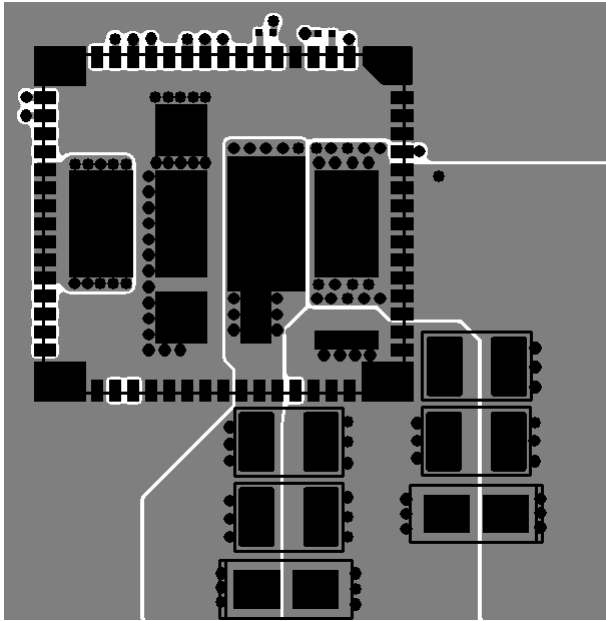


Figure 28. Typical Top Layer Layout

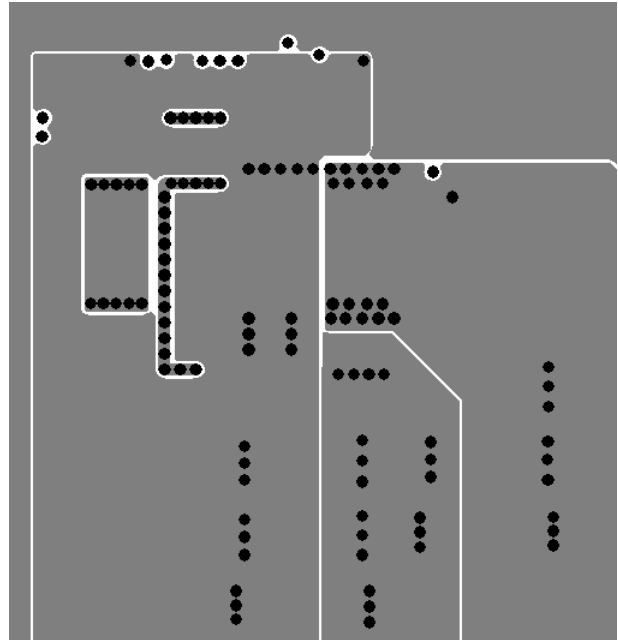


Figure 29. Typical Layer 2 Layout

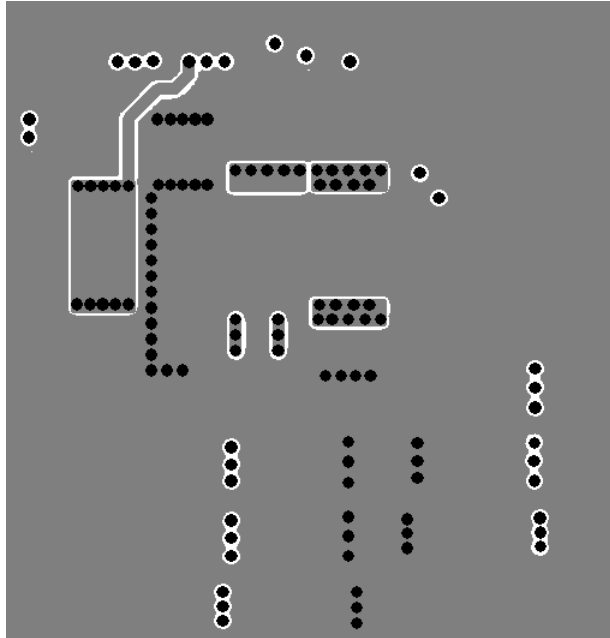


Figure 30. Typical Layer 3 Layout

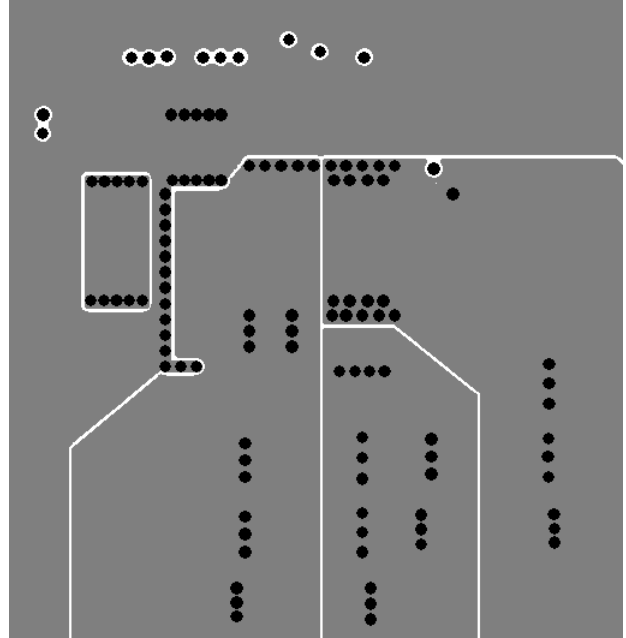


Figure 31. Typical Layer 4 Layout

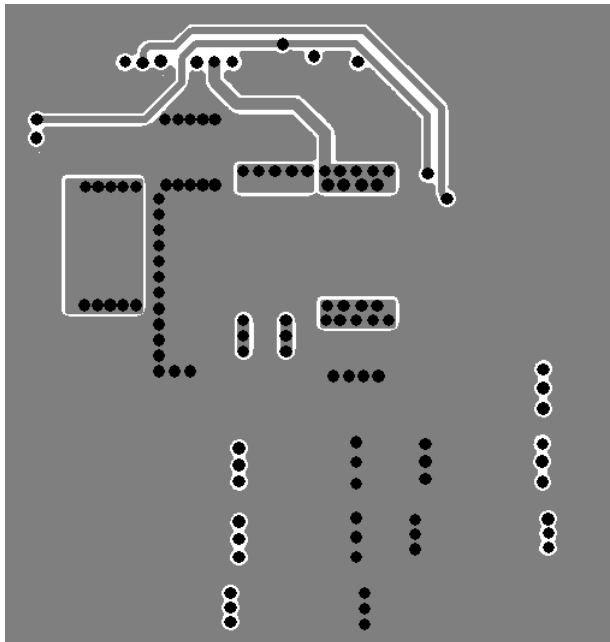


Figure 32. Typical Layer 5 Layout

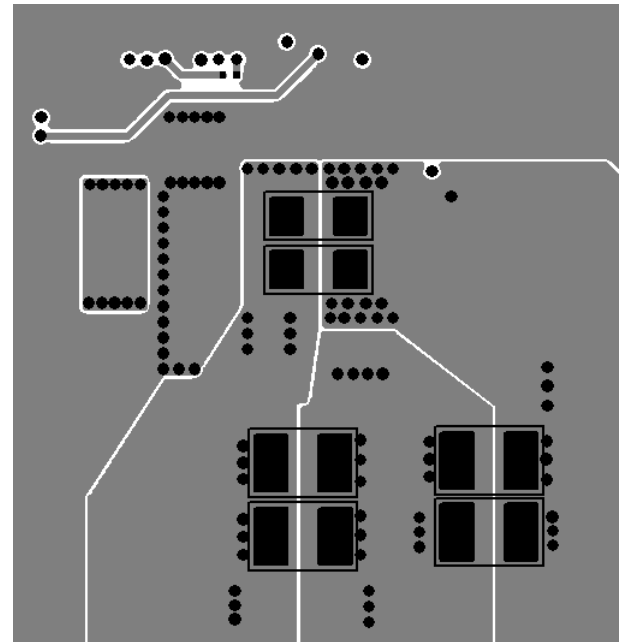


Figure 33. Typical Bottom Layer Layout

EMI

The LMZ31530 is compliant with EN55022 Class A radiated emissions. [Figure 34](#) and [Figure 35](#) show typical examples of radiated emissions plots for the LMZ31530 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

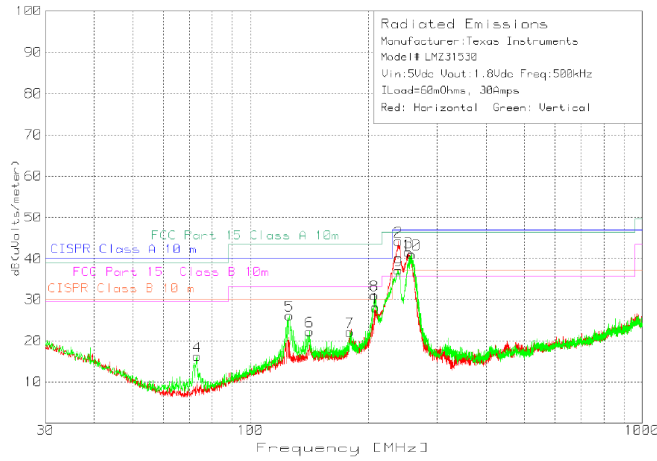


Figure 34. Radiated Emissions 5-V Input, 1.8-V Output, 30-A Load (EN55022 Class A)

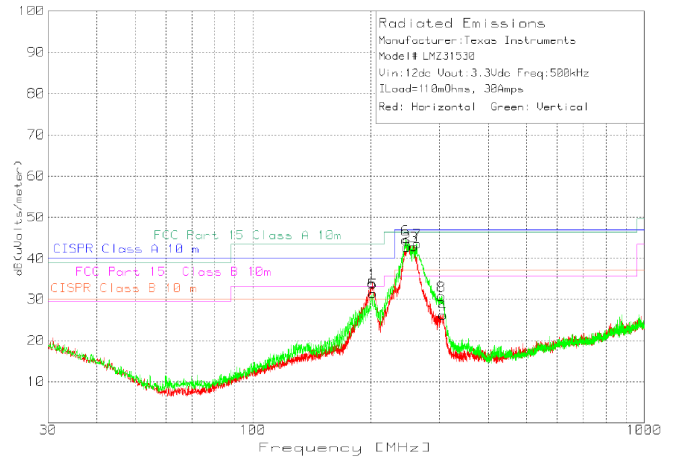


Figure 35. Radiated Emissions 12-V Input, 3.3-V Output, 30-A Load (EN55022 Class A)

REVISION HISTORY


Changes from Revision A (December 2013) to Revision B **Page**

- Added additional capacitors to the recommended capacitor table 13
-

Changes from Original (October 2013) to Revision A **Page**

- Changed 将状态从预览改为生产 1
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ31530RLGT	ACTIVE	BQFN	RLG	72	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	(53355DQP ~ LMZ31530)	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

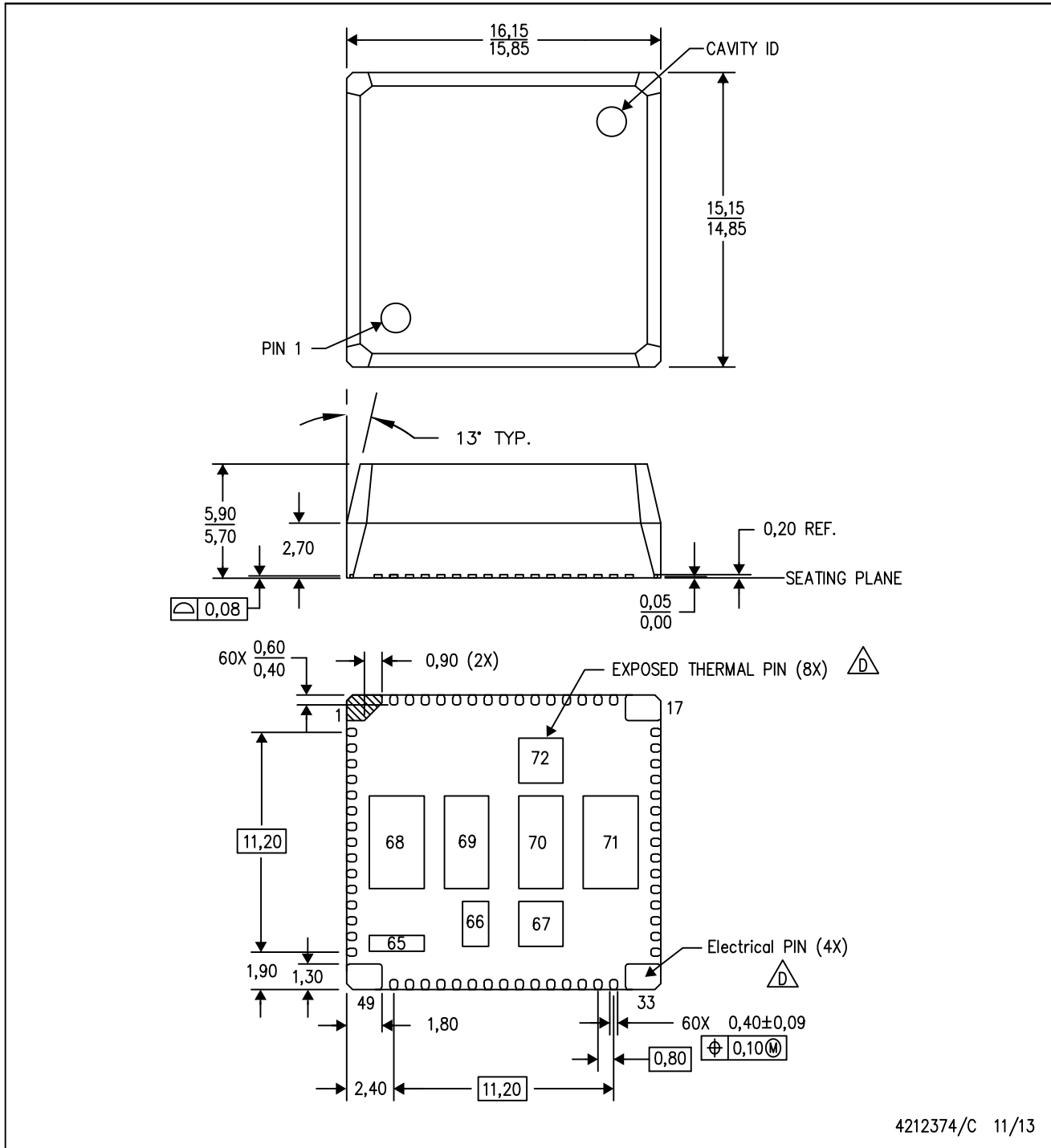
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



RLG (R-PB4QFN-N72)

PLASTIC QUAD FLATPACK NO-LEAD



4212374/C 11/13

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. Quad Flatpack, No-leads (QFN) package configuration.

-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane..

有关 TI 设计信息和资源的重要通知

德州仪器 (TI) 公司提供的技术、应用或其他设计建议、服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用；如果您（个人，或如果是代表贵公司，则为贵公司）以任何方式下载、访问或使用了任何特定的 TI 资源，即表示贵方同意仅为该等目标，按照本通知的条款进行使用。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。

您理解并同意，在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，以及您的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。您就您的应用声明，您具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。您同意，在使用或分发包含 TI 产品的任何应用前，您将彻底测试该等应用和该等应用所用 TI 产品的功能。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

您只有在为开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对 TI 资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无复发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。

TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为您辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

您同意向 TI 及其代表全额赔偿因您不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

本通知适用于 TI 资源。另有其他条款适用于某些类型的材料、TI 产品和服务的使用和采购。这些条款包括但不限于适用于 TI 的半导体产品 (<http://www.ti.com/sc/docs/stdterms.htm>)、[评估模块](http://www.ti.com/sc/docs/sampters.htm)和样品 (<http://www.ti.com/sc/docs/sampters.htm>) 的标准条款。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司