

LMH6645/46/47 2.7V, 650µA, 55MHz, Rail-to-Rail Input and Output Amplifiers with Shutdown Option

Check for Samples: [LMH6645](#), [LMH6646](#), [LMH6647](#)

FEATURES

 $(V_S = 2.7V, T_A = 25^\circ C, R_L = 1k\Omega \text{ to } V^+/2, A_V = +1)$. Typical values unless specified).

- **-3dB BW 55MHz**
- **Supply Voltage Range 2.5V to 12V**
- **Slew Rate 22V/µs**
- **Supply Current 650µA/channel**
- **Output Short Circuit Current 42mA**
- **Linear Output Current ±20mA**
- **Input Common Mode Voltage 0.3V Beyond Rails**
- **Output Voltage Swing 20mV from Rails**
- **Input Voltage Noise 17nV/√Hz**
- **Input Current Noise 0.75pA/√Hz**

APPLICATIONS

- **Active filters**
- **High speed portable devices**
- **Multiplexing applications (LMH6647)**
- **Current sense buffer**
- **High speed transducer amp**

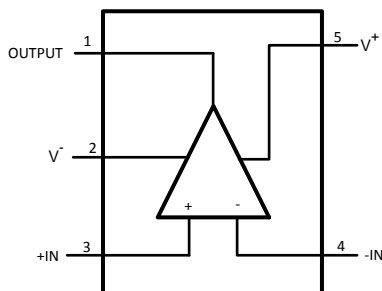
DESCRIPTION

The LMH™6645 (single) and LMH6646 (dual), rail-to-rail input and output voltage feedback amplifiers, offer high speed (55MHz), and low voltage operation (2.7V) in addition to micro-power shutdown capability (LMH6647, single).

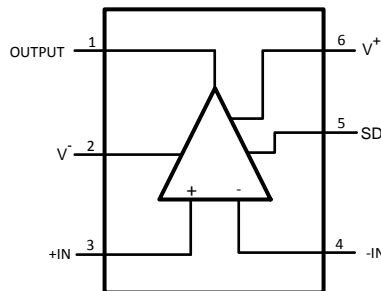
Input common mode voltage range exceeds either supply by 0.3V, enhancing ease of use in multitude of applications where previously only inferior devices could be used. Output voltage range extends to within 20mV of either supply rails, allowing wide dynamic range especially in low voltage applications. Even with low supply current of 650µA/amplifier, output current capability is kept at a respectable ±20mA for driving heavier loads. Important device parameters such as BW, Slew Rate and output current are kept relatively independent of the operating supply voltage by a combination of process enhancements and design architecture.

In portable applications, the LMH6647 provides shutdown capability while keeping the turn-off current to less than 50µA. Both turn-on and turn-off characteristics are well behaved with minimal output fluctuations during transitions. This allows the part to be used in power saving mode, as well as multiplexing applications. Miniature packages (SOT-23, VSSOP-8, and SOIC-8) are further means to ease the adoption of these low power high speed devices in applications where board area is at a premium.

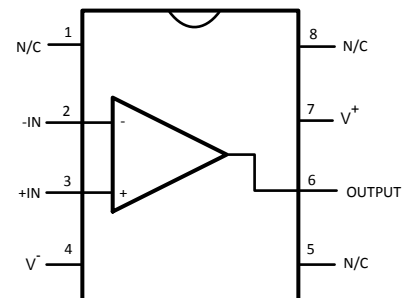
Connection Diagram



**Figure 1. SOT-23-5 (LMH6645)
Package Number DBV0005A
Top View**



**Figure 2. SOT-23-6 (LMH6647)
Package Number DBV0006A
Top View**



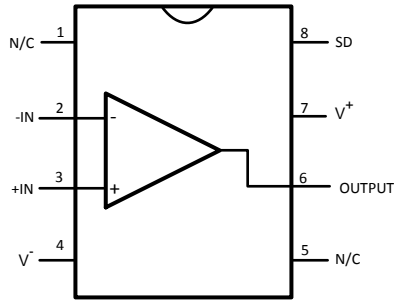
**Figure 3. SOIC-8 (LMH6645)
Package Number D0008A
Top View**



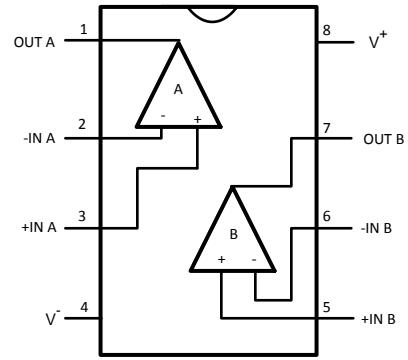
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**Figure 4. SOIC-8 (LMH6647)
Package Number D0008A
Top View**



**Figure 5. SOIC-8 and VSSOP-8 (LMH6646)
Package Numbers D0008A and DGK0008A
Top View**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance	Human Body	2KV (3)
	Machine Model	200V (4)
V_{IN} Differential		$\pm 2.5V$
Output Short Circuit Duration		See (5), (6)
Supply Voltage ($V^+ - V^-$)		12.6V
Voltage at Input/Output pins		$V^+ +0.8V, V^- -0.8V$
Storage Temperature Range		$-65^\circ C$ to $+150^\circ C$
Junction Temperature (7)		$+150^\circ C$
Soldering Information	Infrared or Convection (20 sec)	$235^\circ C$
	Wave Soldering (10 sec)	$260^\circ C$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human body model, 1.5k Ω in series with 100pF.
- (4) Machine Model, 0 Ω in series with 200pF.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 $^\circ C$.
- (6) Output short circuit duration is infinite for $V_S < 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.
- (7) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Supply Voltage ($V^+ - V^-$)		2.5V to 12V
Temperature Range (2)		$-40^\circ C$ to $+85^\circ C$
Package Thermal Resistance (2) (θ_{JA})	SOT-23-5	265 $^\circ C/W$
	SOT-23-6	265 $^\circ C/W$
	SOIC-8	190 $^\circ C/W$
	VSSOP-8	235 $^\circ C/W$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$, and $R_f = 2\text{k}\Omega$, and $R_L = 1\text{k}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	-3dB BW	$A_V = +1$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$, $V_{\text{CM}} = 0.7\text{V}$	40	55		MHz
e_n	Input-Referred Voltage Noise	$f = 100\text{kHz}$		17		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		25		
i_n	Input-Referred Current Noise	$f = 100\text{kHz}$		0.75		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		1.20		
CT Rej.	Cross-Talk Rejection (LMH6646 only)	$f = 5\text{MHz}$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$		47		dB
SR	Slew Rate	$A_V = -1$, $V_O = 2V_{\text{PP}}$ See (3), (4)	15	22		$\text{V}/\mu\text{s}$
T_{ON}	Turn-On Time (LMH6647 only)			250		ns
T_{OFF}	Turn-Off Time (LMH6647 only)			560		ns
TH_{SD}	Shutdown Threshold (LMH6647 only)	$I_S \leq 50\mu\text{A}$		1.95	2.30	V
I_{SD}	Shutdown Pin Input Current (LMH6647 only)	See (5)		-20		μA
V_{OS}	Input Offset Voltage	$0\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$	-3 -4	± 1	3 4	mV
TC V_{OS}	Input Offset Average Drift	See (6)		± 5		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{\text{CM}} = 2.5\text{V}$ (5)		0.40	2 2.2	μA
		$V_{\text{CM}} = 0.5\text{V}$ (5)		-0.68	-2 -2.2	
I_{OS}	Input Offset Current	$0\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$		1	500	nA
R_{IN}	Common Mode Input Resistance			3		$\text{M}\Omega$
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50\text{dB}$		-0.5	-0.3 -0.1	V
			3.0 2.8	3.2		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 2.7V	46	77		dB
		V_{CM} Stepped from 0V to 1.55V	58	76		
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.35\text{V}$ to 2.35V	76 74	87		dB
V_O	Output Swing High	$R_L = 1\text{k}$ to $V^+/2$	2.55	2.66		V
		$R_L = 10\text{k}$ to $V^+/2$		2.68		
	Output Swing Low	$R_L = 1\text{k}$ to $V^+/2$		40	150	mV
		$R_L = 10\text{k}$ to $V^+/2$		20		

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Guaranteed based on characterization only.

(5) Positive current corresponds to current flowing into the device.

(6) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$, and $R_f = 2\text{k}\Omega$, and $R_L = 1\text{k}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to V^- $V_{\text{ID}} = 200\text{mV}$ (7)(8)		43		mA
		Sinking to V^+ $V_{\text{ID}} = -200\text{mV}$ (7)(8)		42		
I_{OUT}	Output Current	$V_{\text{OUT}} = 0.5\text{V}$ from rails		± 20		mA
PSRR	Power Supply Rejection Ratio	$V^+ = 2.7\text{V}$ to 3.7V or $V^- = 0\text{V}$ to -1V	75	83		dB
I_{S}	Supply Current (per channel)	Normal Operation		650	1250	μA
		Shutdown Mode (LMH6647 only)		15	50	

(7) Short circuit test is a momentary test.

(8) Output short circuit duration is infinite for $V_{\text{S}} < 6\text{V}$ at room temperature and below. For $V_{\text{S}} > 6\text{V}$, allowable short circuit duration is 1.5ms.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$, and $R_f = 2\text{k}\Omega$, and $R_L = 1\text{k}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	-3dB BW	$A_V = +1$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$	40	55		MHz
e_n	Input-Referred Voltage Noise	$f = 100\text{kHz}$		17		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		25		
i_n	Input-Referred Current Noise	$f = 100\text{kHz}$		0.75		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		1.20		
CT Rej.	Cross-Talk Rejection (LMH6646 only)	$f = 5\text{MHz}$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$		47		dB
SR	Slew Rate	$A_V = -1$, $V_O = 2\text{V}_{\text{PP}}$ See (3), (4)	15	22		$\text{V}/\mu\text{s}$
T_{ON}	Turn-On Time (LMH6647 only)			210		ns
T_{OFF}	Turn-Off Time (LMH6647 only)			500		ns
TH_{SD}	Shutdown Threshold (LMH6647 only)	$I_{\text{S}} \leq 50\mu\text{A}$		4.25	4.60	V
I_{SD}	Shutdown Pin Input Current (LMH6647 only)	See (5)		-20		μA
V_{OS}	Input Offset Voltage	$0\text{V} \leq V_{\text{CM}} \leq 5\text{V}$	-3 -4	± 1	3 4	mV
TC V_{OS}	Input Offset Average Drift	See (6)		± 5		$\mu\text{V}/\text{C}$
I_{B}	Input Bias Current	$V_{\text{CM}} = 4.8\text{V}$ (5)		+0.36	+2 -2.2	μA
		$V_{\text{CM}} = 0.5\text{V}$ (5)		-0.68	-2 -2.2	
I_{OS}	Input Offset Current	$0\text{V} \leq V_{\text{CM}} \leq 5\text{V}$		1	500	nA
R_{IN}	Common Mode Input Resistance			3		M Ω
C_{IN}	Common Mode Input Capacitance			2		pF

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Guaranteed based on characterization only.

(5) Positive current corresponds to current flowing into the device.

(6) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$, and $R_f = 2\text{k}\Omega$, and $R_L = 1\text{k}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50\text{dB}$		-0.5	-0.3 -0.1	V
			5.3 5.1	5.5		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 5V	56	82		dB
		V_{CM} Stepped from 0V to 3.8V	66	85		
A_{VOL}	Large Signal Voltage Gain	$V_O = 1.5\text{V}$ to 3.5V	76 74	85		dB
V_O	Output Swing High	$R_L = 1\text{k}$ to $V^+/2$	4.80	4.95		V
		$R_L = 10\text{k}$ to $V^+/2$		4.98		
	Output Swing Low	$R_L = 1\text{k}$ to $V^+/2$		50	200	mV
		$R_L = 10\text{k}$ to $V^+/2$		20		
I_{SC}	Output Short Circuit Current	Sourcing to V^- $V_{\text{ID}} = 200\text{mV}$ (7)(8)		55		mA
		Sinking to V^+ $V_{\text{ID}} = -200\text{mV}$ (7)(8)		53		
I_{OUT}	Output Current	$V_{\text{OUT}} = 0.5\text{V}$ From rails		± 20		mA
PSRR	Power Supply Rejection Ratio	$V^+ = 5\text{V}$ to 6V or $V^- = 0\text{V}$ to -1V	75	95		dB
I_S	Supply Current (per channel)	Normal Operation		700	1400	μA
		Shutdown Mode (LMH6647 only)		10	50	

(7) Short circuit test is a momentary test.

(8) Output short circuit duration is infinite for $V_S < 6\text{V}$ at room temperature and below. For $V_S > 6\text{V}$, allowable short circuit duration is 1.5ms.

$\pm 5\text{V}$ Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_O = 0\text{V}$, $R_f = 2\text{k}\Omega$, and $R_L = 1\text{k}\Omega$ to GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	-3dB BW	$A_V = +1$, $V_{\text{OUT}} = 200\text{mV}_{\text{PP}}$	40	55		MHz
e_n	Input-Referred Voltage Noise	$f = 100\text{kHz}$		17		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		25		
i_n	Input-Referred Current Noise	$f = 100\text{kHz}$		0.75		$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		1.20		
CT Rej.	Cross-Talk Rejection (LMH6646 only)	$f = 5\text{MHz}$, Receiver: $R_f = R_g = 510\Omega$, $A_V = +2$		47		dB
SR	Slew Rate	$A_V = -1$, $V_O = 2\text{V}_{\text{PP}}$ (3)	15	22		$\text{V}/\mu\text{s}$
T_{ON}	Turn-On Time (LMH6647 only)			200		ns
T_{OFF}	Turn-Off Time (LMH6647 only)			700		ns
TH_{SD}	Shutdown Threshold (LMH6647 only)	$I_S \leq 50\mu\text{A}$		4.25	4.60	V
I_{SD}	Shutdown Pin Input Current (LMH6647 only)	See (4)		-20		μA
V_{OS}	Input Offset Voltage	$-5\text{V} \leq V_{\text{CM}} \leq 5\text{V}$	-3 -4	± 1	3 4	mV
TC V_{OS}	Input Offset Average Drift	See (5)		± 5		$\mu\text{V}/^\circ\text{C}$

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm.

(3) Slew rate is the average of the rising and falling slew rates.

(4) Positive current corresponds to current flowing into the device.

(5) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = -5\text{V}$, $V_{\text{CM}} = V_O = 0\text{V}$, $R_f = 2\text{k}\Omega$, and $R_L = 1\text{k}\Omega$ to GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_B	Input Bias Current	$V_{\text{CM}} = 4.8\text{V}$ (4)		+0.40	+2 +2.2	μA
		$V_{\text{CM}} = -4.5\text{V}$ (4)		-0.65	-2 -2.2	
I_{OS}	Input Offset Current	$-5\text{V} \leq V_{\text{CM}} \leq 5\text{V}$		3	500	nA
R_{IN}	Common Mode Input Resistance			3		M Ω
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR $\geq 50\text{dB}$		-5.5	-5.3 -5.1	V
				5.3 5.1	5.5	
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from -5V to 5V	60	84		dB
		V_{CM} Stepped from -5V to 3.5V	66	104		
A_{VOL}	Large Signal Voltage Gain	$V_O = -2\text{V}$ to 2V	76 74	85		dB
V_O	Output Swing High	$R_L = 1\text{k}\Omega$	4.70	4.92		V
		$R_L = 10\text{k}\Omega$		4.97		
	Output Swing Low	$R_L = 1\text{k}\Omega$		-4.93	-4.70	V
		$R_L = 10\text{k}\Omega$		-4.98		
I_{SC}	Output Short Circuit Current	Sourcing to V^- $V_{\text{ID}} = 200\text{mV}$ (6)(7)		66		mA
		Sinking to V^+ $V_{\text{ID}} = -200\text{mV}$ (6)(7)		61		
I_{OUT}	Output Current	$V_{\text{OUT}} = 0.5\text{V}$ from rails		± 20		mA
PSRR	Power Supply Rejection Ratio	$V^+ = 5\text{V}$ to 6V or $V^- = -5\text{V}$ to -6V	76	95		dB
I_S	Supply Current (per channel)	Normal Operation		725	1600	μA
		Shutdown Mode (LMH6647 only)		10	50	

(6) Short circuit test is a momentary test.

(7) Output short circuit duration is infinite for $V_S < 6\text{V}$ at room temperature and below. For $V_S > 6\text{V}$, allowable short circuit duration is 1.5ms.

Typical Performance Characteristics

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

Closed Loop Frequency Response for Various Temperature

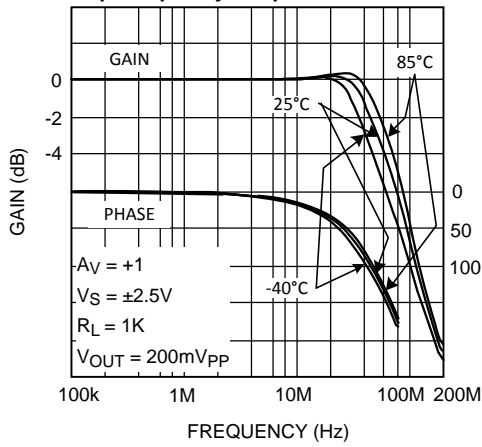


Figure 6.

Frequency Response for Various Av

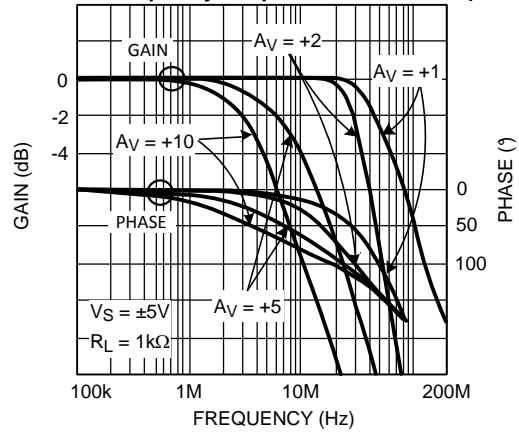


Figure 7.

Open Loop Gain/Phase vs. Frequency for Various Temperature

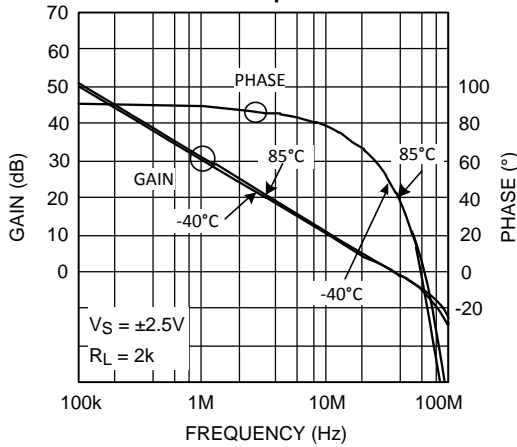


Figure 8.

THD vs. Output Swing

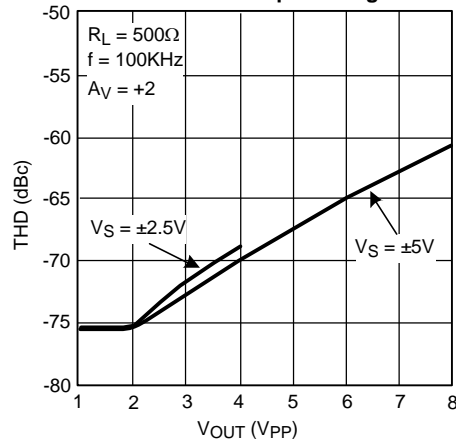


Figure 9.

THD vs. Output Swing

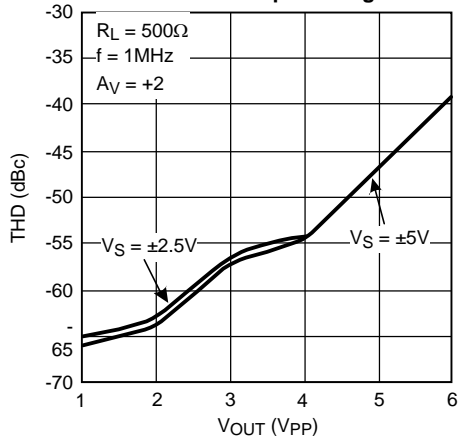


Figure 10.

Output Swing vs. Frequency

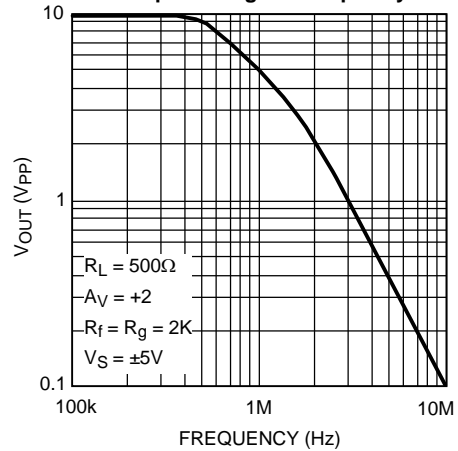


Figure 11.

Typical Performance Characteristics (continued)

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

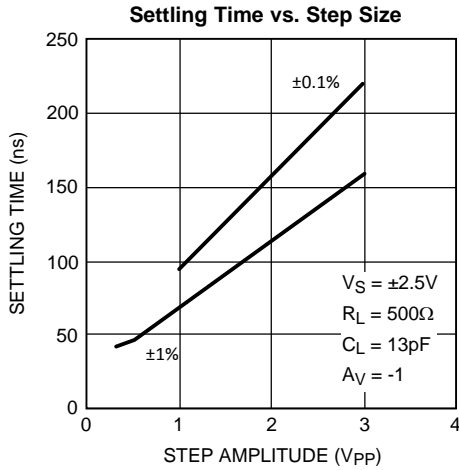


Figure 12.

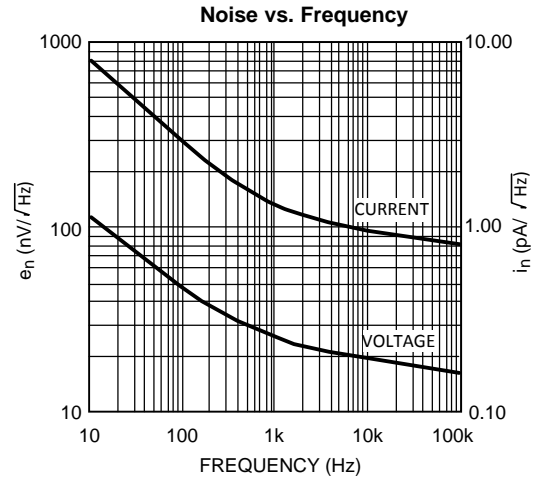


Figure 13.

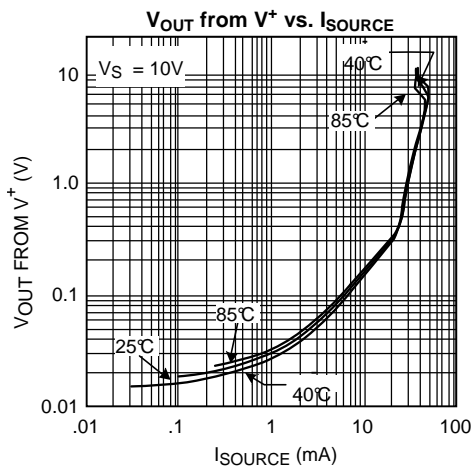


Figure 14.

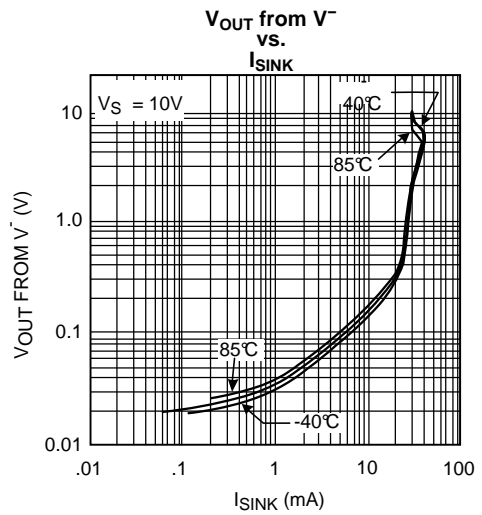


Figure 15.

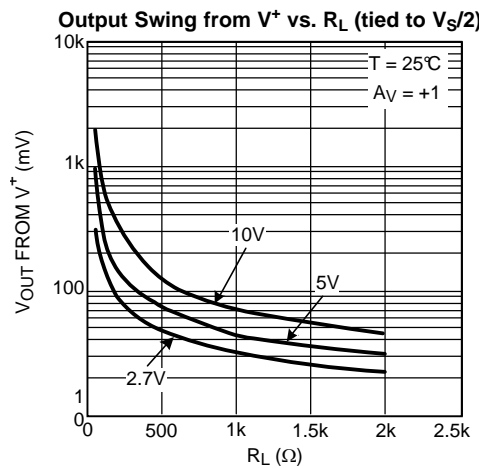


Figure 16.

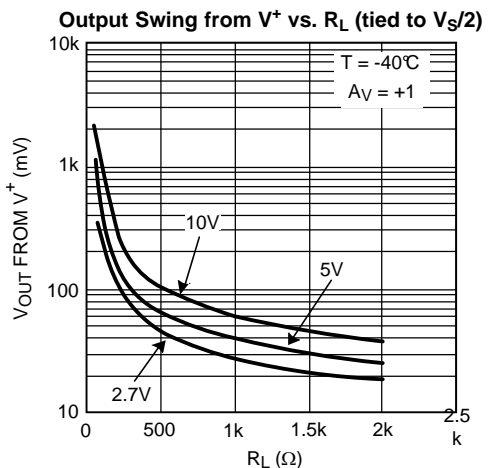


Figure 17.

Typical Performance Characteristics (continued)

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

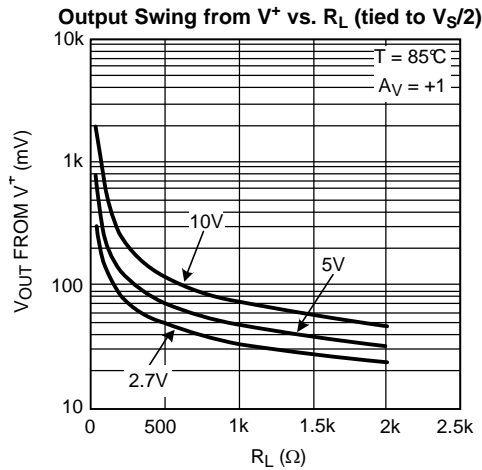


Figure 18.

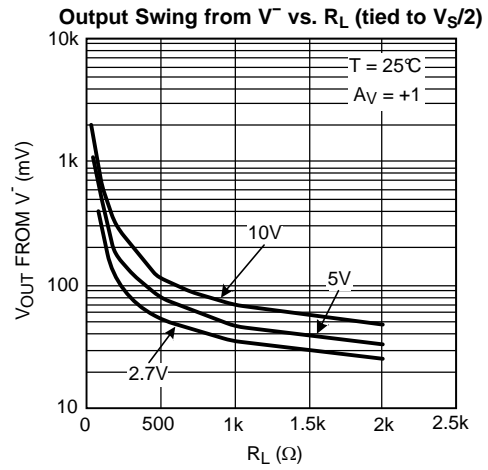


Figure 19.

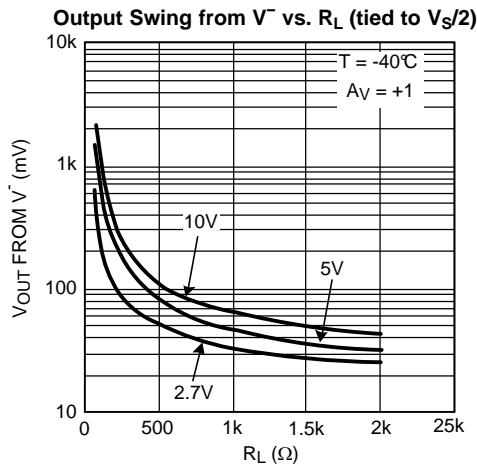


Figure 20.

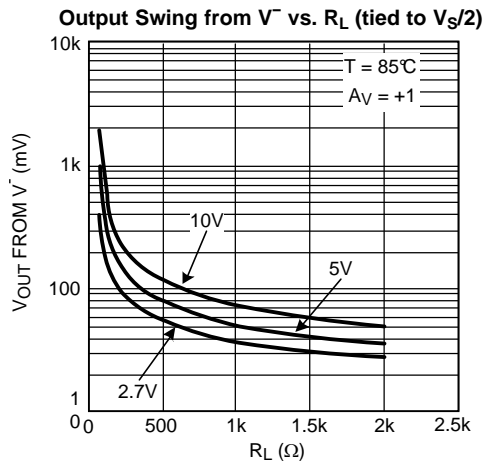


Figure 21.

Cap Load Tolerance and Settling Time vs. Closed Loop Gain

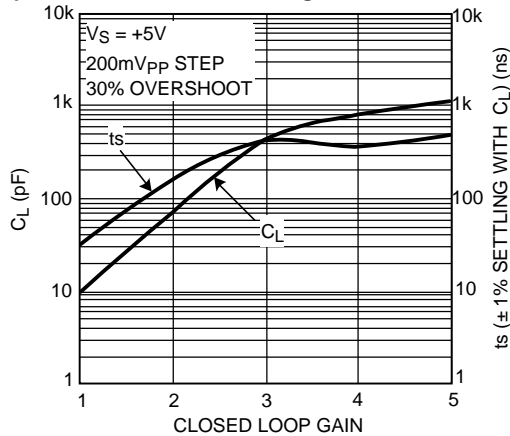


Figure 22.

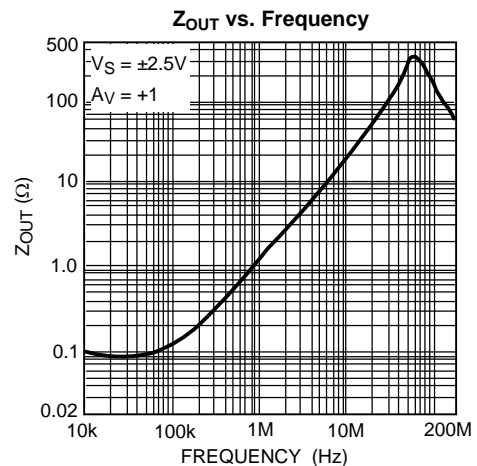


Figure 23.

Typical Performance Characteristics (continued)

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

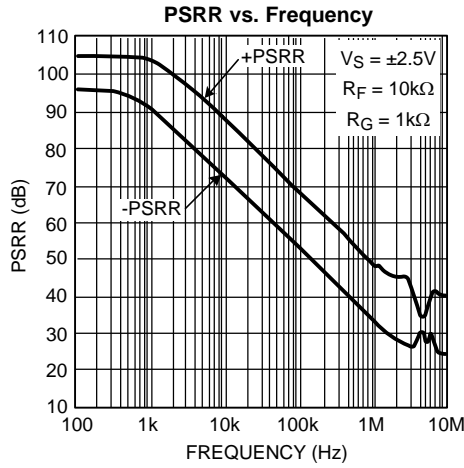


Figure 24.

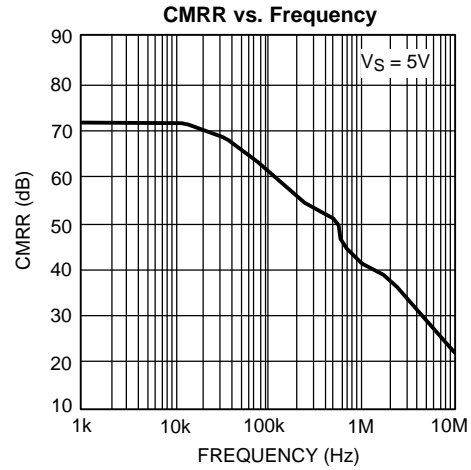


Figure 25.

Crosstalk Rejection vs. Frequency (Output to Output) (LMH6646)

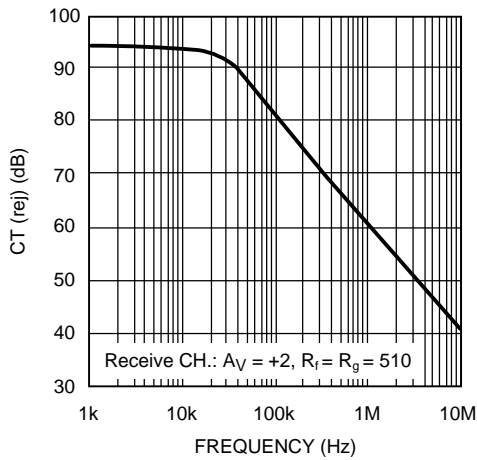


Figure 26.

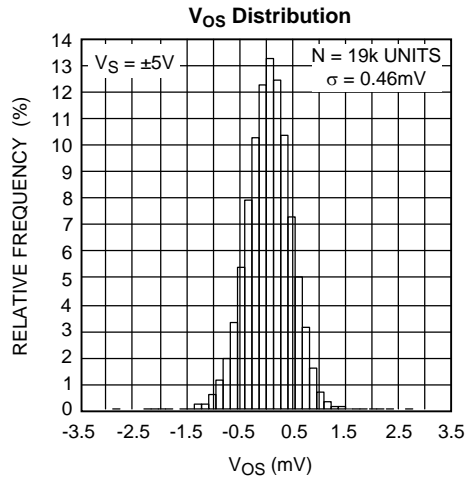


Figure 27.

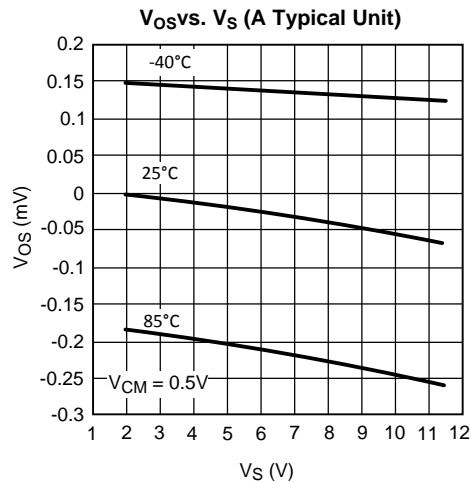


Figure 28.

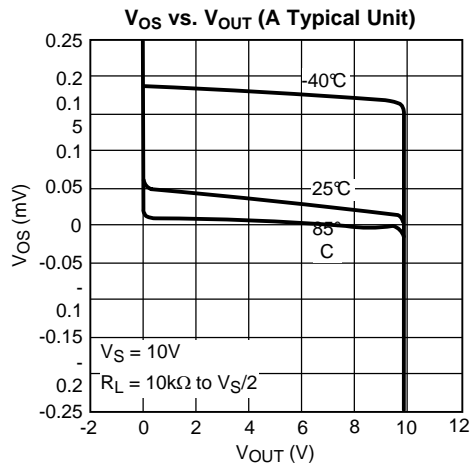


Figure 29.

Typical Performance Characteristics (continued)

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

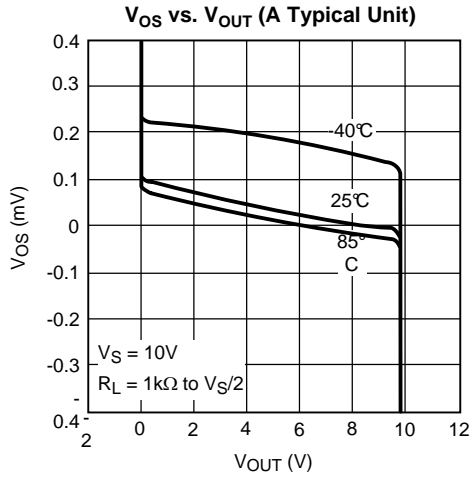


Figure 30.

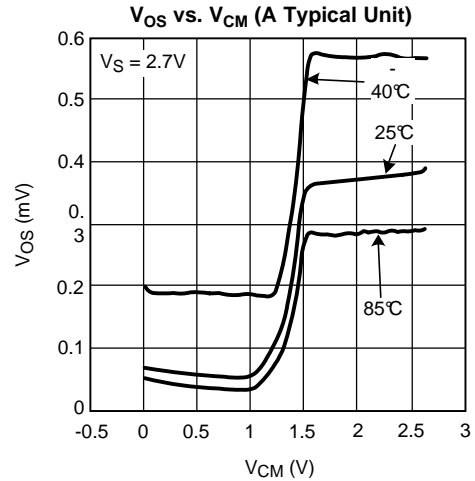


Figure 31.

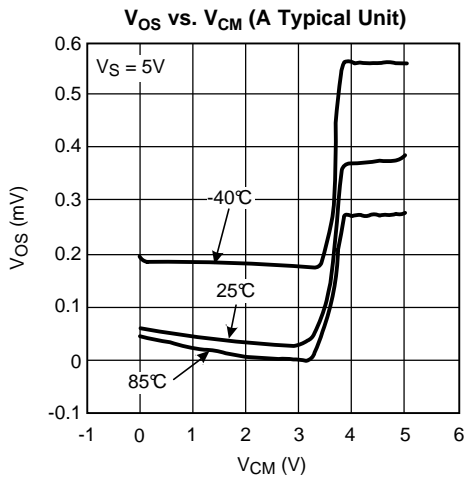


Figure 32.

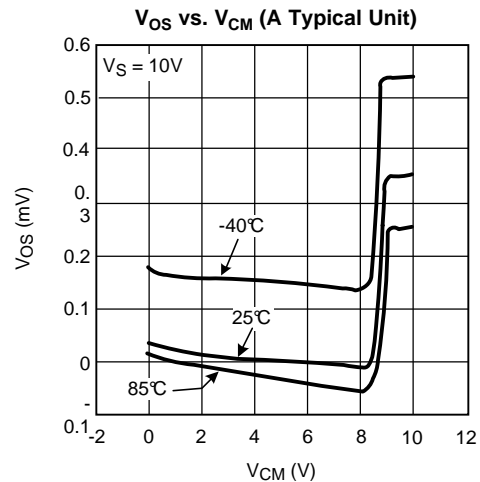


Figure 33.

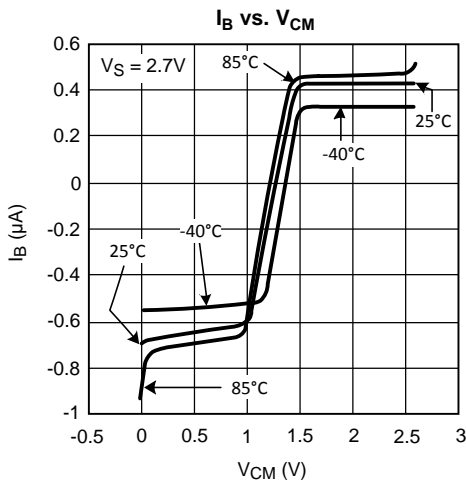


Figure 34.

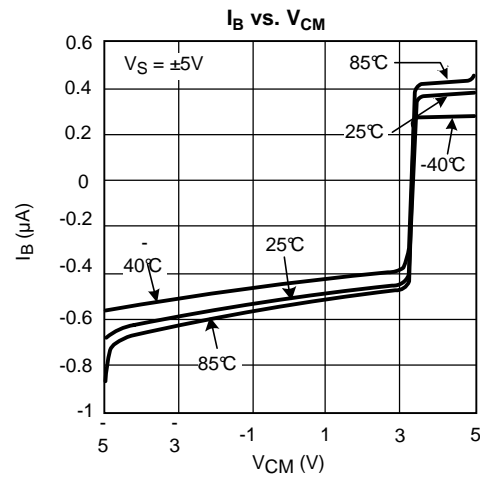


Figure 35.

Typical Performance Characteristics (continued)

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

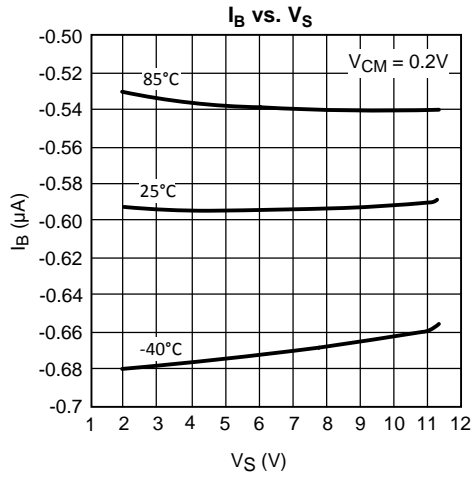


Figure 36.

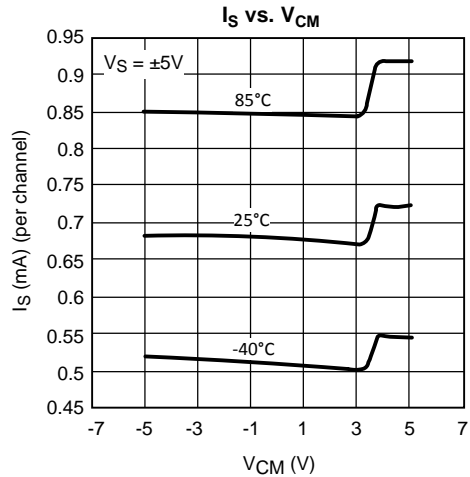


Figure 37.

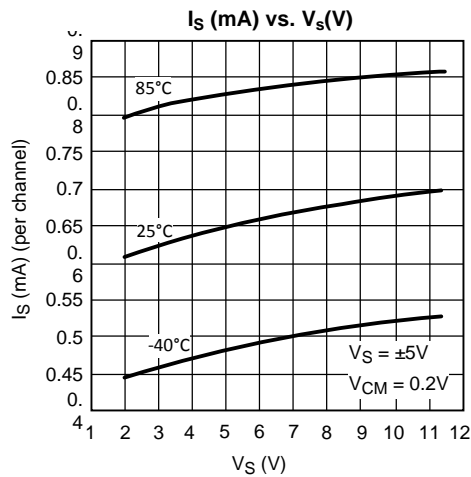


Figure 38.

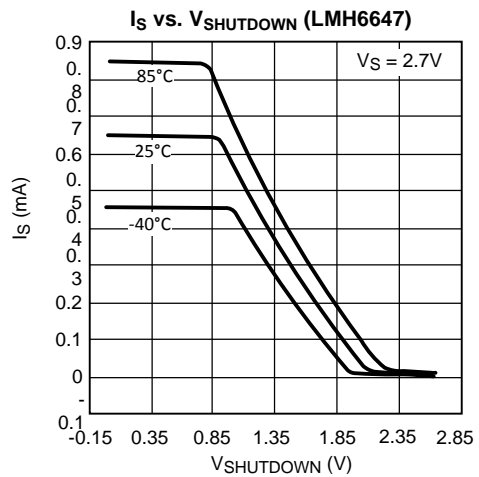


Figure 39.

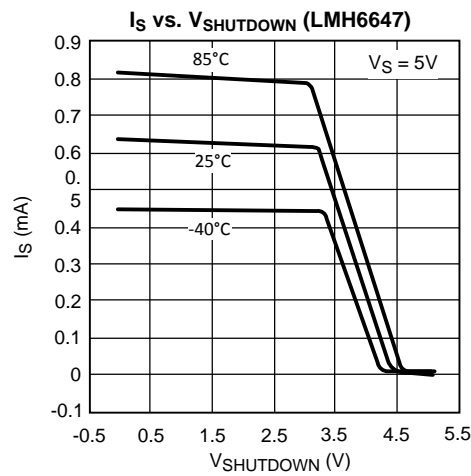


Figure 40.

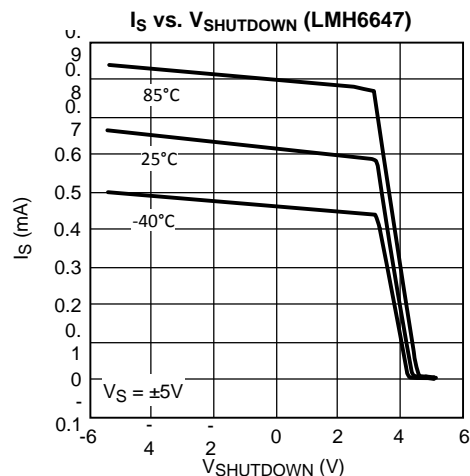


Figure 41.

Typical Performance Characteristics (continued)

At $T_J = 25^\circ\text{C}$. Unless otherwise specified.

Shutdown Pin and Supply Current vs. Shutdown Voltage

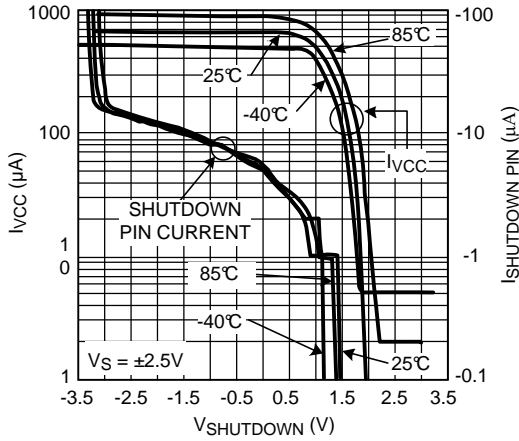


Figure 42.

Small Signal Step Response

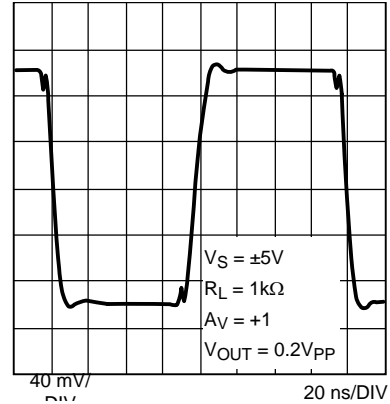


Figure 43.

Large Signal Step Response

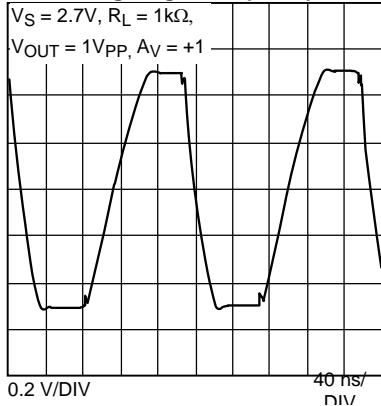


Figure 44.

Large Signal Step Response

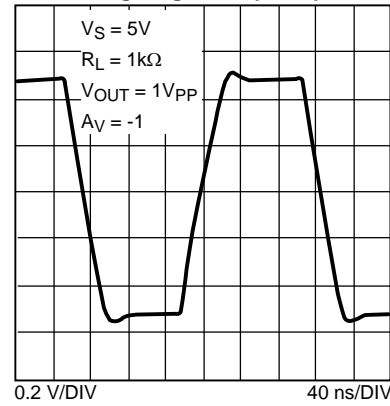


Figure 45.

Output Overload Recovery

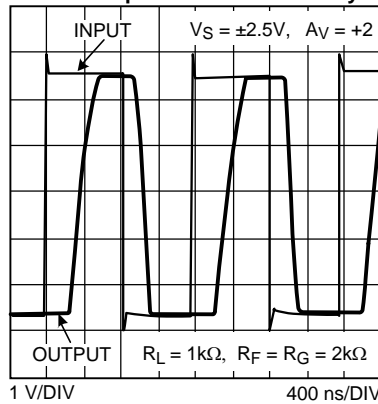


Figure 46.

APPLICATION NOTES

CIRCUIT DESCRIPTION

The LMH6645/6646/6647 family is based on proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8GHz) even under low supply voltage (2.7V) and low Collector bias current.
- Rail-to-Rail input which allows the input common mode voltage to go beyond either rail by about 0.5V typically.
- A class A-B “turn-around” stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-pull output stage capable of 20mA output current (at 0.5V from the supply rails) while consuming only ~700 μ A of total supply current per channel. This architecture allows output to reach within milli-volts of either supply rail at light loads.
- Consistent performance from any supply voltage (2.7V-10V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT} , etc.)

APPLICATION HINTS

The total input common mode voltage range, which extends from below V^- to beyond V^+ , is covered by both a PNP and a NPN stage. The NPN stage is switched on whenever the input is less than 1.2V from V^+ and the PNP stage covers the rest of the range. In terms of the input voltage, there is an overlapping region where both stages are processing the input signal. This region is about 0.5V from beginning to the end. As far as the device application is concerned, this transition is a transparent operation. However, keep in mind that the input bias current value and direction will depend on which input stage is operating (see [Figure 34](#), [35](#), and [36](#) for plots). For low distortion applications, it is best to keep the input common mode voltage from transversing this transition point. Low gain settling applications, which generally encounter larger peak-to-peak input voltages, could be configured as inverting stages to eliminate common mode voltage fluctuations.

In terms of the output, when the output swing approaches either supply rail, the output transistor will enter a Quasi-saturated state. A subtle effect of this operational region is that there is an increase in supply current in this state (up to 1mA). The onset of Quasi-saturation region is a function of output loading (current) and varies from 100mV at no load to about 1V when output is delivering 20mA, as measured from supplies. Both input common mode voltage and output voltage level effect the supply current (see [Figure 37](#) and [38](#). for plot).

With 2.7V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH6645/6646/6647 family is well suited to many low voltage/low power applications. Even with 2.7V supplies, the -3dB BW (@ $A_V = +1$) is typically 55MHz with a tested limit of 45MHz. Production testing guarantees that process variations will not compromise speed.

This device family is designed to avoid output phase reversal. With input over-drive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). [Figure 47](#), below, shows the input and output voltage when the input voltage significantly exceeds the supply voltages:

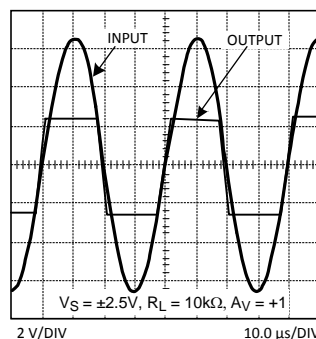


Figure 47. Input/Output Shown with Exceeded Input CMVR

As can be seen, the output does not exhibit any phase reversal as some op amps do. However, if the input voltage range is exceeded by more than a diode drop beyond either rail, the internal ESD protection diodes will start to conduct. The current flow in these ESD diodes should be externally limited.

LMH6647 MICRO-POWER SHUTDOWN

The LMH6647 can be shutdown to save power and reduce its supply current to less than 50µA guaranteed, by applying a voltage to the SD pin. The SD pin is “active high” and needs to be tied to V⁻ for normal operation. This input is low current (<20µA, 4pF equivalent capacitance) and a resistor to V⁻ (≤20kΩ) will result in normal operation. Shutdown is guaranteed when SD pin is 0.4V or less from V⁺ at any operating supply voltage and temperature.

In the shutdown mode, essentially all internal device biasing is turned off in order to minimize supply current flow and the output goes into Hi-Z (high impedance) mode. Complete device Turn-on and Turn-off times vary considerably relative to the output loading conditions, output voltage, and input impedance, but is generally limited to less than 1µs (see tables for actual data).

During shutdown, the input stage has an equivalent circuit as shown below in [Figure 48](#).

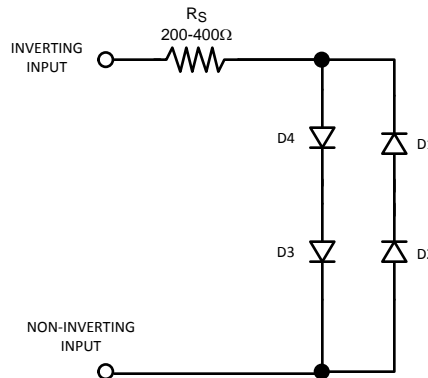


Figure 48. LMH6647 Equivalent Input in Shutdown Mode

As can be seen above, in shutdown, there may be current flow through the internal diodes shown, caused by input potential, if present. This current may flow through the external feedback resistor and result in an apparent output signal. In most shutdown applications the presence of this output is inconsequential. However, if the output is “forced” by another device such as in a multiplexer, the other device will need to conduct the current described in order to maintain the output potential.

To keep the output at or near ground during shutdown when there is no other device to hold the output low, a switch (transistor) could be used to shunt the output to ground. [Figure 49](#) shows a circuit where a NPN bipolar is used to keep the output near ground (~80mV):

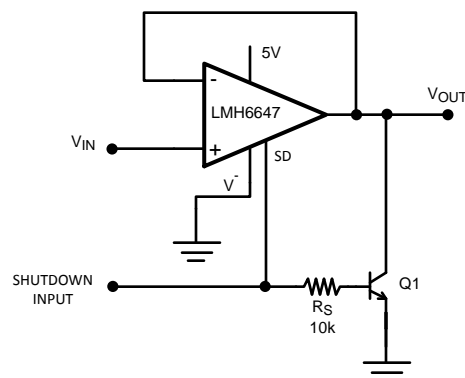


Figure 49. Active Pull-Down Schematic

Figure 50 shows the output waveform.

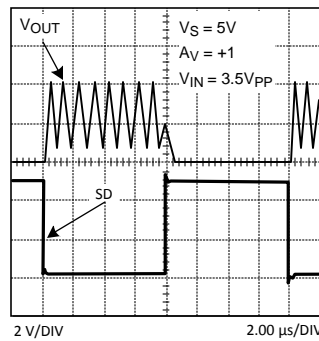


Figure 50. Output Held Low by Active Pull-Down Circuit

If bipolar transistor power dissipation is not tolerable, the switch could be by a N-channel enhancement mode MOSFET.

2.7V SINGLE SUPPLY RRIO 2:1 MUX

The schematic show in Figure 51 will function as a 2:1 MUX operating on a single 2.7V power supply, by utilizing the shutdown feature of the LMH6647:

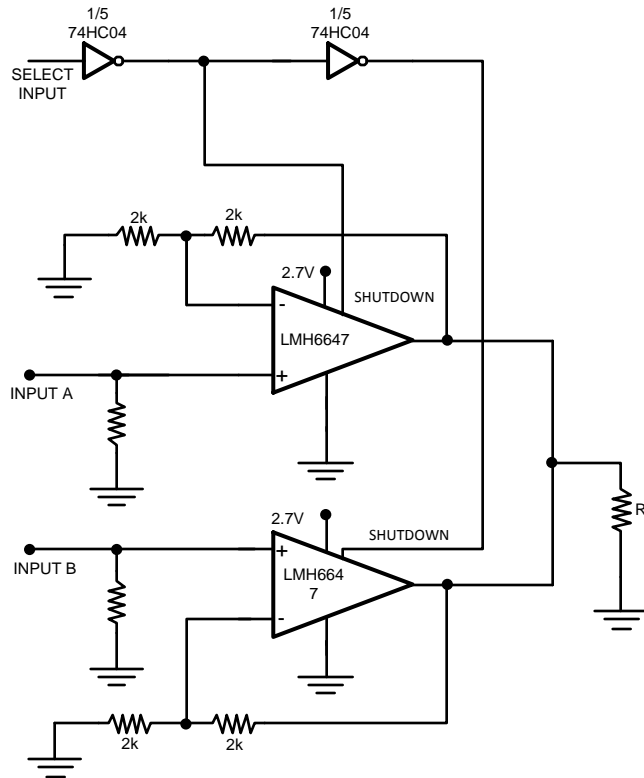


Figure 51. 2:1 MUX Operating off a 2.7V Single Supply

Figure 52 shows the MUX output when selecting between a 1MHz sine and a 250KHz triangular waveform.

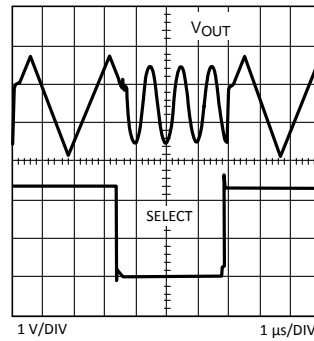


Figure 52. 2:1 MUX Output

As can be seen in Figure 52, the output is well behaved and there are no spikes or glitches due to the switching. Switching times are approximately around 500ns based on the time when the output is considered “valid”.

PRINTED CIRCUIT BOARD LAYOUT, COMPONENT VALUES SELECTION, AND EVALUATION BOARDS

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information).

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing large valued external resistors, will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6645MF	SOT-23-5	CLC730068
LMH6645MA	8-Pin SOIC	CLC730027
LMH6646MA	8-Pin SOIC	CLC730036
LMH6646MM	8-Pin VSSOP	CLC730123
LMH6647MA	8-Pin SOIC	CLC730027
LMH6647MF	SOT-23-6	CLC730116

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor.

LMH6647 Evaluation

For normal operation, tie the SD pin to V^- .

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6645MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 45MA	Samples
LMH6645MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 45MA	Samples
LMH6645MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A68A	
LMH6645MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A68A	Samples
LMH6645MFX	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A68A	
LMH6645MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A68A	Samples
LMH6646MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 46MA	Samples
LMH6646MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 46MA	Samples
LMH6646MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A70A	
LMH6646MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A70A	Samples
LMH6646MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A70A	Samples
LMH6647MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 47MA	Samples
LMH6647MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 47MA	Samples
LMH6647MF	NRND	SOT-23	DBV	6	1000	TBD	Call TI	Call TI	-40 to 85	A69A	
LMH6647MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A69A	Samples
LMH6647MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A69A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

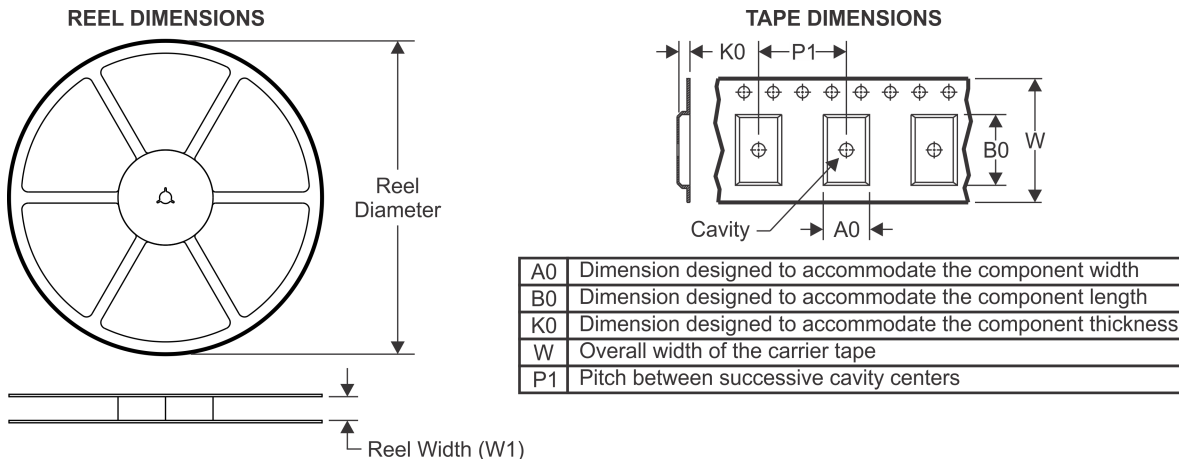
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6645MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6645MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6645MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6646MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6647MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6647MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6647MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6647MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

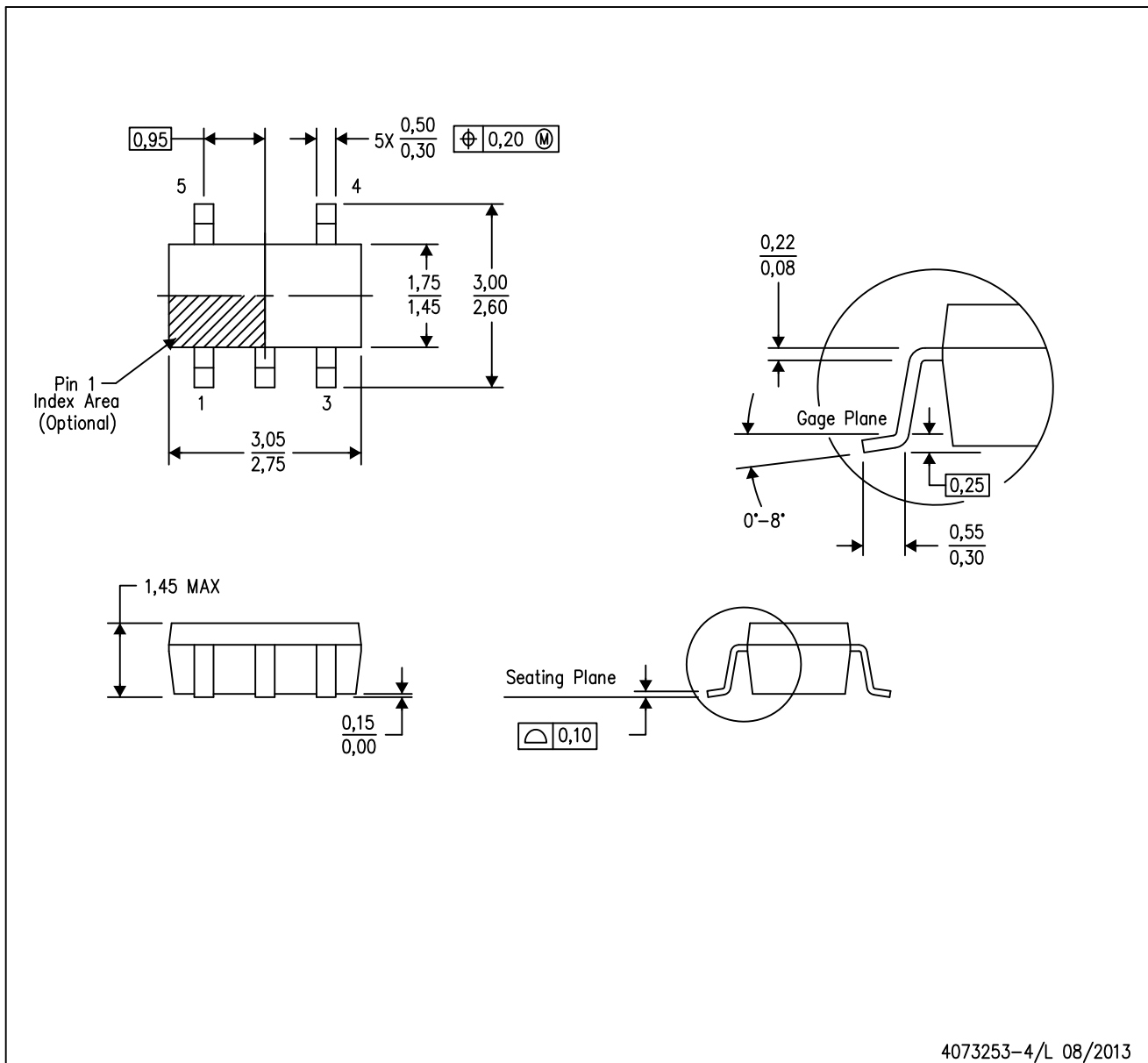

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6645MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6645MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6645MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6646MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6647MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6647MF	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMH6647MF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
LMH6647MFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

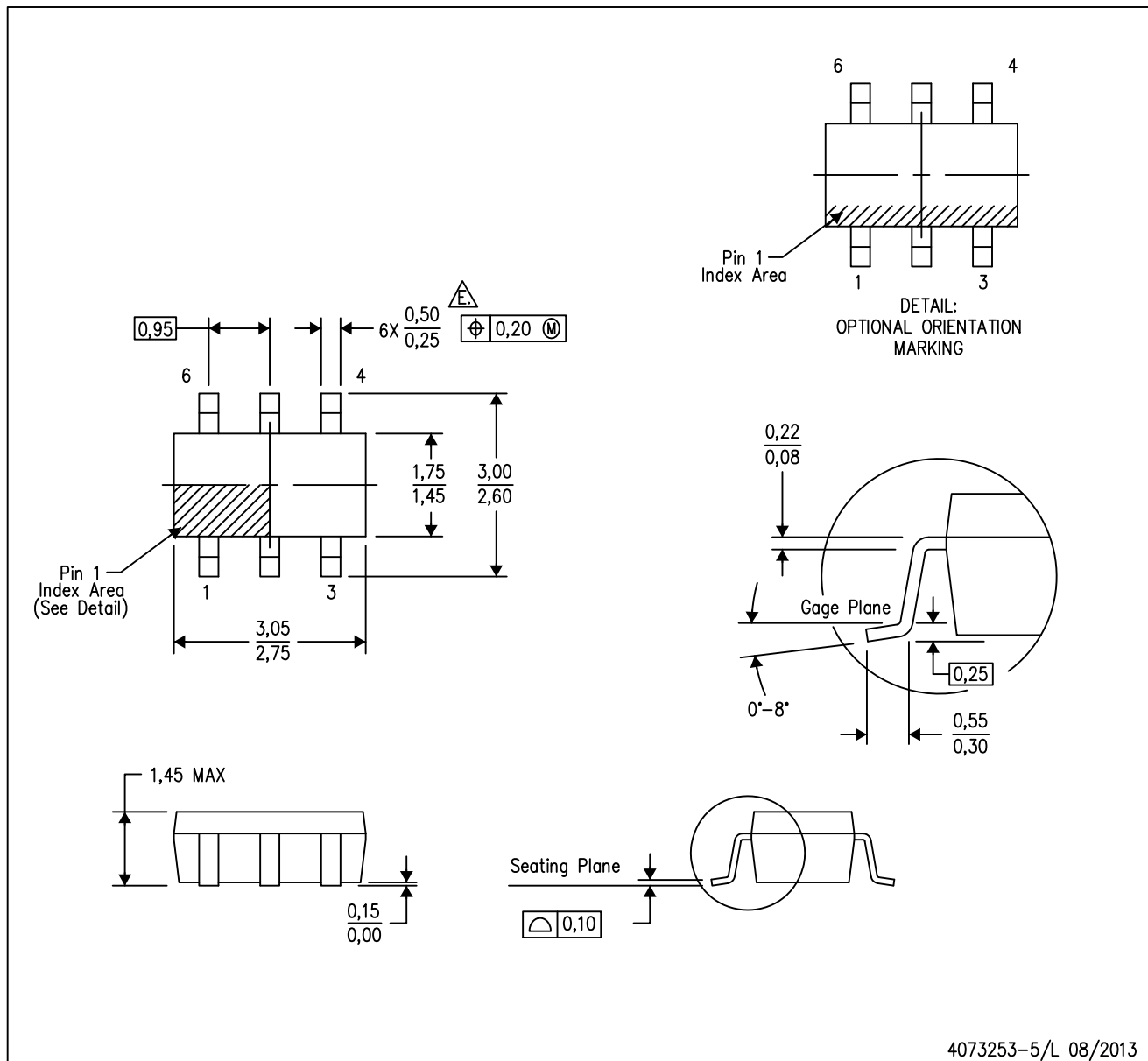


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DBV (R-PDSO-G6)

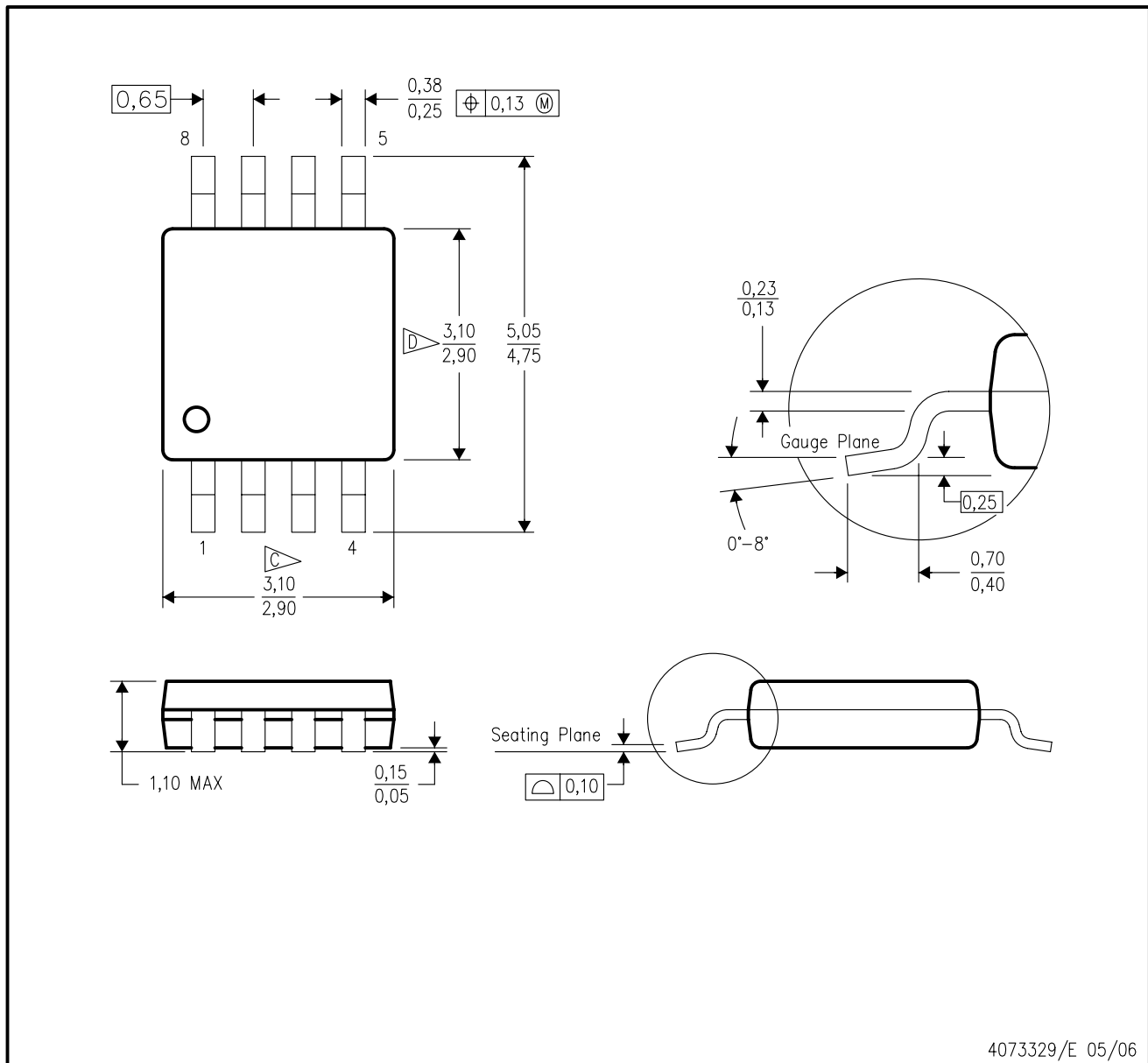
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DGK (S-PDSO-G8)

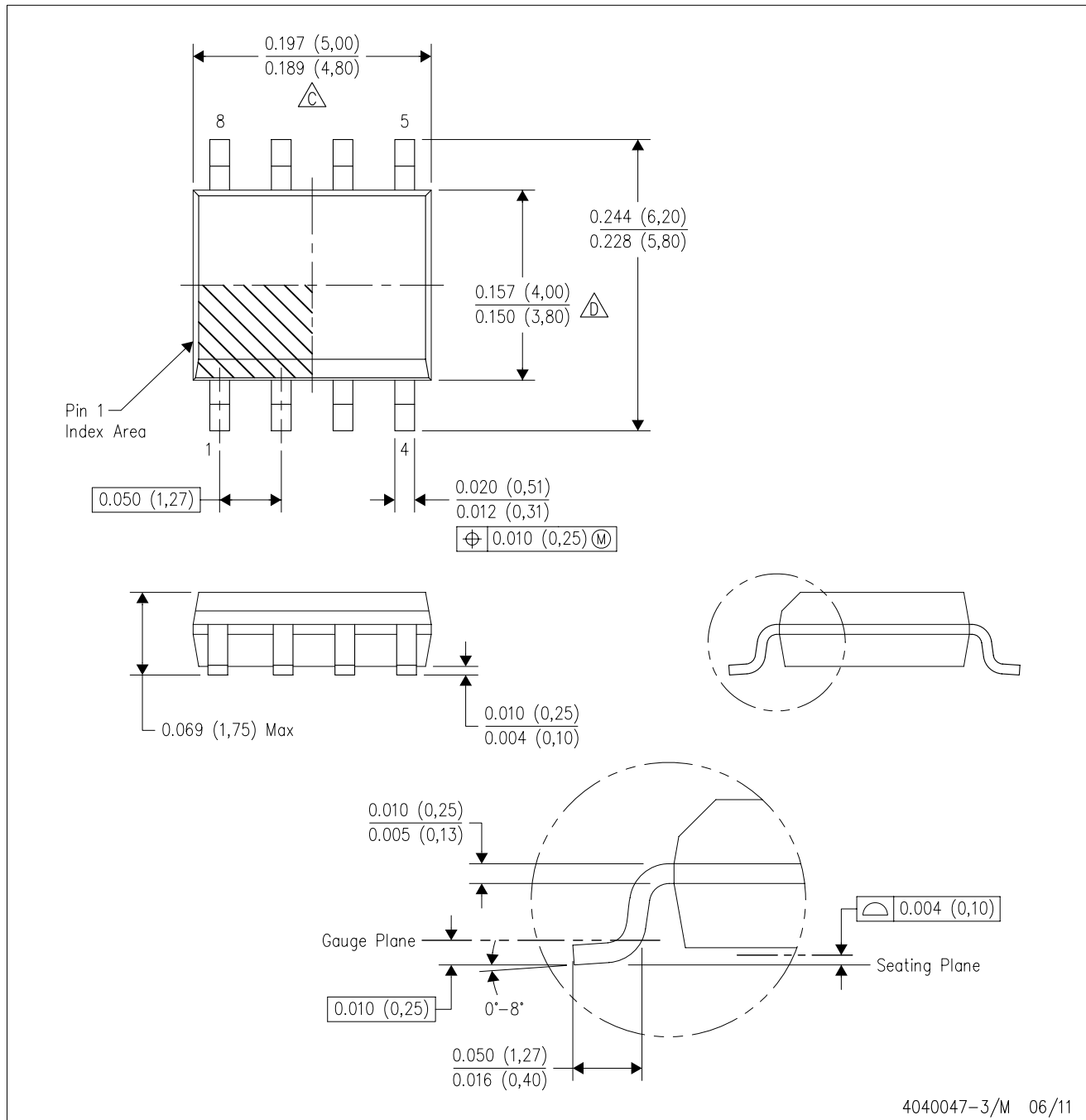
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AA.

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