LMH6609 900MHz Voltage Feedback Op Amp

Check for Samples: LMH6609

FEATURES

- **900MHz −3dB bandwidth ($A_V = 1$)**
- **Large signal bandwidth and slew rate 100% tested**
- **280MHz −3dB bandwidth ($A_V = +2$, $V_{OUT} = 2V_{PP}$)**
- **90mA linear output current**
- **1400V/μs slew rate**
- **Unity gain stable**
- **<1mV input Offset voltage**
- **7mA Supply current (no load)**
- **6.6V to 12V supply voltage range**
- **0.01%/0.026° differential gain/phase PAL**
- **3.1nV$\sqrt{Hz}$ voltage noise**
- **Improved replacement for CLC440, CL420, CL426**

APPLICATIONS

- **Test equipment**
- **IF/RF amplifier**
- **A/D Input driver**
- **Active filter**
- **Integrator**
- **DAC output buffer**
- **TI's Transimpedance amplifier**

DESCRIPTION

The LMH6609 is an ultra wideband, unity gain stable, low power, voltage feedback op amp that offers 900MHz bandwidth at a gain of 1, 1400V/μs slew rate and 90mA of linear output current.

The LMH6609 is designed with voltage feedback architecture for maximum flexibility especially for active filters and integrators. The LMH6609 has balanced, symmetrical inputs with well-matched bias currents and minimal offset voltage.

With Differential Gain of 0.01% and Differential Phase of 0.026° the LMH6609 is suited for video applications. The 90mA of linear output current makes the LMH6609 suitable for multiple video loads and cable driving applications as well.

The supply voltage is specified at 6.6V and 10V. A low supply current of 7mA (at 10V supply) makes the LMH6609 useful in a wide variety of platforms, including portable or remote equipment that must run from battery power.

The LMH6609 is available in the industry standard 8-pin SOIC package and in the space-saving 5-pin SOT-23 package. The LMH6609 is specified for operation over the -40°C to +85°C temperature range. The LMH6609 is manufactured in state-of-the-art VIP10™ technology for high performance.

Typical Application

$$K = 1 + \frac{R_F}{R_G} \qquad Q = \frac{m}{1 + m^2(2 - K)} \qquad \omega_o = \frac{1}{mRC}$$

Q, K ARE UNITLESS.
ω_O IS RELATED TO BANDWIDTH AND IS IN UNITS OF RADIANS/SEC. DIVIDE ω_O BY 2π TO GET IT IN Hz.
REFER TO OA-26 FOR MORE INFORMATION.

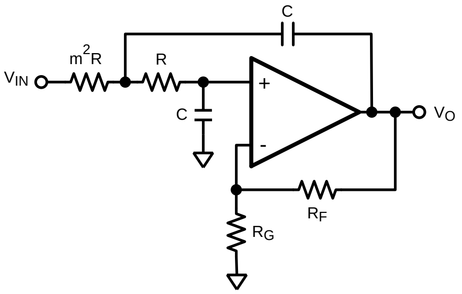

Figure 1. Sallen Key Low Pass Filter with Equal C Value

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

V_S (V^+ - V^-)	±6.6V
I_{OUT}	(2)
Common Mode Input Voltage	V+ to V−
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	+300°C
ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. For specifications, see the Electrical Characteristics tables.
(2) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details.
(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω In series with 200pF.

Operating Ratings (1)

Thermal Resistance	Package	(θ_{JC})	(θ_{JA})
	8-Pin SOIC	65°C/W	145°C/W
	5-Pin SOT23	120°C/W	187°C/W
Operating Temperature		−40°C	+85°C
Nominal Supply Voltage (2)		±3.3V	±6V

(1) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Section for more details.
(2) Nominal Supply voltage range is for supplies with regulation of 10% or better.

±5V Electrical Characteristics

Unless specified, $A_V = +2$, $R_F = 250\Omega$: $V_S = \pm5V$, $R_L = 100\Omega$; unless otherwise specified. **Boldface** limits apply over temperature Range. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
SSBW	−3dB Bandwidth	$V_{OUT} = 0.5V_{PP}$		260		MHz
LSBW	−3dB Bandwidth	$V_{OUT} = 4.0V_{PP}$	150	170		MHz
SSBWG1	−3dB Bandwidth $A_V = 1$	$V_{OUT} = 0.25V_{PP}$		900		MHz
GFP	.1dB Bandwidth	Gain is Flat to .1dB		130		MHz
DG	Differential Gain	$R_L = 150\Omega$, 4.43MHz		0.01		%
DP	Differential Phase	$R_L = 150\Omega$, 4.43MHz		0.026		deg
Time Domain Response						
TRS	Rise and Fall Time	1V Step		1.6		ns
TRL		4V Step		2.6		ns
t_s	Settling Time to 0.05%	2V Step		15		ns
SR	Slew Rate	4V Step (2)	1200	1400		V/µs

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature derating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Slew rate is Average of Rising and Falling 40-60% slew rates.

±5V Electrical Characteristics (continued)

Unless specified, $A_V = +2$, $R_F = 250\Omega$: $V_S = \pm5V$, $R_L = 100\Omega$; unless otherwise specified. **Boldface** limits apply over temperature Range. (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz		−63		dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 20MHz		−57		dBc
	Equivalent Input Noise					
VN	Voltage Noise	>1MHz		3.1		$nV/\sqrt{Hz}$
CN	Current Noise	>1MHz		1.6		$pA/\sqrt{Hz}$
Static, DC Performance						
V_{IO}	Input Offset Voltage			±0.8	±2.5 **±3.5**	mV
	Input Voltage Temperature Drift			4		μV/°C
I_{BN}	Input Bias Current			−2	±5 **±8**	μA
	Bias Current Temperature Drift			11		nA/°C
I_{BI}	Input Offset Current			0.1	±1.5 **±3**	μA
PSRR	Power Supply Rejection Ratio	DC, 1V Step	67 **65**	73		dB
CMRR	Common Mode Rejection Ratio	DC, 2V Step	67 **65**	73		dB
I_{CC}	Supply Current	$R_L = \infty$		7.0	7.8 **8.5**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance			1		MΩ
C_{IN}	Input Capacitance			1.2		pF
R_{OUT}	Output Resistance	Closed Loop		0.3		Ω
V_O	Output Voltage Range	$R_L = \infty$	±3.6 **±3.3**	±3.9		V
V_{OL}		$R_L = 100\Omega$	±3.2 **±3.0**	±3.5		V
CMIR	Input Voltage Range	Common Mode, CMRR > 60dB	±2.8 **±2.5**	±3.0		V
I_O	Linear Output Current	V_{OUT}	±60 **±50**	±90		mA

±3.3V Electrical Characteristics

Unless specified, A_V = +2, R_F = 250Ω: V_S = ±3.3V, R_L = 100Ω; unless otherwise specified. **Boldface** limits apply over temperature Range. (1)

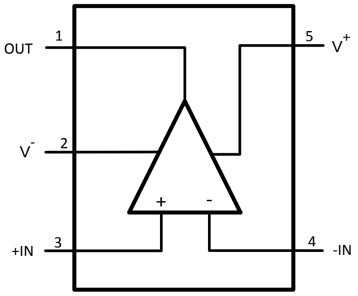
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
SSBW	−3dB Bandwidth	V_{OUT} = 0.5V_{PP}		180		MHz
LSBW	−3dB Bandwidth	V_{OUT} = 3.0V_{PP}		110		MHz
SSBWG1	−3dB Bandwidth A_V = 1	V_{OUT} = 0.25V_{PP}		450		MHz
GFP	.1dB Bandwidth	V_{OUT} = 1V_{PP}		40		MHz
DG	Differential Gain	R_L = 150Ω, 4.43MHz		.01		%
DP	Differential Phase	R_L = 150Ω, 4.43MHz		.06		deg
Time Domain Response						
TRL		1V Step		2.2		ns
SR	Slew Rate	2V Step (2)		800		V/µs
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz		−63		dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz		−43		dBc
	Equivalent Input Noise					
VN	Voltage Noise	>1MHz		3.7		nV/ pA/√Hz
CN	Current Noise	>1MHz		1.1		pA/√Hz
Static, DC Performance						
V_{IO}	Input Offset Voltage			0.8	±2.5 **±3.5**	mV
I_{BN}	Input Bias Current			−1	±3 **±6**	µA
I_{BI}	Input Offset Current			0	±1.5 **±3**	µA
PSRR	Power Supply Rejection Ratio	DC, .5V Step	67	73		dB
CMRR	Common Mode Rejection Ratio	DC, 1V Step	67	75		dB
I_{CC}	Supply Current	R_L = ∞		3.6	5 **6**	mA
Miscellaneous Performance						
R_{OUT}	Input Resistance	Close Loop		.05		Ω
V_O	Output Voltage Range	R_L = ∞	±2.1	±2.3		V
V_{OL}		R_L = 100Ω	±1.9	±2.0		V
CMIR	Input Voltage Range	Common Mode		±1.3		V
I_O	Linear Output Current	V_{OUT}	±30	±45		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature derating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

(2) Slew rate is Average of Rising and Falling 40-60% slew rates.

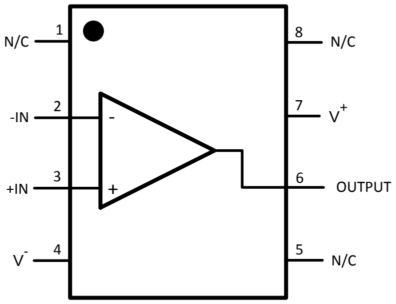
CONNECTION DIAGRAM

5-Pin SOT-23
(Top View)



See Package Number D0008A

8-Pin SOIC
(Top View)



See Package Number DBV0005A

Typical Performance Characteristics

Small Signal Non-Inverting Frequency Response

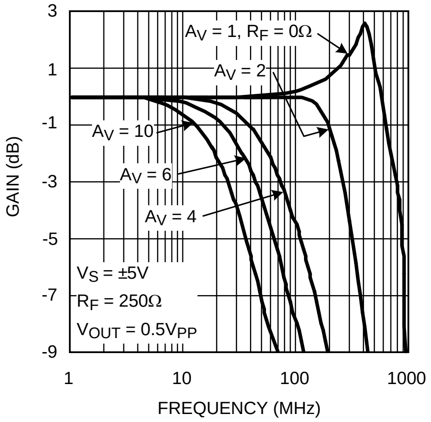


Figure 2.

Large Signal Non-Inverting Frequency Response

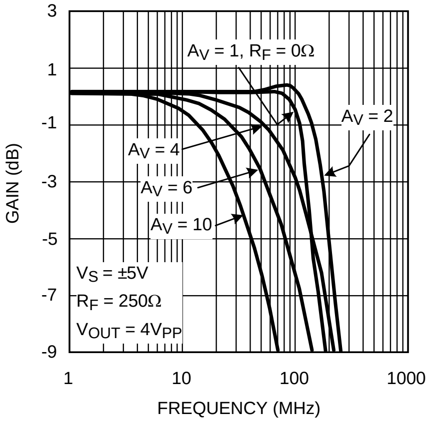


Figure 3.

Small Signal Inverting Frequency Response

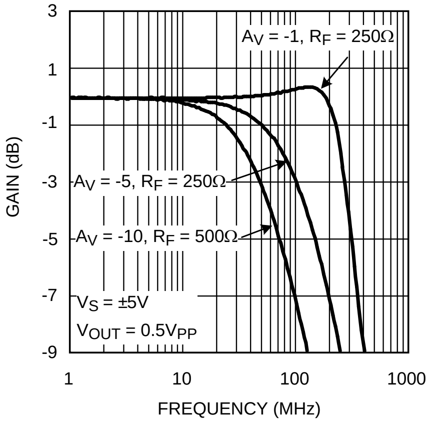


Figure 4.

Large Signal Inverting Frequency Response

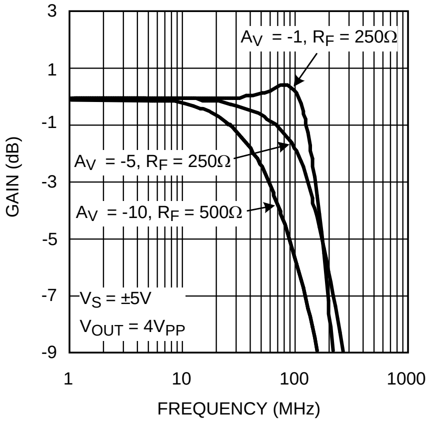


Figure 5.

Frequency Response vs. V_{OUT} $A_V = 2$

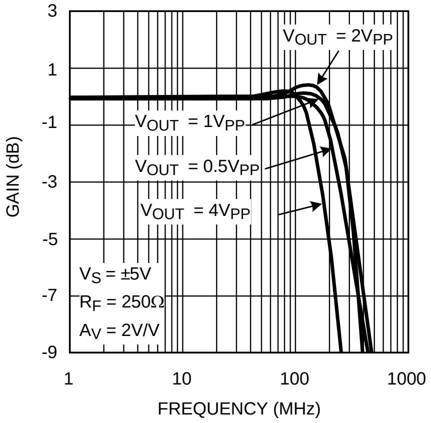


Figure 6.

Frequency Response vs. V_{OUT} $A_V = 2$

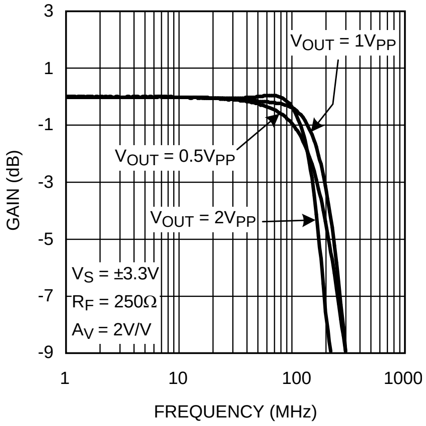


Figure 7.

Typical Performance Characteristics (continued)

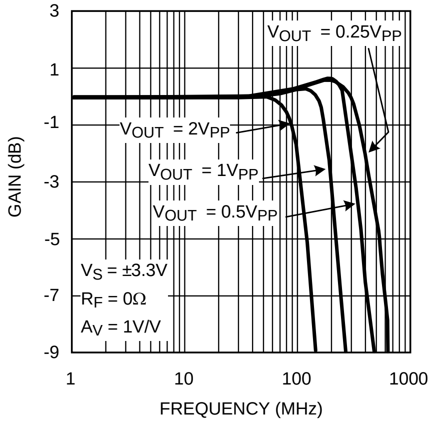

Frequency Response vs. V_{OUT} $A_V = 1$

Figure 8.

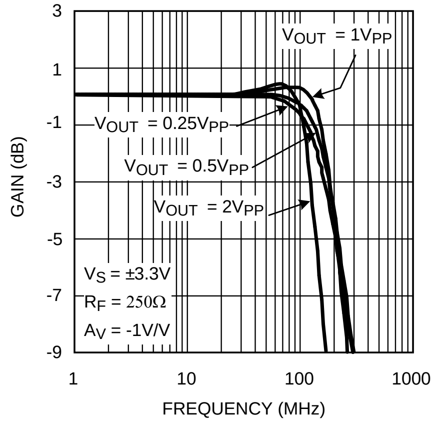

Frequency Response vs. V_{OUT} $A_V = -1$

Figure 9.

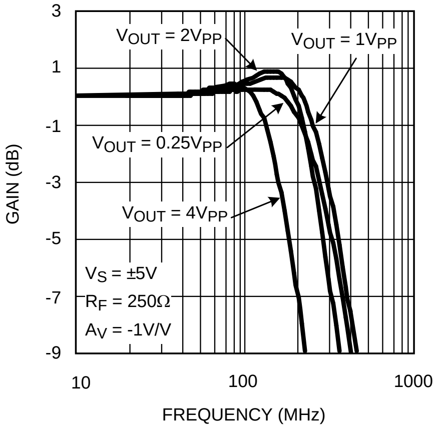

Frequency Response vs. V_{OUT} $A_V = -1$

Figure 10.

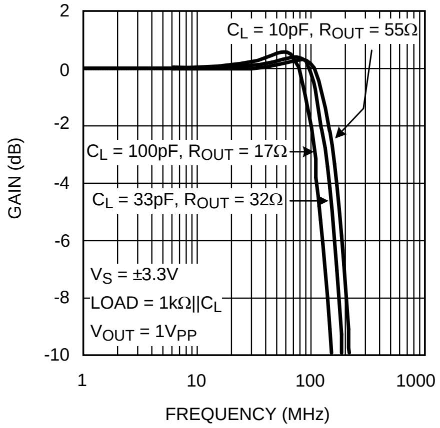

Frequency Response vs. Cap Load

Figure 11.

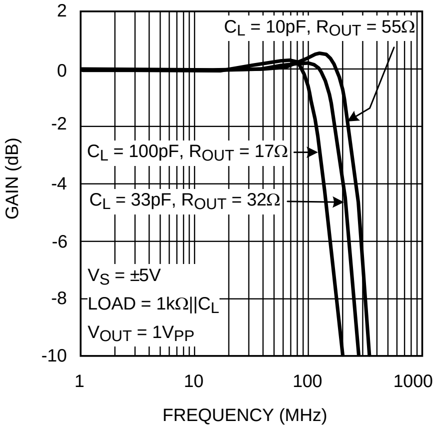

Frequency Response vs. Cap Load

Figure 12.

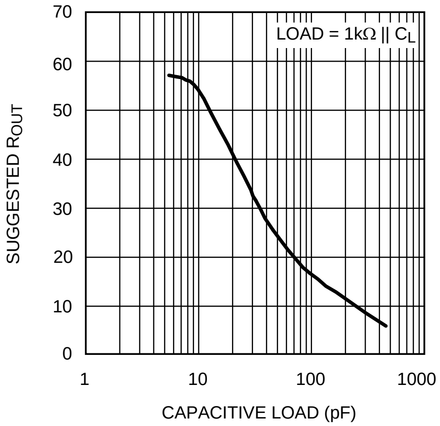

Suggested R_{OUT} vs. Cap Load

Figure 13.

Typical Performance Characteristics (continued)

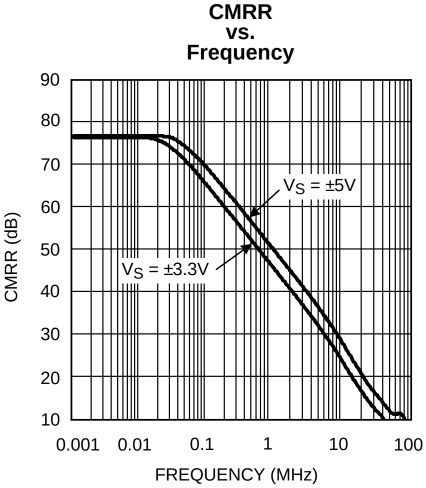


Figure 14.

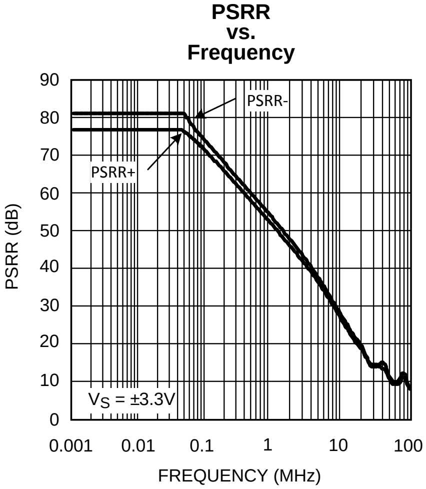


Figure 15.

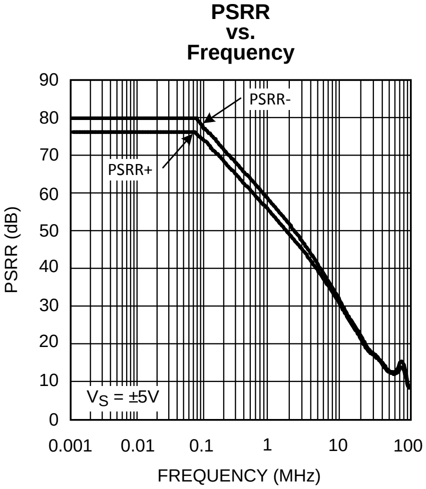


Figure 16.

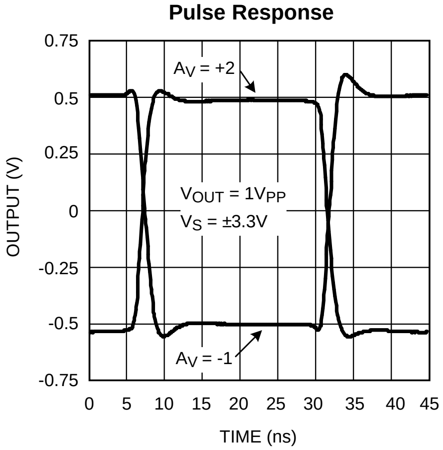


Figure 17.

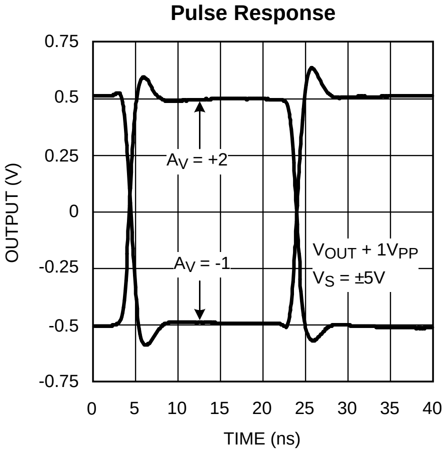


Figure 18.

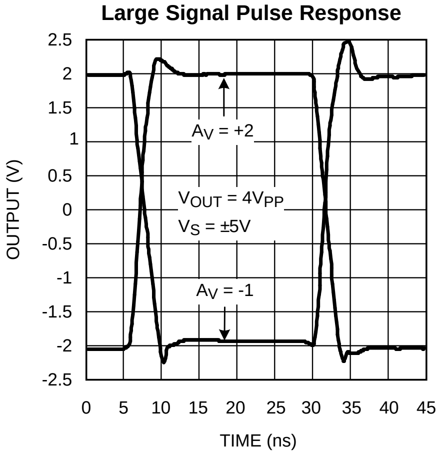


Figure 19.

Typical Performance Characteristics (continued)

Noise vs. Frequency

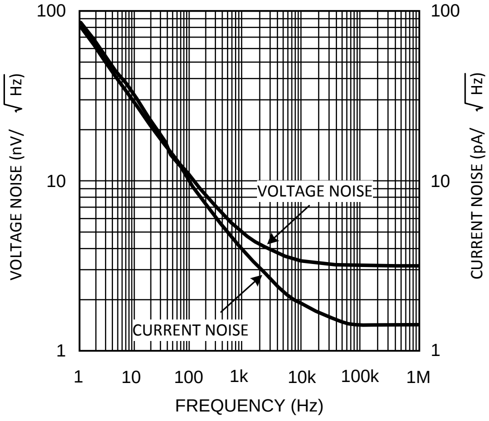


Figure 20.

HD2 vs. V_{OUT}

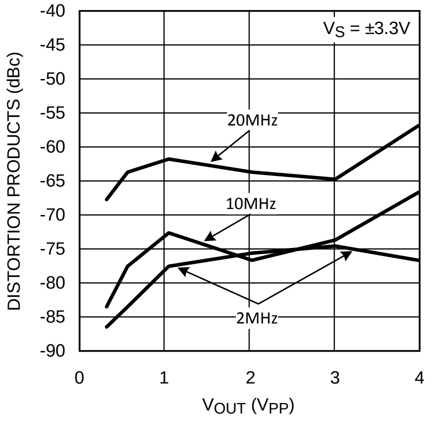


Figure 21.

HD3 vs. V_{OUT}

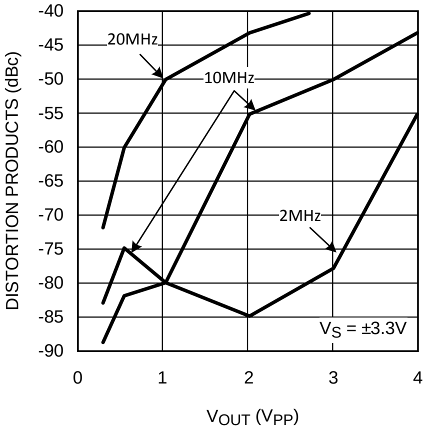


Figure 22.

HD2 vs. V_{OUT}

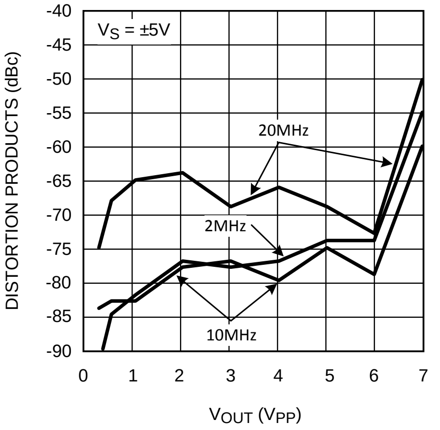


Figure 23.

HD3 vs. V_{OUT}

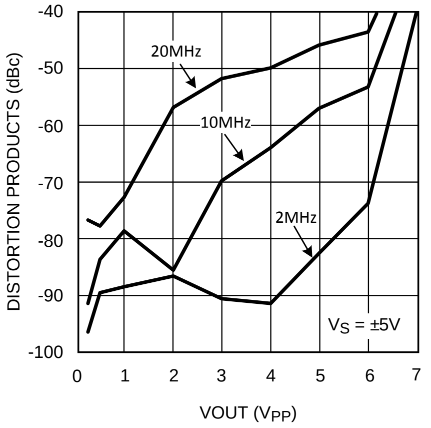


Figure 24.

HD2 & HD3 vs. Frequency

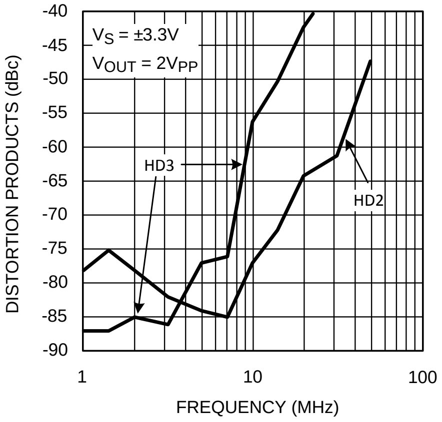


Figure 25.

Typical Performance Characteristics (continued)

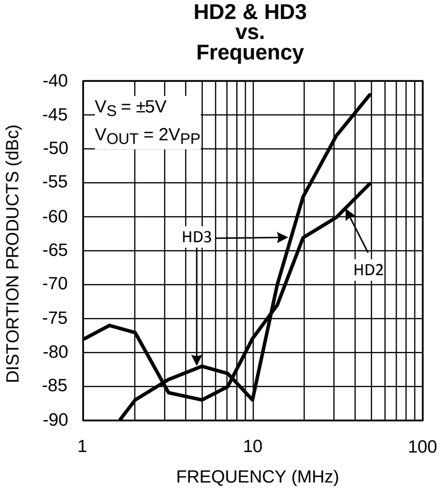


Figure 26.

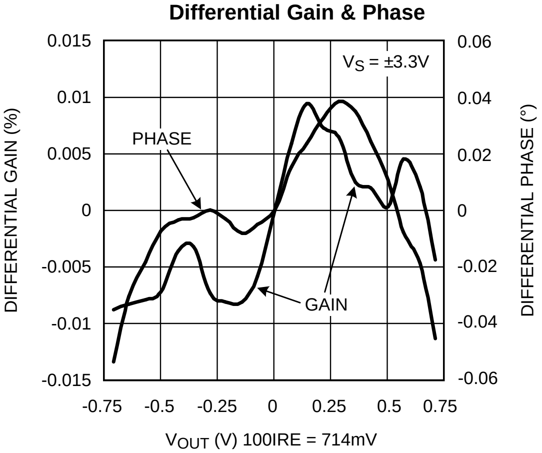


Figure 27.

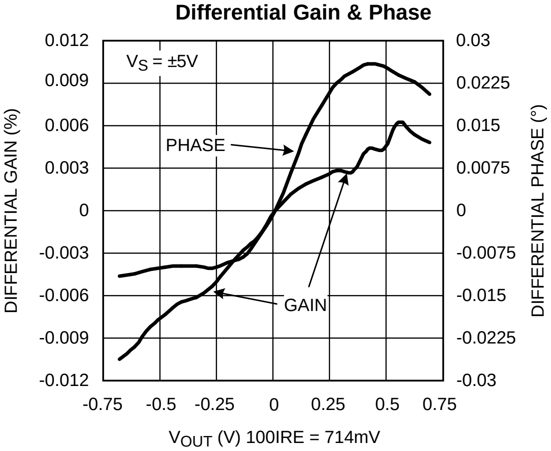


Figure 28.

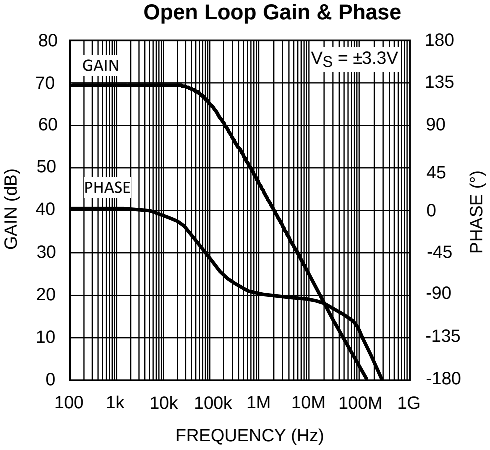


Figure 29.

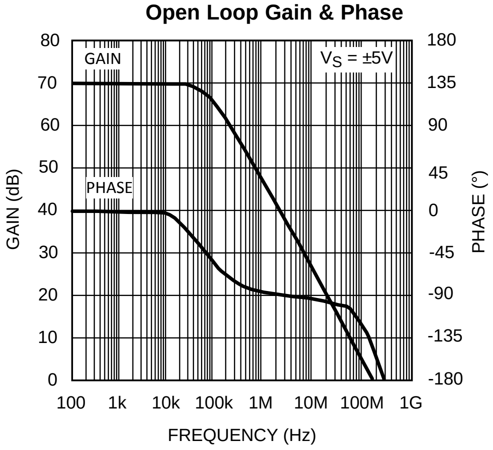


Figure 30.

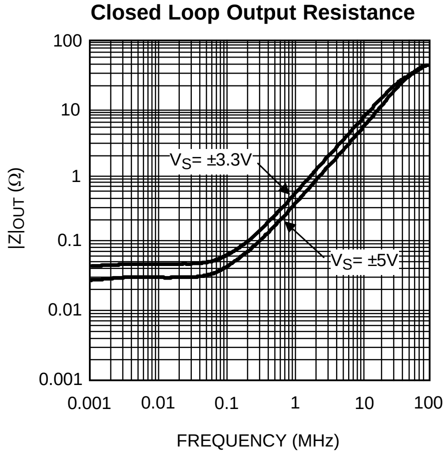


Figure 31.

APPLICATION INFORMATION

GENERAL DESIGN EQUATION

The LMH6609 is a unity gain stable voltage feedback amplifier. The matched input bias currents track well over temperature. This allows the DC offset to be minimized by matching the impedance seen by both inputs.

GAIN

The non-inverting and inverting gain equations for the LMH6609 are as follows:

$$\text{NON-INVERTING GAIN : } 1+\frac{R_F}{R_G}$$

$$\text{INVERTING GAIN : } -\frac{R_F}{R_G} \qquad (1)$$

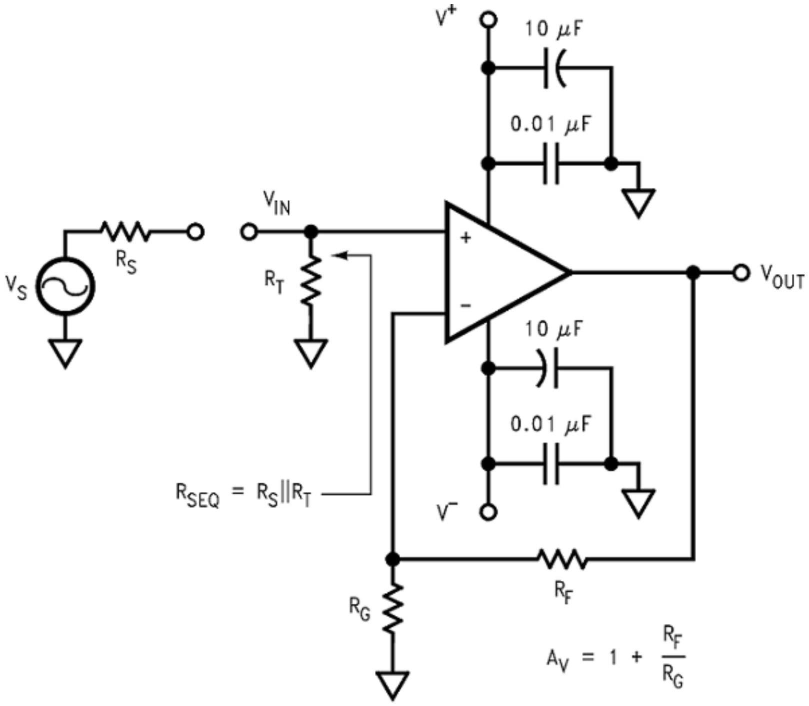


Figure 32. Typical Non-Inverting Application

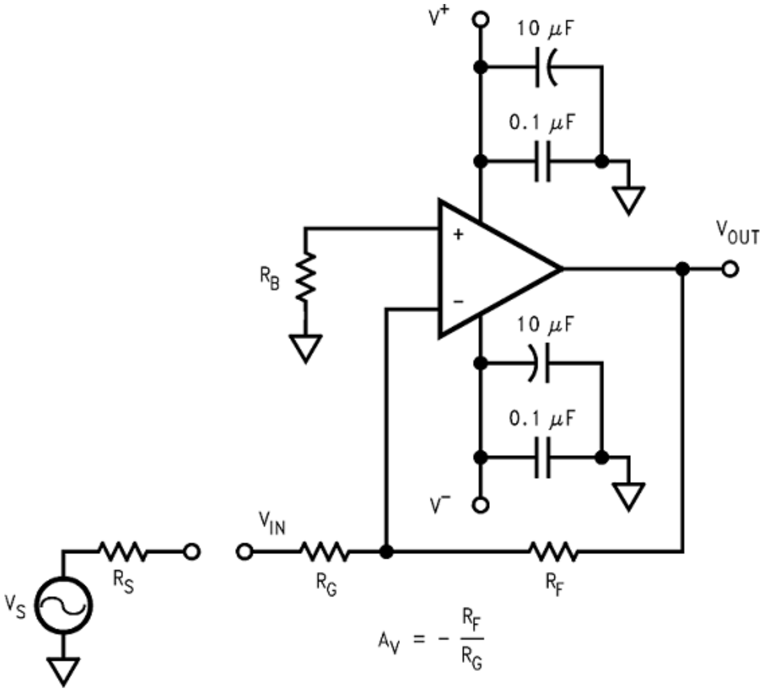


Figure 33. Typical Inverting Application

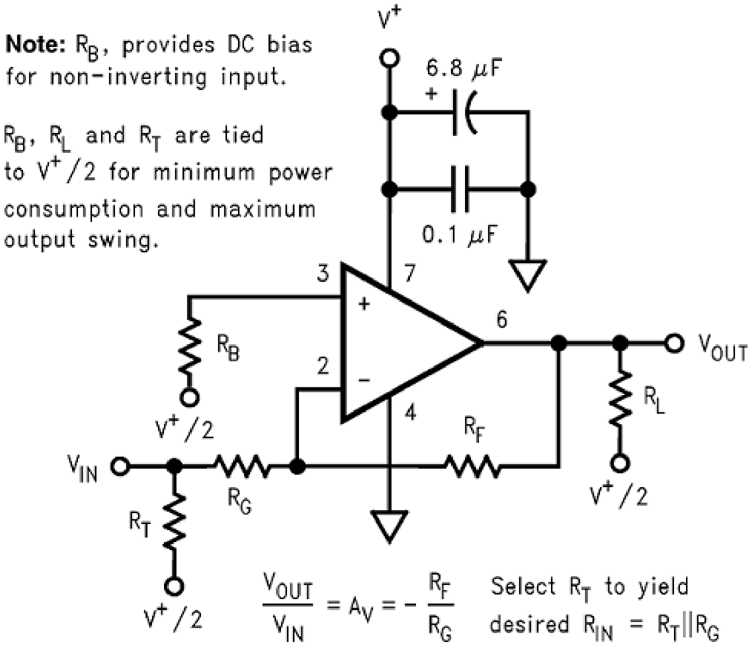


Figure 34. Single Supply Inverting

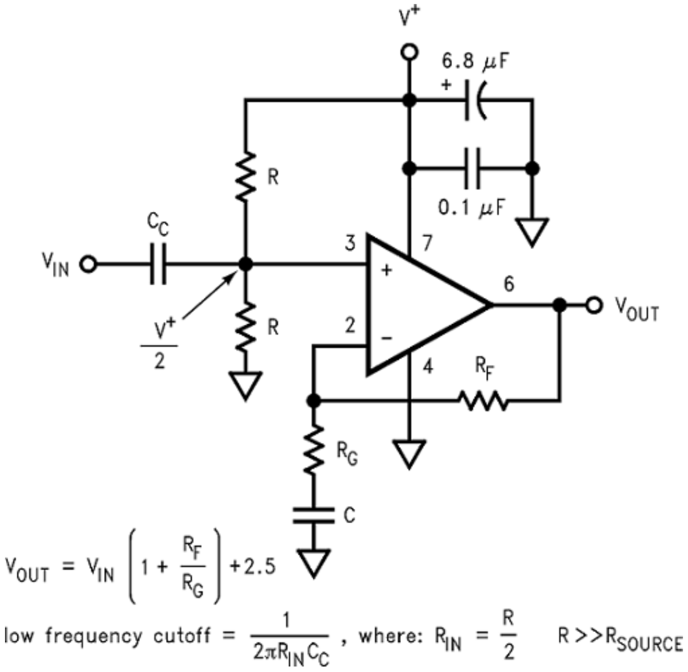


Figure 35. AC Coupled Non-Inverting

GAIN BANDWIDTH PRODUCT

The LMH6609 is a voltage feedback amplifier, whose closed-loop bandwidth is approximately equal to the gain-bandwidth product (GBP) divided by the gain (A_V). For gains greater than 5, A_V sets the closed-loop bandwidth of the LMH6609.

$$\text{CLOSED LOOP BANDWIDTH} = \frac{\text{GBP}}{A_V}$$

$$A_V = \frac{(R_F + R_G)}{R_G}$$

$$\text{GBP} = 240\text{MHz} \tag{2}$$

For Gains less than 5, refer to the frequency response plots to determine maximum bandwidth. For large signal bandwidth the slew rate is a more accurate predictor of bandwidth.

$$f_{MAX} = \frac{S_R}{2\pi\ V_P} \tag{3}$$

Where f_{MAX} = bandwidth, S_R = Slew rate and V_P = peak amplitude.

OUTPUT DRIVE AND SETTLING TIME PERFORMANCE

The LMH6609 has large output current capability. The 100mA of output current makes the LMH6609 an excellent choice for applications such as:

- Video Line Drivers
- Distribution Amplifiers

When driving a capacitive load or coaxial cable, include a series resistance R_{OUT} to back match or improve settling time. Refer to the Driving Capacitive Loads section for guidance on selecting an output resistor for driving capacitive loads.

EVALUATION BOARDS

TI offers the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the data sheet plots were measured with these boards.

Device	Package	Board Part #
LMH6609MA	SOIC	LMH730227
LMH6609MF	SOT-23	LMH730216

CIRCUIT LAYOUT CONSIDERATION

A proper printed circuit layout is essential for achieving high frequency performance. TI provides evaluation boards for the LMH6609 as shown above. These boards were laid out for optimum, high-speed performance. The ground plane was removed near the input and output pins to reduce parasitic capacitance. Also, all trace lengths were minimized to reduce series inductances.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. 10µF tantalum and .01µF capacitors are recommended on both supplies (from supply to ground). In addition, a 0.1µF ceramic capacitor can be added from V^+ to V^- to aid in second harmonic suppression.

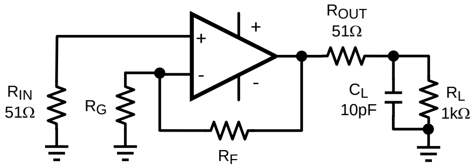


Figure 36. Driving Capacitive Loads with R_{OUT} for Improved Stability

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Figure 36 shows the use of a series output resistor, R_{OUT} as it might be applied when driving an analog to digital converter. The charts "Suggested R_O vs. Cap Load" in the Typical Performance Section give a recommended value for mitigating capacitive loads. The values suggested in the charts are selected for .5dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_O can be reduced slightly from the recommended values. There will be amplitude lost in the series resistor unless the gain is adjusted to compensate; this effect is most noticeable with heavy resistive loads.

COMPONENT SELECTION AND FEEDBACK RESISTOR

Surface mount components are highly recommended for the LMH6609. Leaded components will introduce unpredictable parasitic loading that will interfere with proper device operation. Do not use wire wound resistors.

The LMH6609 operates best with a feedback resistor of approximately 250Ω for all gains of +2 and greater and for −1 and less. With lower gains in particular, large value feedback resistors will exaggerate the effects of parasitic capacitances and may lead to ringing on the pulse response and frequency response peaking. Large value resistors also add undesirable thermal noise. Feedback resistors that are much below 100Ω will load the output stage, which will reduce voltage output swing, increase device power dissipation, increase distortion and reduce current available for driving the load.

In the buffer configuration the output should be shorted directly to the inverting input. This feedback does not load the output stage because the inverting input is a high impedance point and there is no gain set resistor to ground.

OPTIMIZING DC ACCURACY

The LMH6609 offers excellent DC accuracy. The well-matched inputs of this amplifier allows even better performance if care is taken to balance the impedances seen by the two inputs. The parallel combination of the gain setting R_G and feedback R_F resistors should be equal to R_{SEQ}, the resistance of the source driving the op amp in parallel with any terminating Resistor (See Figure 32). Combining this with the non inverting gain equation gives the following parameters:

$R_F = A_{VRSEQ}$

$R_G = R_F/(A_V - 1)$

For Inverting gains the bias current cancellation is accomplished by placing a resistor R_B on the non-inverting input equal in value to the resistance seen by the inverting input (See Figure 33). $R_B = R_F \parallel (R_G + R_S)$

The additional noise contribution of R_B can be minimized by the use of a shunt capacitor (not shown).

POWER DISSIPATION

The LMH6609 has the ability to drive large currents into low impedance loads. Some combinations of ambient temperature and device loading could result in device overheating. For most conditions peak power values are not as important as RMS powers. To determine the maximum allowable power dissipation for the LMH6609 use the following formula:

$$P_{MAX} = (150^{o} - T_{AMB})/\theta_{JA} \quad (4)$$

Where T_{AMB} = Ambient temperature (°C) and θJA = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package θJA is 148°C/W, for the SOT-23 it is 250°C/W. 150ºC is the absolute maximum limit for the internal temperature of the device.

Either forced air cooling or a heat sink can greatly increase the power handling capability for the LMH6609.

VIDEO PERFORMANCE

The LMH6609 has been designed to provide good performance with both PAL and NTSC composite video signals. The LMH6609 is specified for PAL signals. NTSC performance is typically marginally better due to the lower frequency content of the signal. Performance degrades as the loading is increased, therefore best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. This means that the device should be configured for a gain of 2 in order to have a net gain of 1 after the terminating resistor. (See Figure 37)

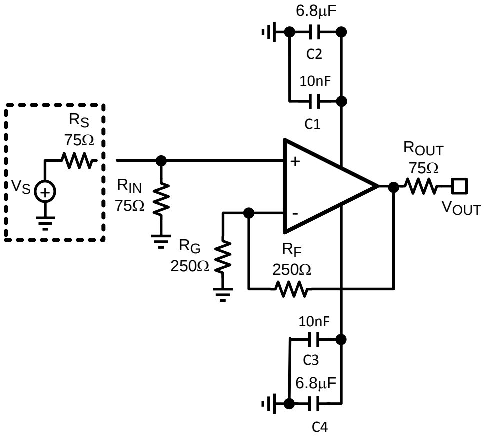


Figure 37. Typical Video Application

ESD PROTECTION

The LMH6609 is protected against electrostatic discharge (ESD) on all pins. The LMH6609 will survive 2000V Human Body model or 200V Machine model events.

Under closed loop operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes may be evident. For instance, if the amplifier is powered down and a large input signal is applied the ESD diodes will conduct.

TRANSIMPEDANCE AMPLIFIER

The low input current noise and unity gain stability of the LMH6609 make it an excellent choice for transimpedance applications. Figure 38 illustrates a low noise transimpedance amplifier that is commonly implemented with photo diodes. R_F sets the transimpedance gain. The photo diode current multiplied by R_F determines the output voltage.

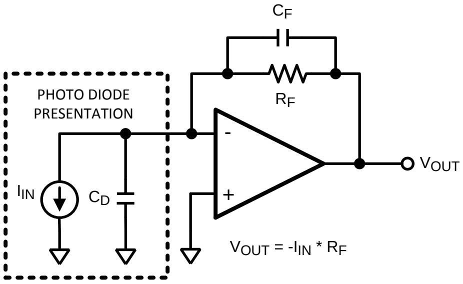


Figure 38. Transimpedance Amplifier

The capacitances are defined as:

- C_D = Equivalent Diode Capacitance
- C_F = Feedback Capacitance

The feedback capacitor is used to give optimum flatness and stability. As a starting point the feedback capacitance should be chosen as ½ of the Diode capacitance. Lower feedback capacitors will peak frequency response.

Rectifier

The large bandwidth of the LMH6609 allows for high-speed rectification. A common rectifier topology is shown in Figure 39. R_1 and R_2 set the gain of the rectifier.

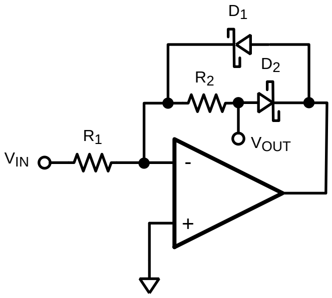


Figure 39. Rectifier Topology

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	**Page**
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6609MA	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH66 09MA	Samples
LMH6609MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 09MA	Samples
LMH6609MAX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMH66 09MA	Samples
LMH6609MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 09MA	Samples
LMH6609MF	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A89A	Samples
LMH6609MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A89A	Samples
LMH6609MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A89A	Samples
LMH6609MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A89A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

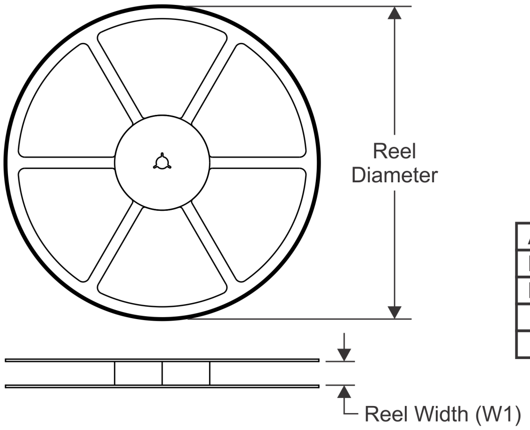
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

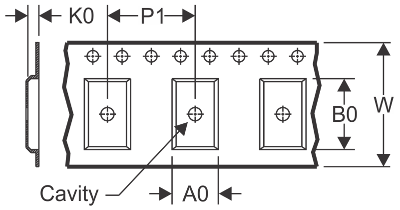
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

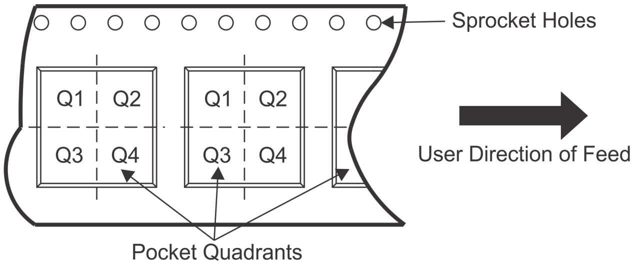


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

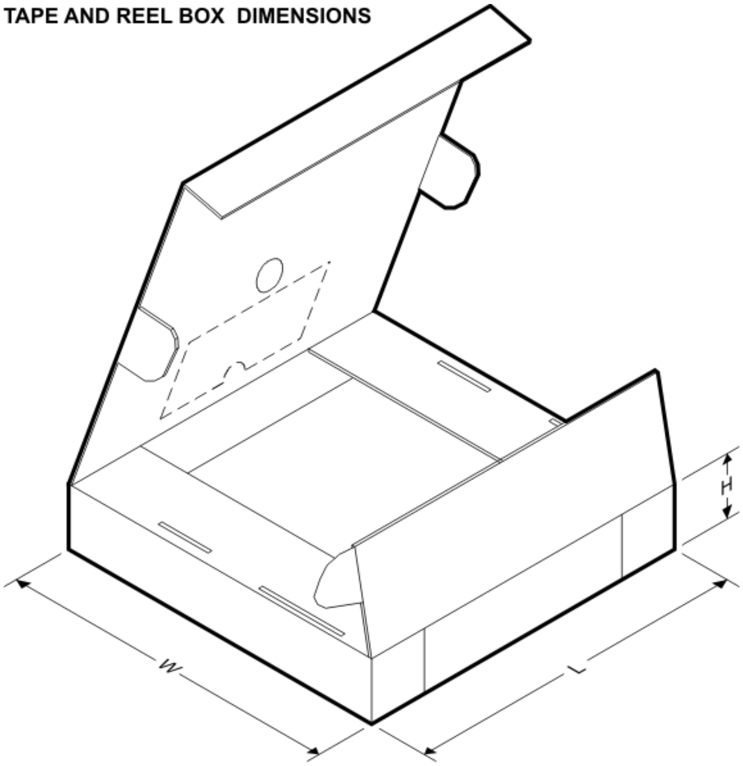
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6609MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6609MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6609MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6609MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6609MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6609MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

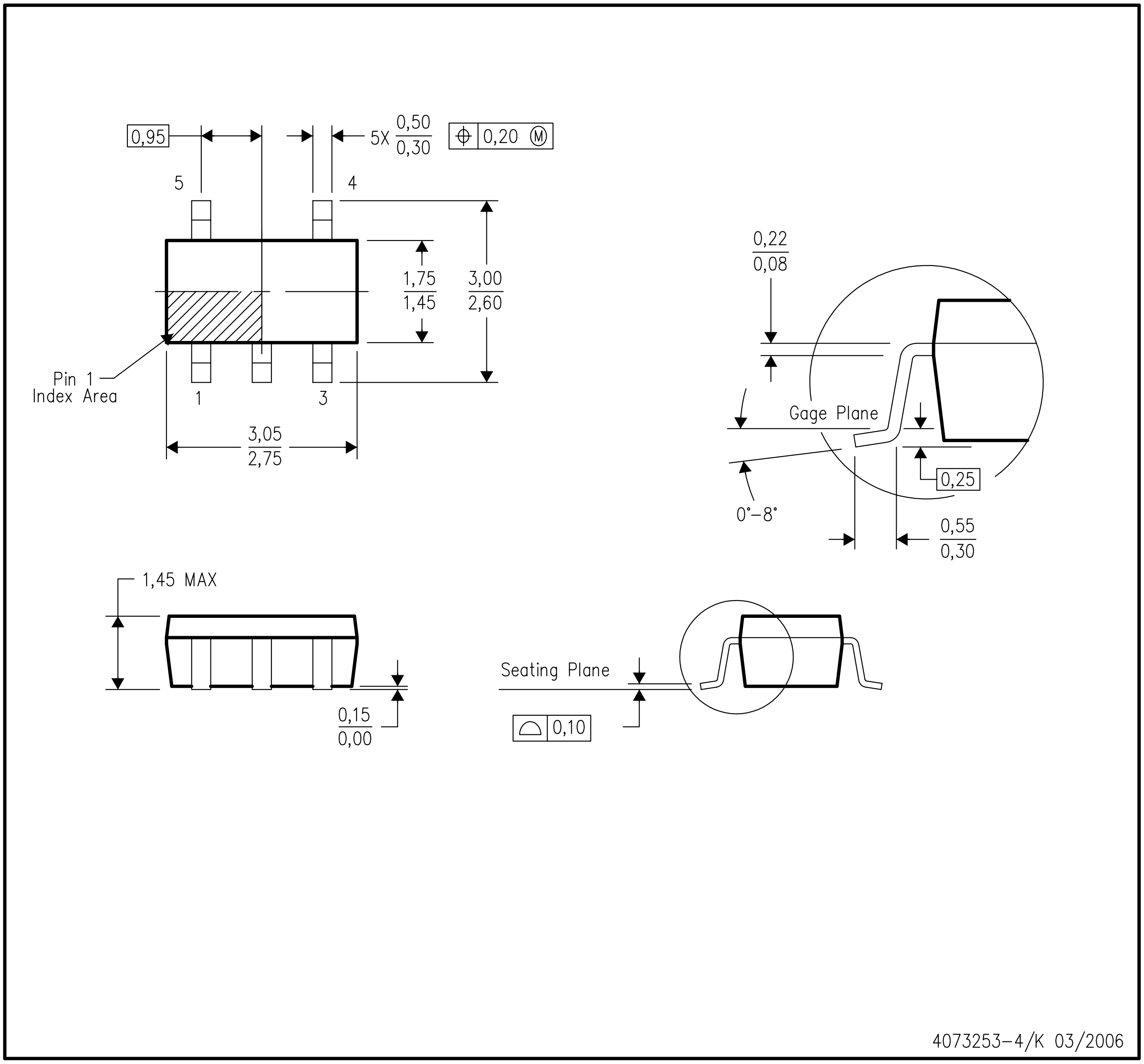
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

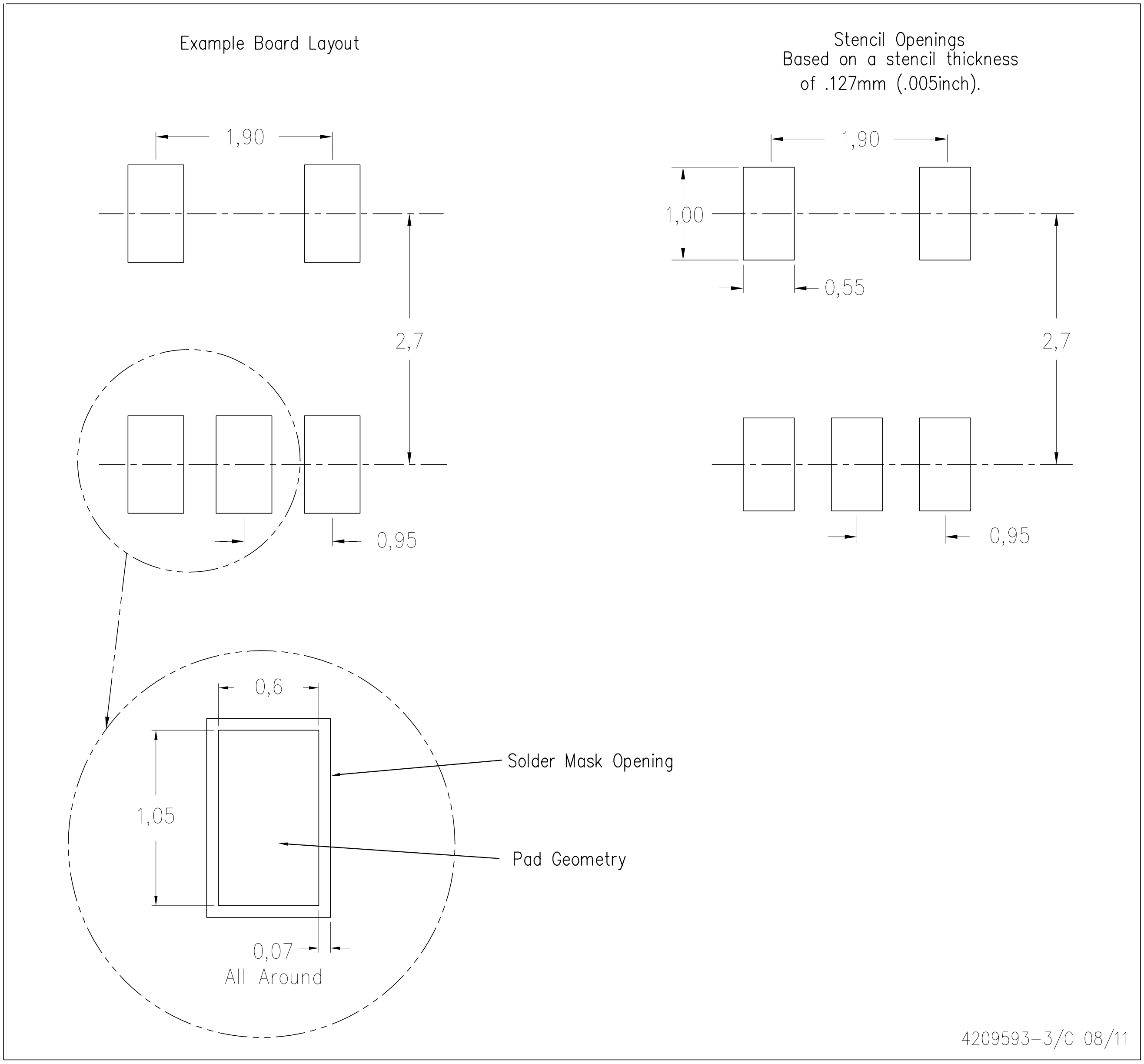
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6609MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6609MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6609MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6609MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6609MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6609MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



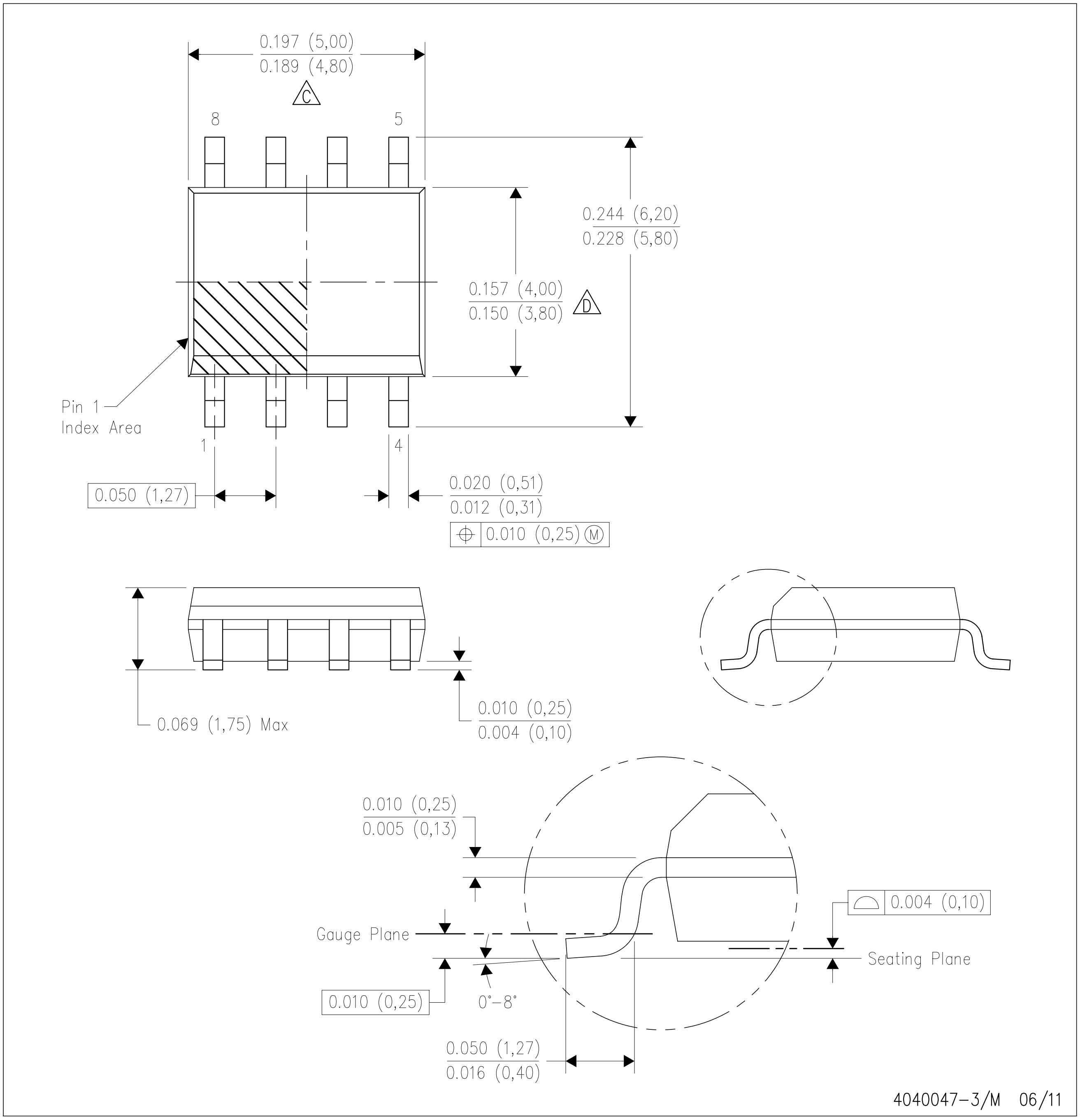
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

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