

LM98725 3 Channel, 16-Bit, 81 MSPS Analog Front End with LVDS/CMOS Output, Integrated CCD/CIS Sensor Timing Generator and Spread Spectrum Clock Generation

Check for Samples: [LM98725](#)

FEATURES

- LVDS/CMOS Outputs
- LVDS/CMOS/Crystal Clock Source with PLL Multiplication
- Integrated Flexible Spread Spectrum Clock Generation
- CDS or S/H Processing for CCD or CIS Sensors
- Independent Gain/Offset Correction for Each Channel
- Automatic per-Channel Gain and Offset Calibration
- Programmable Input Clamp Voltage
- Flexible CCD/CIS Sensor Timing Generator

KEY SPECIFICATIONS

- **Maximum Input Level**
 - 1.2 or 2.4 Volt Modes
 - (Both with + or - Polarity Option)
- **ADC Resolution: 16-Bit**
- **ADC Sampling Rate: 81 MSPS**
- **INL: +17/- 28 LSB (typ)**
- **Channel Sampling Rate: 30/30/27 MSPS**
- **PGA Gain Steps: 256 Steps**
- **PGA Gain Range: 0.62 to 8.3x**
- **Analog DAC Resolution: +/-9 Bits**
- **Analog DAC Range: +/-307mV or +/-614mV**
- **Digital DAC Resolution: +/-6 Bits**
- **Digital DAC Range: -2048 LSB to + 2016 LSB**
- **SNR: -74dB (@0dB PGA Gain)**
- **Power Dissipation: 755mW (LVDS)**
- **Operating Temp: 0 to 70°C**
- **Supply Voltage: 3.3V Nominal (3.0V to 3.6V Range)**

APPLICATIONS

- **Multi-Function Peripherals**
- **High-speed Currency/Check Scanners**
- **Flatbed or Handheld Color Scanners**
- **High-speed Document Scanners**

DESCRIPTION

The LM98725 is a fully integrated, high performance 16-Bit, 81 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative architecture utilizing Correlated Double Sampling (CDS), typically employed with CCD arrays, or Sample and Hold (S/H) inputs (for higher speed CCD or CMOS image sensors). The signal paths utilize 8 bit Programmable Gain Amplifiers (PGA), a +/-9-Bit offset correction DAC and independently controlled Digital Black Level correction loops for each input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for each of the three analog inputs. The signals are then routed to a 81MHz high performance analog-to-digital converter (ADC). The fully differential processing channel shows exceptional noise immunity, having a very low noise floor of -74dB. The 16-bit ADC has excellent dynamic performance making the LM98725 transparent in the image reproduction chain.

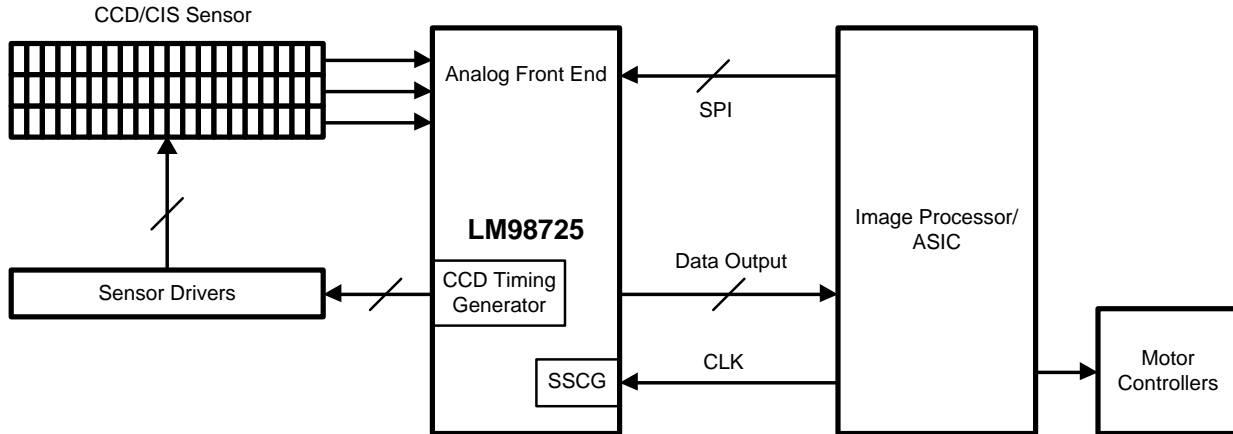
A very flexible integrated Spread Spectrum Clock Generation (SSCG) modulator is included to assist with EM compliance and reduce system costs.



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System Block Diagram



LM98725 Overall Chip Block Diagram

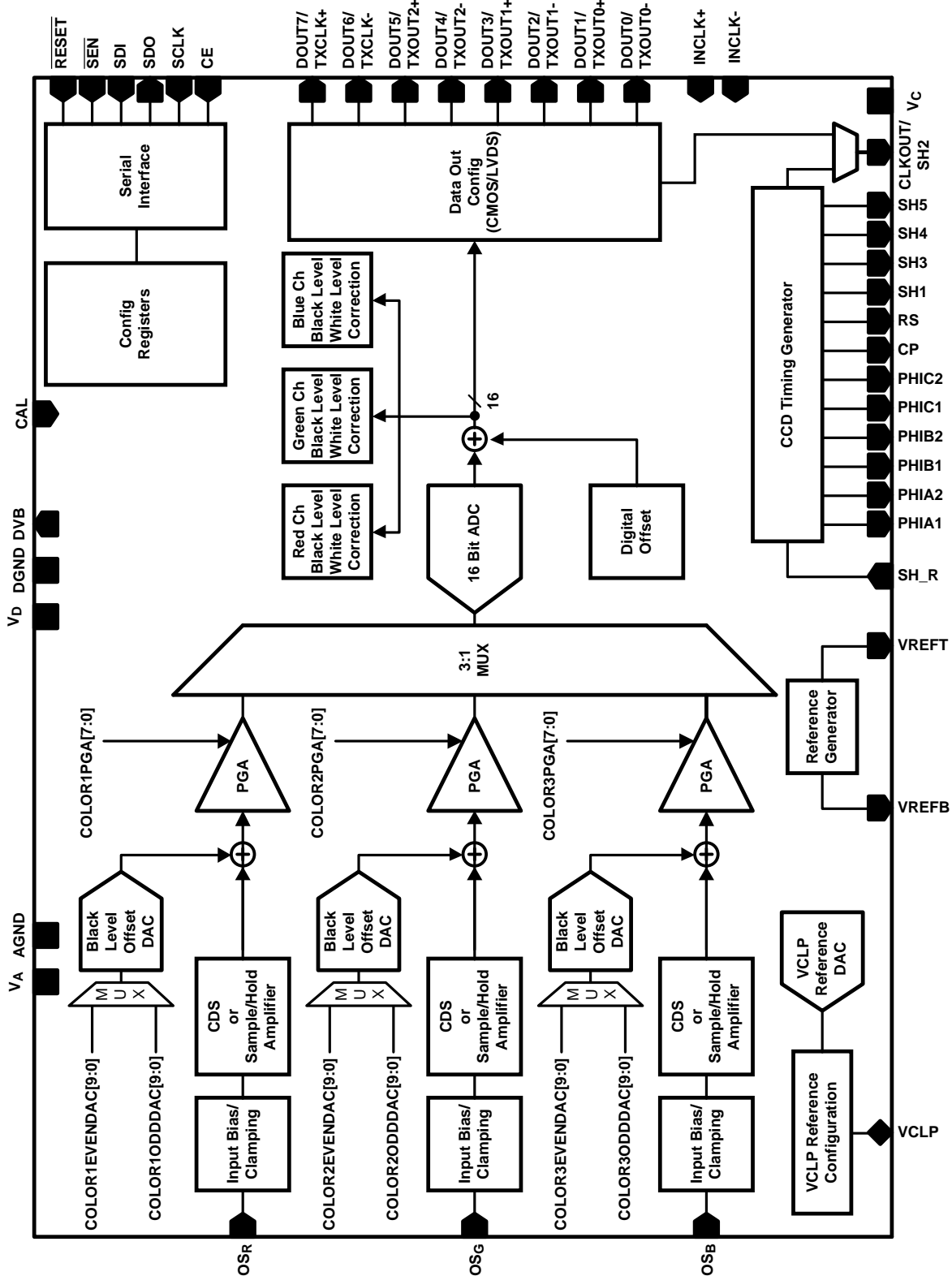
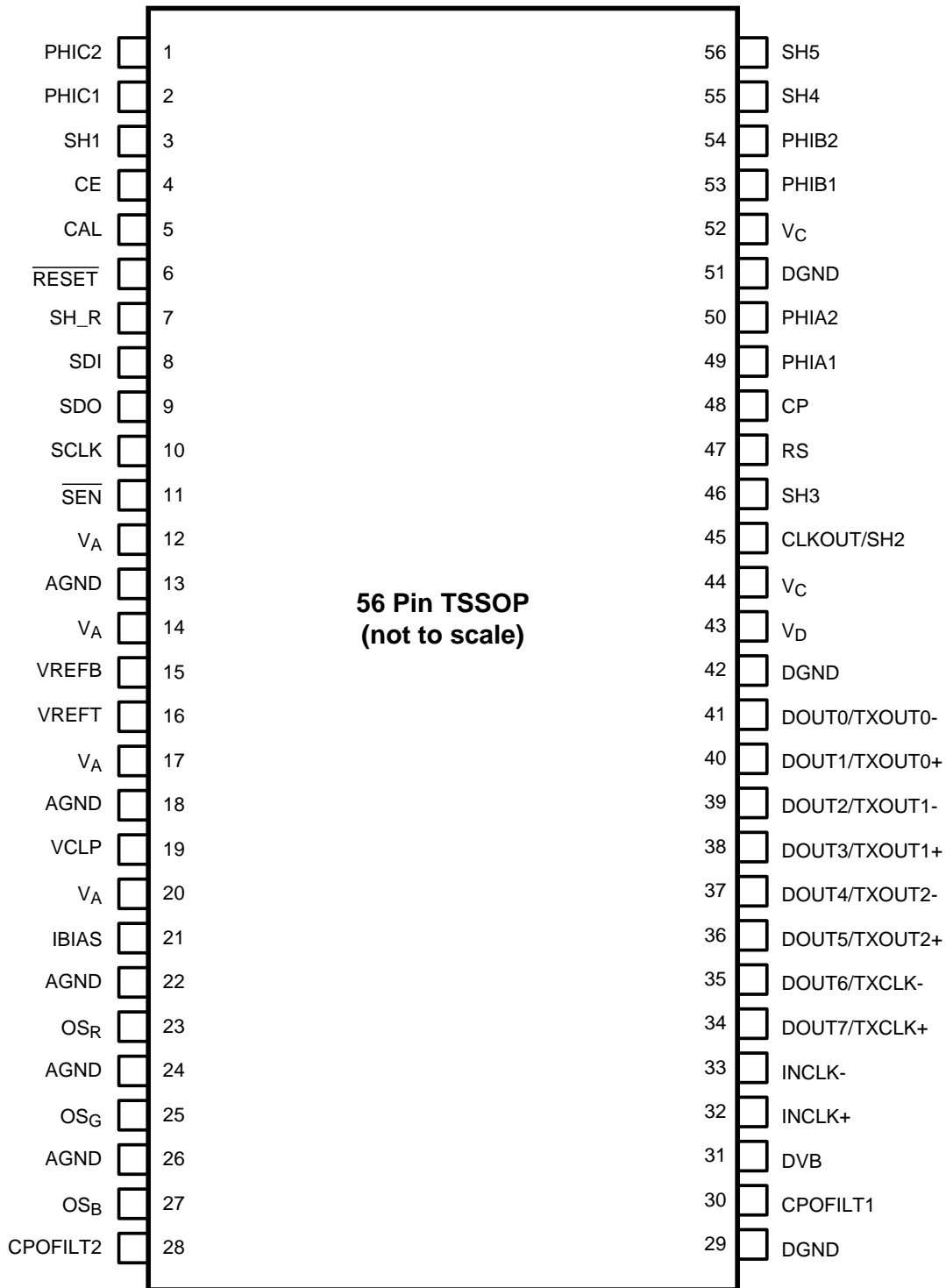


Figure 1. Chip Block Diagram

LM98725 Pin Out Diagram



**Figure 2. TSSOP Package
See Package Number DGG0056A**

Typical Application Diagram

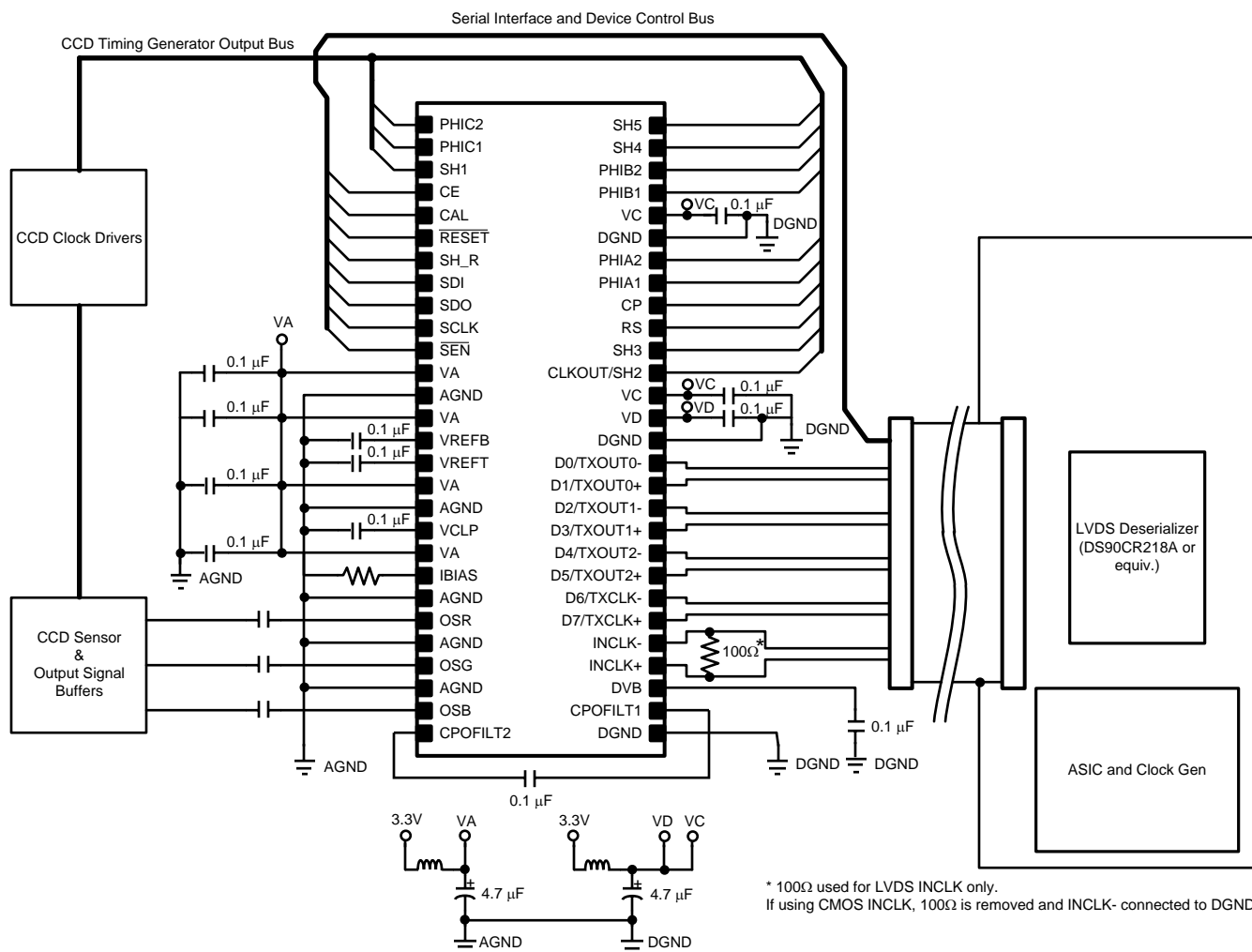


Figure 3. Typical Application Diagram

Pin Descriptions

| Pin | Name | I/O | Typ | Res | Description | |
|-----|---------------------------|-----|-----|-----|---|----------------|
| 1 | PHIC2 | O | D | PU | Configurable high speed sensor timing output. | |
| 2 | PHIC1 | O | D | PD | Configurable high speed sensor timing output. | |
| 3 | SH1 | O | D | PU | Configurable low speed sensor timing output. | |
| 4 | CE | I | D | | Chip Serial Interface Address Setting Input | |
| | | | | | CE Level | Address |
| | | | | | V _D | 01 |
| | | | | | Float | 10 |
| | DGND | 00 | | | | |
| 5 | CAL | I | D | PD | Initiate calibration sequence. Leave unconnected or tie to DGND if unused. | |
| 6 | $\overline{\text{RESET}}$ | I | D | PU | Active-low master reset. NC when function not being used. | |
| 7 | SH_R | I | D | PD | External request for an SH interval. | |
| 8 | SDI | I | D | PD | Serial Interface Data Input. | |
| 9 | SDO | O | D | | Serial Interface Data Output. | |
| 10 | SCLK | I | D | PD | Serial Interface shift register clock. | |
| 11 | $\overline{\text{SEN}}$ | I | D | PU | Active-low chip enable for the Serial Interface. | |
| 12 | V _A | | P | | Analog power supply. Bypass voltage source with 4.7 μ F and pin with 0.1 μ F to AGND. | |
| 13 | AGND | | P | | Analog ground return. | |
| 14 | V _A | | P | | Analog power supply. Bypass voltage source with 4.7 μ F and pin with 0.1 μ F to AGND. | |
| 15 | VREFB | O | A | | Bottom of ADC reference. Bypass with a 0.1 μ F capacitor to ground. | |
| 16 | VREFT | O | A | | Top of ADC reference. Bypass with a 0.1 μ F capacitor to ground. | |
| 17 | V _A | | P | | Analog power supply. Bypass voltage source with 4.7 μ F and pin with 0.1 μ F to AGND. | |
| 18 | AGND | | P | | Analog ground return. | |
| 19 | VCLP | IO | A | | Input Clamp Voltage. Normally bypassed with a 0.1 μ F , and a 4.7 μ F capacitor to AGND. An external reference voltage may be applied to this pin. | |
| 20 | V _A | | P | | Analog power supply. Bypass voltage source with 4.7 μ F and pin with 0.1 μ F to AGND. | |
| 21 | IBIAS | O | A | | Bias setting pin. Connect a 9.0 kOhm 1% resistor to AGND. | |
| 22 | AGND | | P | | Analog ground return. | |
| 23 | OS _R | I | A | | Analog input signal. Typically sensor Red output AC-coupled thru a capacitor. | |
| 24 | AGND | | P | | Analog ground return. | |
| 25 | OS _G | I | A | | Analog input signal. Typically sensor Green output AC-coupled thru a capacitor. | |
| 26 | AGND | | P | | Analog ground return. | |
| 27 | OS _B | I | A | | Analog input signal. Typically sensor Blue output AC-coupled thru a capacitor. | |
| 28 | CPOFILT2 | | A | | Charge Pump Filter Capacitor. Bypass this supply pin with a 0.1 μ F capacitor to CPOFILT1. | |
| 29 | DGND | | P | | Digital ground return. | |
| 30 | CPOFILT1 | | A | | Charge Pump Filter Capacitor. Bypass this supply pin with a 0.1 μ F capacitor to CPOFILT2. | |
| 31 | DVB | O | D | | Digital Core Voltage bypass. Not an input. Bypass with 0.1 μ F capacitor to DGND. | |
| 32 | INCLK+ | I | D | | Clock Input. Non-Inverting input for LVDS clocks or CMOS clock input. CMOS clock is selected when pin 29 is held at DGND, otherwise clock is configured for LVDS operation. | |
| 33 | INCLK- | I | D | | Clock Input. Inverting input for LVDS clocks, connect to DGND for CMOS clock. | |
| 34 | DOU7/ TXCLK+ | O | D | | Bit 7 of the digital video output bus in CMOS Mode, LVDS Frame Clock+ in LVDS Mode. | |
| 35 | DOU6/ TXCLK- | O | D | | Bit 6 of the digital video output bus in CMOS Mode, LVDS Frame Clock- in LVDS Mode. | |
| 36 | DOU5/ TXOUT2+ | O | D | | Bit 5 of the digital video output bus in CMOS Mode, LVDS Data Out2+ in LVDS Mode. | |
| 37 | DOU4/ TXOUT2- | O | D | | Bit 4 of the digital video output bus in CMOS Mode, LVDS Data Out2- in LVDS Mode. | |

Pin Descriptions (continued)

| Pin | Name | I/O | Typ | Res | Description |
|-----|-------------------|-----|-----|-----|--|
| 38 | DOUT3/ TXOUT1+ | O | D | | Bit 3 of the digital video output bus in CMOS Mode, LVDS Data Out1+ in LVDS Mode. |
| 39 | DOUT2/ TXOUT1- | O | D | | Bit 2 of the digital video output bus in CMOS Mode, LVDS Data Out1- in LVDS Mode. |
| 40 | DOUT1/ TXOUT0+ | O | D | | Bit 1 of the digital video output bus in CMOS Mode, LVDS Data Out0+ in LVDS Mode. |
| 41 | DOUT0/ TXOUT0- | O | D | | Bit 0 of the digital video output bus in CMOS Mode, LVDS Data Out0- in LVDS Mode. |
| 42 | DGND | O | D | PD | Configurable sensor control output. |
| 43 | V _D | | P | | Power supply for the digital circuits. Bypass this supply pin with 0.1µF capacitor. A single 4.7µF capacitor should be used between the supply and the VD, VR and VC pins. |
| 44 | V _C | | P | | Power supply for the sensor control outputs. Bypass this supply pin with 0.1µF capacitor. |
| 45 | CLKOUT/SH2 | O | D | | Output clock for registering output data when using CMOS outputs, or a configurable low speed sensor timing output. |
| 46 | SH3 | O | D | | Configurable low speed sensor timing output. |
| 47 | RS | O | D | | Configurable high speed sensor timing output. |
| 48 | CP | O | D | | Configurable high speed sensor timing output. |
| 49 | PHIA1 | O | D | | Configurable high speed sensor timing output. |
| 50 | PHIA2 | O | D | | Configurable high speed sensor timing output. |
| 51 | DGND | | P | | Digital ground return. |
| 52 | V _C | | P | | Power supply for the sensor control outputs. Bypass this supply pin with 0.1µF capacitor. |
| 53 | PHIB1 | O | D | | Configurable high speed sensor timing output. |
| 54 | PHIB2 | O | D | | Configurable high speed sensor timing output. |
| 55 | SH4 | O | D | | Configurable low speed sensor timing output. |
| 56 | SH5 | O | D | | Configurable low speed sensor timing output. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

| | | |
|--|------------------|----------------------------------|
| Supply Voltage (V _A , V _R , V _D , V _C) | | 4.2V |
| Voltage on Any Input Pin (Not to exceed 4.2V) | | -0.3V to (V _A + 0.3V) |
| Voltage on Any Output Pin (except DVB and not to exceed 4.2V) | | -0.3V to (V _A + 0.3V) |
| DVB Output Pin Voltage | | 2.0V |
| Input Current at any pin other than Supply Pins ⁽⁴⁾ | | ±25 mA |
| Package Input Current (except Supply Pins) ⁽⁴⁾ | | ±50 mA |
| Maximum Junction Temperature (T _A) | | 150°C |
| Thermal Resistance (θ _{JA}) | | <66°C/W |
| Package Dissipation at T _A = 25°C ⁽⁵⁾ | | >1.89W |
| ESD Rating ⁽⁶⁾ | Human Body Model | 2500V |
| | Machine Model | 250V |
| Storage Temperature | | -65°C to +150°C |
| <i>Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.⁽⁷⁾</i> | | |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
- (2) All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.
- (5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = (T_{JMAX} - T_A)/θ_{JA}. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
- (6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
- (7) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings⁽¹⁾⁽²⁾

| | | |
|-----------------------------|--|------------------------------|
| Operating Temperature Range | | 0°C ≤ T _A ≤ +70°C |
| All Supply Voltage | | +3.0V to +3.6V |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
- (2) All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.

Electrical Characteristics

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.⁽¹⁾

| Parameter | Test Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units | |
|---|--|--|--------------------|--------------------|---------|---------|
| CMOS Digital Input DC Specifications (RESETb, SH_R, SCLK, SENb) | | | | | | |
| V_{IH} | Logical "1" Input Voltage | 2.0 | | | V | |
| V_{IL} | Logical "0" Input Voltage | | | 0.8 | V | |
| V_{IHYST} | Logic Input Hysteresis | | 0.6 | | | |
| I_{IH} | Logical "1" Input Current | $V_{IH} = V_D$ RESET, SEN SH_R, SCLK, SDI, CAL CE | | 100 | nA | |
| | | | | 65 | μA | |
| | | | | 30 | nA | |
| I_{IL} | Logical "0" Input Current | $V_{IL} = DGND$ RESET, SEN SH_R, SCLK, SDI, CAL CE | | -65 | μA | |
| | | | | -100 | nA | |
| | | | | -30 | μA | |
| CMOS Digital Output DC Specifications (SH1 to SH5, RS, CP, PHIA, PHIB, PHIC) | | | | | | |
| V_{OH} | Logical "1" Output Voltage | $I_{OUT} = -0.5mA$ | 3.0 | | V | |
| V_{OL} | Logical "0" Output Voltage | $I_{OUT} = 1.6mA$ | | 0.21 | V | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = DGND$ | | 18 | mA | |
| | | $V_{OUT} = V_D$ | | -25 | | |
| I_{OZ} | CMOS Output TRI-STATE Current | $V_{OUT} = DGND$ | | 20 | nA | |
| | | $V_{OUT} = V_D$ | | -25 | | |
| CMOS Digital Output DC Specifications (CMOS Data Outputs) | | | | | | |
| V_{OH} | Logical "1" Output Voltage | $I_{OUT} = -0.5mA$ | | 2.3 | V | |
| V_{OL} | Logical "0" Output Voltage | $I_{OUT} = 1.6mA$ | | 0.12 | V | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = DGND$ | | 12 | mA | |
| | | $V_{OUT} = V_D$ | | -14 | | |
| I_{OZ} | CMOS Output TRI-STATE Current | $V_{OUT} = DGND$ | | 20 | nA | |
| | | $V_{OUT} = V_D$ | | -25 | | |
| LVDS/CMOS Clock Receiver DC Specifications (INCLK+ and INCLK- Pins) | | | | | | |
| V_{IHL} | Differential LVDS Clock High Threshold Voltage | $R_L = 100\Omega$ V_{CM} (LVDS Input Common Mode Voltage) = 1.25V | | | 200 | mV |
| V_{ILL} | Differential LVDS Clock Low Threshold Voltage | | -200 | | | mV |
| V_{IHC} | CMOS Clock High Threshold Voltage | INCLK- = DGND | 2.0 | | | V |
| V_{ILC} | CMOS Clock Low Threshold Voltage | | | | 0.8 | V |
| I_{IHL} | CMOS Clock Input High Current | | | 230 | 260 | μA |
| I_{ILC} | CMOS Clock Input Low Current | | -135 | -120 | | μA |

- (1) The analog inputs are protected as shown in [Figure 4](#). Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per [Note 4](#) under the Absolute Maximum Ratings Table. However, input errors will be generated if the input goes above V_A and below AGND.
- (2) Test limits are specified to Texas Instruments' AOQL (Average Outgoing Quality Level).
- (3) Typical figures are at $T_A = 25^\circ C$, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

Electrical Characteristics (continued)

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.⁽¹⁾

| Parameter | | Test Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|--|--|--|--------------------|--------------------|--------------------|----------|
| LVDS Output DC Specifications | | | | | | |
| V_{OD} | Differential Output Voltage | $R_L = 100\Omega$ | 280 | 390 | 490 | mV |
| V_{OS} | LVDS Output Offset Voltage | | 1.08 | 1.20 | 1.33 | V |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V$, $R_L = 100\Omega$ | | 8.5 | | mA |
| Power Supply Specifications | | | | | | |
| IA | VA Analog Supply Current | LVDS Output Data Format | | 152 | 180 | mA |
| | | LVDS Output Data Format (Powerdown) | | 3.6 | 6 | mA |
| | | CMOS Output Data Format (40 MHz) | | 136 | 168 | mA |
| ID | VD Digital Output Driver Supply Current | LVDS Output Data Format | | 76 | 94 | mA |
| | | LVDS Output Data Format (Powerdown) | | 8.5 | 17 | mA |
| | | CMOS Output Data Format (ATE Loading of CMOS Outputs > 50 pF) (40 MHz) | | 46 | 68 | mA |
| IC | VC CCD Timing Generator Output Driver Supply Current | Typical sensor outputs: SH1-SH5, PHIA, PHIB, PHIC, RS, CP (ATE Loading of CMOS Outputs > 50pF) | | 1 | 4 | mA |
| PWR | Average Power Dissipation | LVDS Output Data Format | | 755 | 885 | mW |
| | | LVDS Output Data Format (Powerdown) | | 40 | 70 | mW |
| | | CMOS Output Data Format (ATE Loading of CMOS Outputs > 50pF) (40 MHz) | | 600 | 740 | mW |
| Input Sampling Circuit Specifications | | | | | | |
| V_{IN} | Input Voltage Level | CDS Gain=1x, PGA Gain=1x CDS Gain=2x, PGA Gain= 1x | | 2.3 1.22 | | Vp-p |
| I_{IN_SH} | Sample and Hold Mode Input Leakage Current | Source Followers Off CDS Gain = 1x $OS_X = VA$ ($OS_X = AGND$) | | 32 (-200) | 50 (-165) | μA |
| | | Source Followers Off CDS Gain = 2x $OS_X = VA$ ($OS_X = AGND$) | (-290) | 55 (-240) | 70 | μA |
| | | Source Followers On CDS Gain = 2x $OS_X = VA$ ($OS_X = AGND$) | (-250) | 20 (-50) | 250 | nA |
| | | CDS Gain = 1x | | 2.5 | | pF |
| C_{SH} | Sample/Hold Mode Equivalent Input Capacitance | CDS Gain = 2x | | 4 | | pF |
| | | Source Followers Off | | 10 | 250 | nA |
| I_{IN_CDS} | CDS Mode | $OS_X = VA$ ($OS_X = AGND$) | (-250) | (-50) | | |
| | Input Leakage Current | | | | | |
| R_{CLPIN} | CLPIN Switch Resistance | | | 16 | 55 | Ω |
| | (OS_X to VCLP Node) | | | | | |

Electrical Characteristics (continued)

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.⁽¹⁾

| Parameter | Test Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|--|--|--|-----------------------------|--------------------|-------------------------|
| VCLP Reference Circuit Specifications | | | | | |
| V_{VCLP} | VCLP Voltage 000 | VCLP Voltage Setting = 000 | | 0.85VA | V |
| | VCLP Voltage 001 | VCLP Voltage Setting = 001 | | 0.9VA | V |
| | VCLP Voltage 010 | VCLP Voltage Setting = 010 | | 0.95VA | V |
| | VCLP Voltage 011 | VCLP Voltage Setting = 011 | | 0.6VA | V |
| | VCLP Voltage 100 | VCLP Voltage Setting = 100 | | 0.55VA | V |
| | VCLP Voltage 101 | VCLP Voltage Setting = 101 | | 0.4VA | V |
| | VCLP Voltage 110 | VCLP Voltage Setting = 110 | | 0.35VA | V |
| | VCLP Voltage 111 | VCLP Voltage Setting = 111 | | 0.15VA | V |
| I_{SC} | VCLP DAC Short Circuit Output Current | 0001 xxxxb VCLP Config. Register = | | 30 | mA |
| Black Level Offset DAC Specifications | | | | | |
| | Resolution | | | 10 | Bits |
| | Monotonicity | | Ensured by characterization | | |
| | Offset Adjustment Range Referred to AFE Input | CDS Gain = 1x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF | | -614 614 | mV |
| | | CDS Gain = 2x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF | | -307 307 | mV |
| | Offset Adjustment Range Referred to AFE Output | Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF | -17500 +16130 | | -16130 +17500 LSB |
| | DAC LSB Step Size | CDS Gain = 1x Referred to AFE Output | | 1.2 (32) | mV (LSB) |
| DNL | Differential Non-Linearity | | -0.84 | +0.74/ -0.37 | +2.4 LSB |
| INL | Integral Non-Linearity | | -2.5 | +0.72/ -0.56 | +2.5 LSB |
| PGA Specifications | | | | | |
| | Gain Resolution | | | 8 | Bits |
| | Monotonicity | | Ensured by characterization | | |
| | Maximum Gain | CDS Gain = 1x | 7.7 | 8.3 | 8.8 V/V |
| | | CDS Gain = 1x | 17.7 | 18.4 | 18.9 dB |
| | Minimum Gain | CDS Gain = 1x | 0.58 | 0.62 | 0.67 V/V |
| | | CDS Gain = 1x | -4.7 | -4.2 | -3.5 dB |
| | PGA Function | Gain (V/V) = (180/(277-PGA Code)) Gain (dB) = 20LOG10(180/(277-PGA Code)) | | | |
| | Channel Matching | Minimum PGA Gain Maximum PGA Gain | | 3 12.7 | % |
| ADC Specifications | | | | | |
| V_{REFT} | Top of Reference | | | 2.07 | V |
| V_{REFB} | Bottom of Reference | | | 0.89 | V |
| $V_{REFT} - V_{REFB}$ | Differential Reference Voltage | | 1.06 | 1.18 | 1.30 V |
| | Overrange Output Code | | | 65535 | |
| | Underrange Output Code | | | 0 | |

Electrical Characteristics (continued)

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.⁽¹⁾

| Parameter | Test Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units | |
|---|----------------------------|---------------------------------|--------------------|--------------------|-------|-----|
| Digital Offset “DAC” Specifications | | | | | | |
| Resolution | | | 7 | | Bits | |
| Digital Offset DAC LSB Step Size | Referred to AFE Output | | 32 | | LSB | |
| Offset Adjustment Range Referred to AFE Output | Min DAC Code = 7b0000000 | | -2048 | | LSB | |
| | Mid DAC Code = 7b1000000 | | 0 | | | |
| | Max DAC Code = 7b1111111 | | +2016 | | | |
| Full Channel Performance Specifications | | | | | | |
| DNL | Differential Non-Linearity | See ⁽⁴⁾ | -0.999 | +0.8/-0.7 | 2.5 | LSB |
| INL | Integral Non-Linearity | See ⁽⁴⁾ | -75 | +18/-25 | 75 | LSB |
| SNR | Total Output Noise | Minimum PGA Gain ⁽⁴⁾ | | -76 | | dB |
| | | | | | 10 | 26 |
| | | Maximum PGA Gain ⁽⁴⁾ | | -56 | | dB |
| | | | | | 96 | |
| Channel to Channel Crosstalk | Mode 3 | | 26 | | LSB | |
| | Mode 2 | | 17 | | | |

(4) This parameter ensured by design and characterization.

AC Timing Specifications

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.⁽¹⁾

| Parameter | Test Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|--|--------------------------------------|--------------------|--------------------|---|-----------|
| Input Clock Timing Specifications | | | | | |
| f_{INCLK} | INCLK = PIXCLK (Pixel Rate Clock) | 0.66 | | 27 (Mode 3) | MHz |
| | | 1 | | 30 (Mode 2) | |
| | | 1 | | 30 (Mode 1) | |
| | INCLK = ADCCLK (ADC Rate Clock) | 2 | | 81 (Mode 3) 60 (Mode 2) 30 (Mode 1) | MHz |
| T_{dc} | Input Clock Duty Cycle | 40/60 | 50/50 | 60/40 | % |
| Full Channel Latency Specifications | | | | | |
| t_{LAT3} | 3 Channel Mode Pipeline Delay | PIXPHASE0 | | 24 | T_{ADC} |
| | | PIXPHASE1 | | 23 1/2 | |
| | | PIXPHASE2 | | 23 | |
| | | PIXPHASE3 | | 22 1/2 | |
| t_{LAT2} | 2 Channel Mode Pipeline Delay | PIXPHASE0 | | 21 | T_{ADC} |
| | | PIXPHASE1 | | 20 1/2 | |
| | | PIXPHASE2 | | 20 | |
| | | PIXPHASE3 | | 19 1/2 | |

(1) The analog inputs are protected as shown in Figure 4. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per Note 4 under the Absolute Maximum Ratings Table. However, input errors will be generated if the input goes above V_A and below AGND.

(2) Test limits are specified to AOQL (Average Outgoing Quality Level).

(3) Typical figures are at $T_A = 25^\circ C$, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

AC Timing Specifications (continued)

The following specifications apply for $V_A = V_D = V_R = V_C = 3.3V$, $C_L = 10pF$, and $f_{INCLK} = 27MHz$ unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.⁽¹⁾

| Parameter | | Test Conditions | Min ⁽²⁾ | Typ ⁽³⁾ | Max ⁽²⁾ | Units |
|---|---|--|--------------------|--------------------|--------------------|-------------|
| t_{LAT1} | 1 Channel Mode Pipeline Delay | PIXPHASE0 | | 19 | | T_{ADC} |
| | | PIXPHASE1 | | 18 1/2 | | |
| | | PIXPHASE2 | | 18 | | |
| | | PIXPHASE3 | | 17 1/2 | | |
| SH_R Timing Specifications | | | | | | |
| t_{SHR_S} | SH_R Setup Time | | | 2 | | ns |
| t_{SHR_H} | SH_R Hold Time | | | 2 | | ns |
| LVDS Output Timing Specifications | | | | | | |
| TX_{pp0} | TXCLK to Pulse Position 0 | LVDS Output | -0.26 | 0 | 0.26 | ns |
| TX_{pp1} | TXCLK to Pulse Position 1 | Specifications not tested in production. Min/Max ensured by design, characterization and statistical analysis. | 1.50 | 1.76 | 2.02 | ns |
| TX_{pp2} | TXCLK to Pulse Position 2 | | 3.26 | 3.53 | 3.79 | ns |
| TX_{pp3} | TXCLK to Pulse Position 3 | | 5.03 | 5.29 | 5.55 | ns |
| TX_{pp4} | TXCLK to Pulse Position 4 | | 6.80 | 7.06 | 7.32 | ns |
| TX_{pp5} | TXCLK to Pulse Position 5 | | 8.56 | 8.82 | 9.08 | ns |
| TX_{pp6} | TXCLK to Pulse Position 6 | | 10.32 | 10.58 | 10.84 | ns |
| CMOS Output Timing Specifications | | | | | | |
| t_{CRDO} | CLKOUT Rising Edge to CMOS Output Data Transition | $f_{INCLK} = 40MHz$ INCLK = ADCCLK (ADC Rate Clock) | 2 | 4.5 | 9 | ns |
| Serial Interface Timing Specifications | | | | | | |
| f_{SCLK} | Input Clock Frequency | $f_{SCLK} \leq f_{INCLK}$ INCLK = PIXCLK (Pixel Rate Clock) Mode 3/2/1 | | | 27/30/30 | MHz |
| | | $f_{SCLK} \leq f_{INCLK}$ INCLK = ADCCLK (ADC Rate Clock) Mode 3/2/1 | | | 81/60/30 | MHz |
| | SCLK Duty Cycle | | | 50/50 | | ns |
| t_{IH} | Input Hold Time | | 1.5 | | | ns |
| t_{IS} | Input Setup Time | | 2.5 | | | ns |
| t_{SENSC} | SCLK Start Time After \overline{SEN} Low | | 1.5 | | | ns |
| t_{SCSEN} | \overline{SEN} High after last SCLK Rising Edge | | 2.5 | | | ns |
| t_{SEW} | \overline{SEN} Pulse Width | INCLK present | 6 | | | T_{INCLK} |
| | | INCLK stopped ⁽⁴⁾⁽⁵⁾ | 50 | | | ns |
| t_{OD} | Output Delay Time | | | 11 | 14 | ns |
| t_{HZ} | Data Output to High Z | | | | 0.5 | T_{SCLK} |

(4) If the input INCLK is divided down to a lower internal clock rate via the PLL, the parameter t_{SEW} will be increased by the same factor.

(5) When the Spread Spectrum Clock Generation feature is enabled, t_{SEW} should be increased by 1.

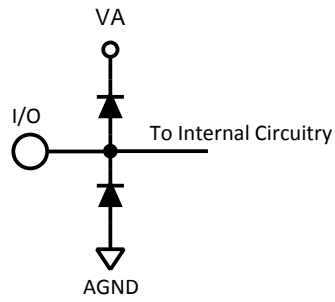


Figure 4.

REVISION HISTORY

| Changes from Revision D (April 2013) to Revision E | Page |
|--|--------------------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 14 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LM98725CCMT/NOPB | ACTIVE | TSSOP | DGG | 56 | 34 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | 0 to 70 | LM98725CCMT | Samples |
| LM98725CCMTX/NOPB | ACTIVE | TSSOP | DGG | 56 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | 0 to 70 | LM98725CCMT | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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