

LM723QML Voltage Regulator

Check for Samples: [LM723QML](#)

FEATURES

- 150 mA Output Current Without External Pass Transistor
- Output Currents in Excess of 10A Possible by Adding External Transistors
- Input Voltage 40V Max
- Output Voltage Adjustable from 2V to 37V
- Can be Used as Either a Linear or a Switching Regulator

DESCRIPTION

The LM723 is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723 is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

Connection Diagram

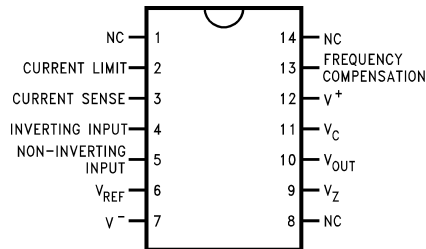
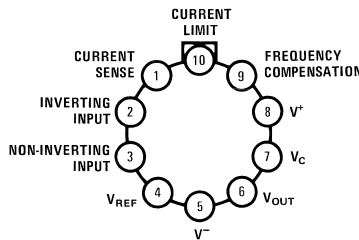


Figure 1. Dual-In-Line Package (Top View)
See Package J0014A



Note: Pin 5 connected to case.

Figure 2. Metal Can Package (Top View)
See Package LME0010C



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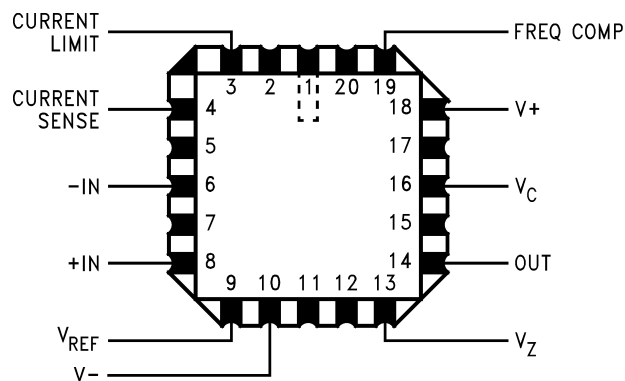
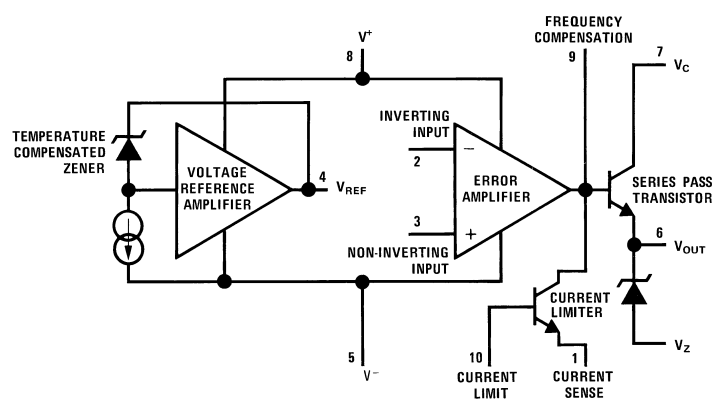


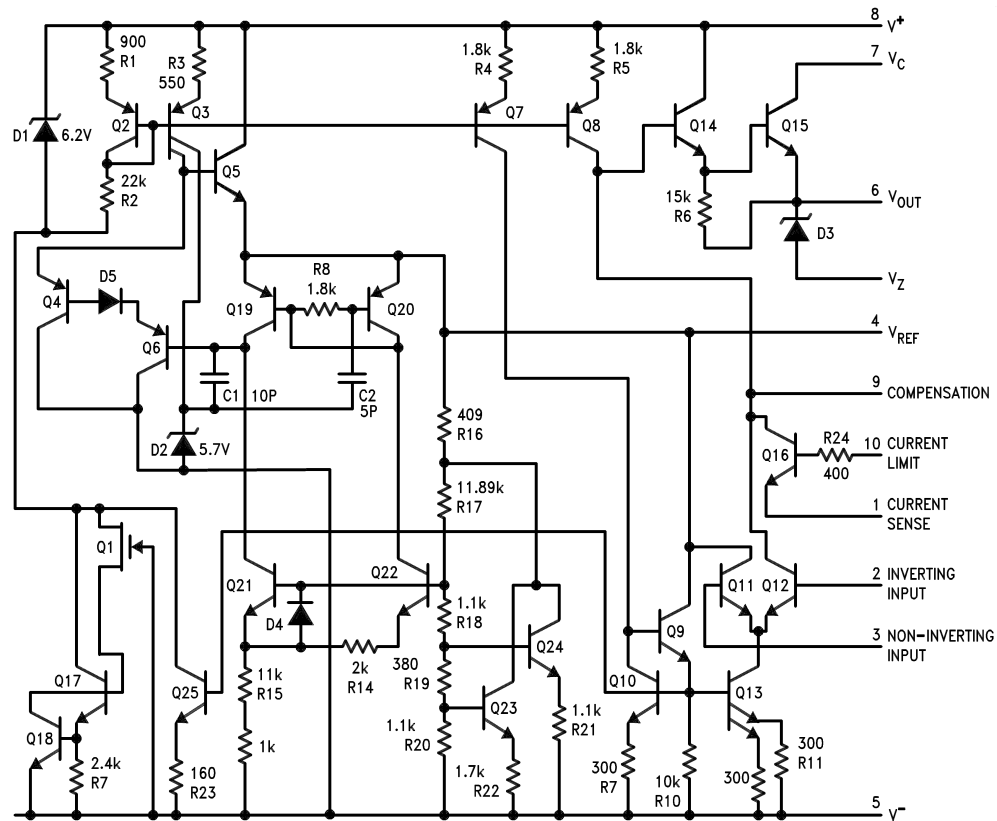
Figure 3. Top View
See Package NAJ0020A

Equivalent Circuit



(1) Pin numbers refer to metal can package.

Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Pulse Voltage from V ⁺ to V ⁻ (50 ms)			50V
Continuous Voltage from V ⁺ to V ⁻			40V
Input-Output Voltage Differential			40V
Maximum Amplifier Input Voltage	Either Input		8.5V
	Differential		5V
Current from V _Z			25 mA
Current from V _{REF}			15 mA
Internal Power Dissipation Metal Can ⁽²⁾	Cavity DIP ⁽²⁾		900 mW 800 mW
	LCCC ⁽²⁾		900 mW
Operating Temperature Range			-55°C ≤ T _A ≤ +125°C
Maximum T _J			+150°C
Storage Temperature Range			-65°C ≤ T _A ≤ +150°C
Lead Temperature (Soldering, 4 sec. max.)			300°C
Thermal Resistance	θ _{JA}	CDIP (Still Air)	100°C/W
		CDIP (500LF/ Min Air flow)	61°C/W
		Metal Can (Still Air)	156°C/W
		Metal Can (500LF/ Min Air flow)	89°C/W
		LCCC (Still Air)	96°C/W
		LCCC (500LF/ Min Air flow)	70°C/W
	θ _{JC}	CDIP	22°C/W
		Metal Can	37°C/W
		LCCC	27°C/W
ESD Tolerance ⁽³⁾			500V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For specified specifications and test conditions, see the Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is less. See derating curves for maximum power rating above 25°C .
- (3) Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Quality Conformance Inspection — MIL-STD-883, Method 5005 — Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Electrical Characteristics

DC Parameters⁽¹⁾

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{rline}	Line Regulation	$12V \leq V_{IN} \leq 15V$, $V_{OUT} = 5V$, $I_L = 1mA$		-0.1	0.1	% V_{OUT}	1
				-0.2	0.2	% V_{OUT}	2
				-0.3	0.3	% V_{OUT}	3
		$12V \leq V_{IN} \leq 40V$, $V_{OUT} = 2V$, $I_L = 1mA$		-0.2	0.2	% V_{OUT}	1
		$9.5V \leq V_{IN} \leq 40V$, $V_{OUT} = 5V$, $I_L = 1mA$		-0.3	0.3	% V_{OUT}	1
V_{rload}	Load Regulation	$1mA \leq I_L \leq 50mA$, $V_{IN} = 12V$, $V_{OUT} = 5V$		-0.1 5	0.15	% V_{OUT}	1
				-0.4	0.4	% V_{OUT}	2
				-0.6	0.6	% V_{OUT}	3
		$1mA \leq I_L \leq 10mA$, $V_{IN} = 40V$, $V_{OUT} = 37V$		-0.5	0.5	% V_{OUT}	1
V_{REF}	Voltage Reference	$I_{REF} = 1mA$, $V_{IN} = 12V$		6.95	7.35	V	1
				6.9	7.4	V	2, 3
I_{SCD}	Standby Current	$V_{IN} = 30V$, $I_L = I_{REF} = 0$, $V_{OUT} = V_{REF}$		0.5	3	mA	1
				0.5	2.4	mA	2
				0.5	3.5	mA	3
I_{OS}	Short Circuit Current	$V_{OUT} = 5V$, $V_{IN} = 12V$, $R_{SC} = 10\Omega$, $R_L = 0$		45	85	mA	1
V_Z	Zener Voltage	$V_{IN} = 40V$, $V_{OUT} = 7.15V$, $I_Z = 1mA$	See ⁽²⁾ (3)	5.58	6.82	V	1
V_{OUT}	Output Voltage	$V_{IN} = 12V$, $V_{OUT} = 5V$, $I_L = 1mA$		4.5	5.5	V	1, 2, 3

- (1) Unless otherwise specified, $T_A = 25^\circ C$, $V_{IN} = V^+ = V_C = 12V$, $V^- = 0$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10k\Omega$ connected as shown in [Figure 15](#) Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
- (2) For metal can applications where V_Z is required, an external 6.2V zener diode should be connected in series with V_{OUT} .
- (3) Tested for DIPS only.

Electrical Characteristics

AC Parameters⁽¹⁾

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
Delta V_{OUT} Delta V_{IN}	Ripple Rejection	$f = 120Hz$, $C_{REF} = 0$, $V_{INS} = 2V_{RMS}$		55		dB	4
		$f = 120Hz$, $C_{REF} = 5\mu F$, $V_{INS} = 2V_{RMS}$		67		dB	4

- (1) Unless otherwise specified, $T_A = 25^\circ C$, $V_{IN} = V^+ = V_C = 12V$, $V^- = 0$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10k\Omega$ connected as shown in [Figure 15](#) Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Typical Performance Characteristics

Load Regulation Characteristics with Current Limiting

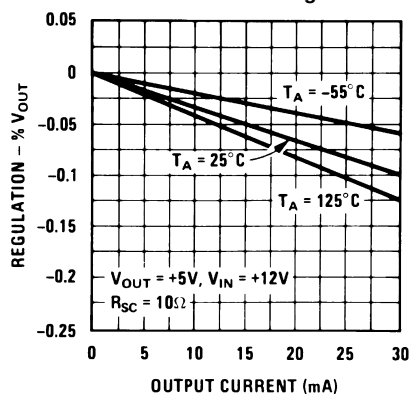


Figure 4.

Load Regulation Characteristics with Current Limiting

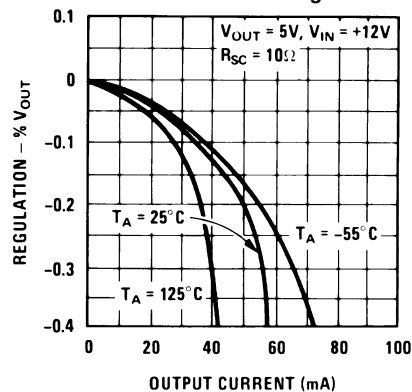


Figure 5.

Load & Line Regulation vs Input-Output Voltage Differential

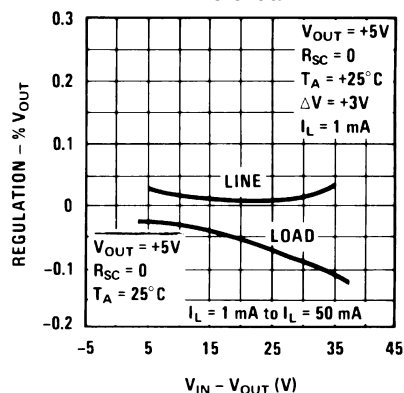


Figure 6.

Current Limiting Characteristics

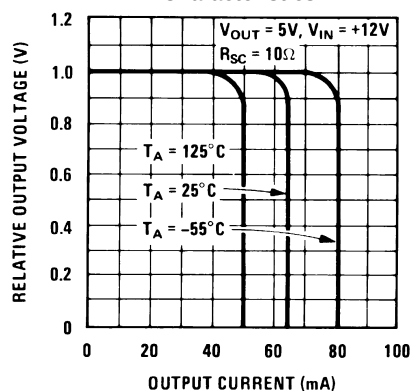


Figure 7.

Current Limiting Characteristics vs Junction Temperature

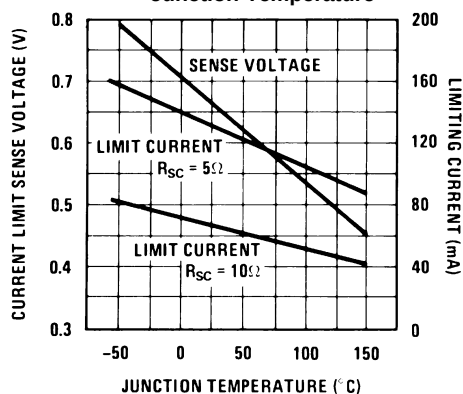


Figure 8.

Standby Current Drain vs Input Voltage

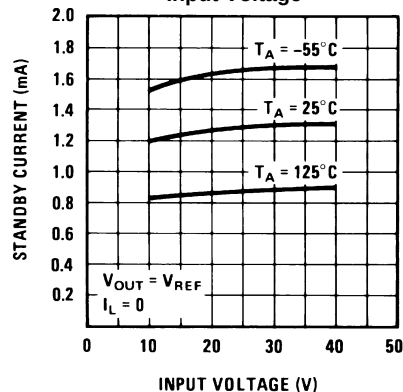


Figure 9.

Typical Performance Characteristics (continued)

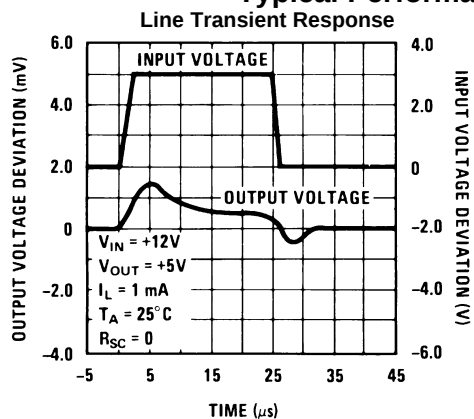


Figure 10.

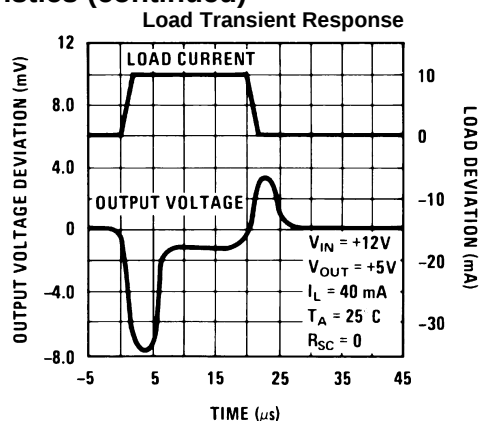


Figure 11.

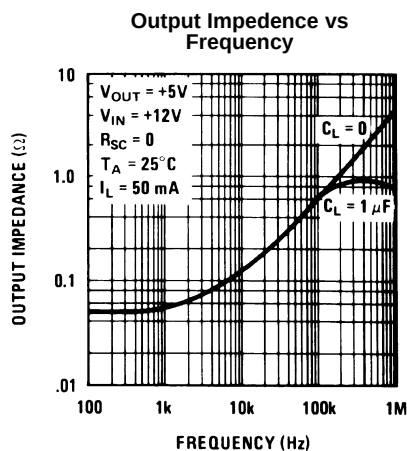
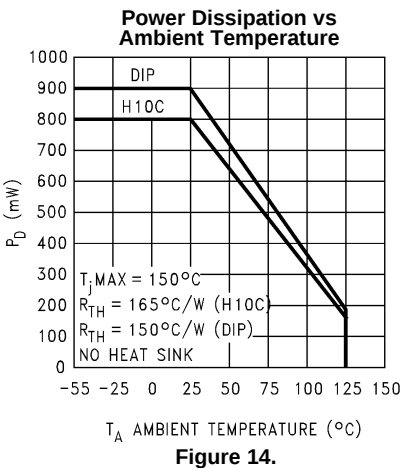
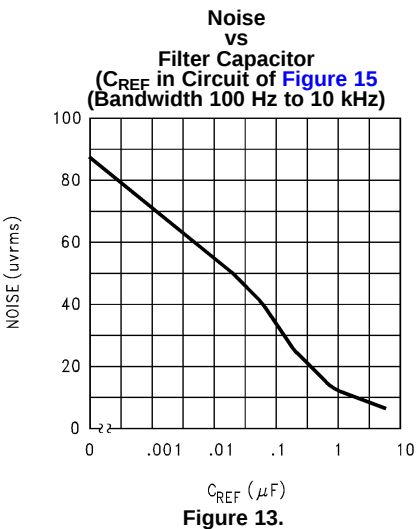


Figure 12.

Maximum Power Ratings



RESISTOR VALUES (KΩ) FOR STANDARD OUTPUT VOLTAGE

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% ⁽¹⁾			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	See ⁽²⁾	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	−6 ⁽³⁾	3, (10)	3.57	2.43	1.2	0.5	0.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 9, 12)	1.87	7.15	0.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

(1) Replace R1/R2 in figures with divider shown in [Figure 27](#).

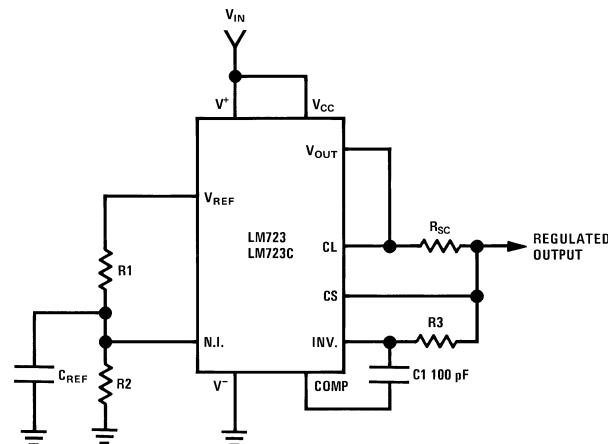
(2) Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

(3) V⁺ and V_{CC} must be connected to a +3V or greater supply.

Table 1. Formulae for Intermediate Output Voltages

Outputs from +2 to +7 volts (Figure 15 , Figure 18 , Figure 19 , Figure 20 , Figure 23 , Figure 26)	Outputs from +4 to +250 volts (Figure 21)	Current Limiting
$V_{OUT} = \left(V_{REF} \times \frac{R2}{R1 + R2} \right) \quad (1)$	$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1} \right); R3 = R4 \quad (2)$	$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}} \quad (3)$
Outputs from +7 to +37 volts (Figure 16 , Figure 18 , Figure 19 , Figure 20 , Figure 23 , Figure 26)	Outputs from −6 to −250 volts (Figure 17 , Figure 22 , Figure 24)	Foldback Current Limiting
$V_{OUT} = \left(V_{REF} \times \frac{R1 + R2}{R2} \right) \quad (5)$	$V_{OUT} = \left(\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1} \right); R3 = R4 \quad (6)$	$I_{KNEE} = \left(\frac{V_{OUT} R3}{R_{SC} R4} + \frac{V_{SENSE} (R3 + R4)}{R_{SC} R4} \right)$ $I_{SHORT\ CKT} = \left(\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4} \right) \quad (4)$

Typical Applications

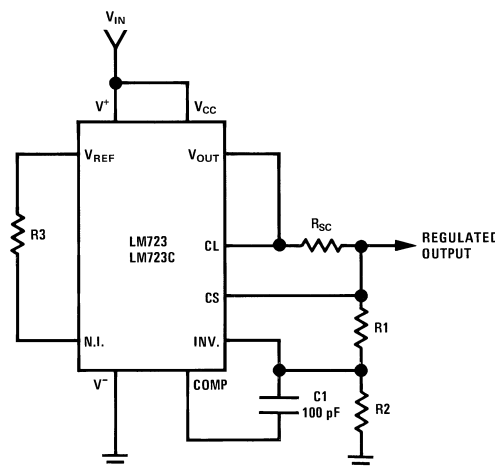


Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 15. Basic Low Voltage Regulator ($V_{OUT} = 2$ to 7 Volts)

Table 2. Basic Low Voltage Regulator ($V_{OUT} = 2$ to 7 Volts)

Typical Performance	
Regulated Output Voltage	5V
Line Regulation ($\Delta V_{IN} = 3V$)	0.5mV
Load Regulation ($\Delta I_L = 50$ mA)	1.5mV



Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Figure 16. Basic High Voltage Regulator $V_{OUT} = 7$ to 37 Volts)

Table 3. Basic High Voltage Regulator $V_{OUT} = 7$ to 37 Volts)

Typical Performance	
Regulated Output Voltage	15V
Line Regulation ($\Delta V_{IN} = 3V$)	1.5 mV
Load Regulation ($\Delta I_L = 50$ mA)	4.5 mV

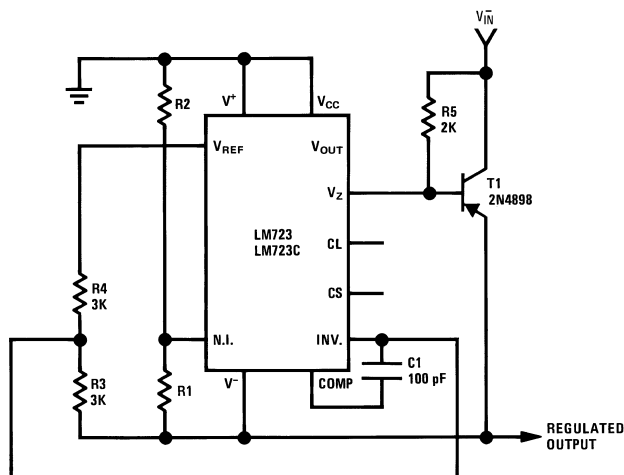


Figure 17. Negative Voltage Regulator

Table 4. Negative Voltage Regulator

Typical Performance	
Regulated Output Voltage	-15V
Line Regulation ($\Delta V_{IN} = 3V$)	1 mV
Load Regulation ($\Delta I_L = 100 \text{ mA}$)	2 mV

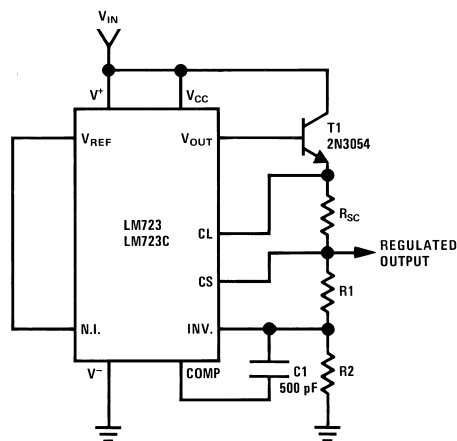


Figure 18. Positive Voltage Regulator - (External NPN Pass Transistor)

Table 5. Positive Voltage Regulator - (External NPN Pass Transistor)

Typical Performance	
Regulated Output Voltage	+15V
Line Regulation ($\Delta V_{IN} = 3V$)	1.5 mV
Load Regulation ($\Delta I_L = 1A$)	15 mV

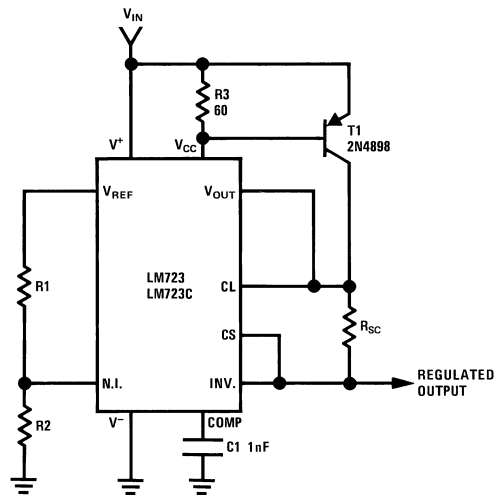


Figure 19. Positive Voltage Regulator – (External PNP Pass Transistor)

Table 6. Positive Voltage Regulator – (External PNP Pass Transistor)

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 3V$)	0.5 mV
Load Regulation ($\Delta I_L = 1A$)	5 mV

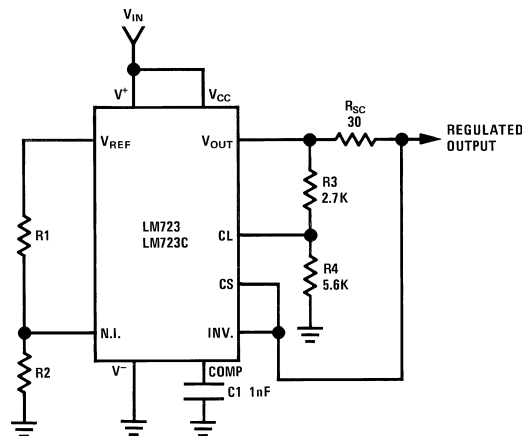


Figure 20. Foldback Current Limiting

Table 7. Foldback Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 3V$)	0.5 mV
Load Regulation ($\Delta I_L = 10 \text{ mA}$)	1 mV
Short Circuit Current	20 mA

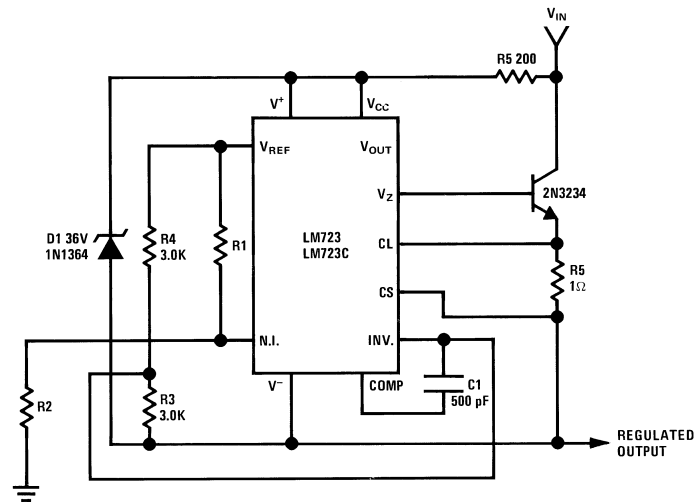


Figure 21. Positive Floating Regulator

Table 8. Positive Floating Regulator

Typical Performance	
Regulated Output Voltage	+50V
Line Regulation ($\Delta V_{IN} = 20V$)	15 mV
Load Regulation ($\Delta I_L = 50 \text{ mA}$)	20 mV

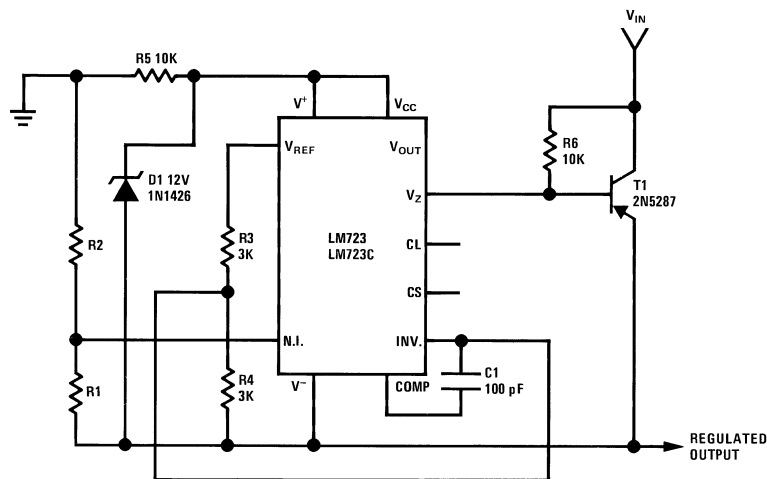


Figure 22. Negative Floating Regulator

Table 9. Negative Floating Regulator

Typical Performance	
Regulated Output Voltage	-100V
Line Regulation ($\Delta V_{IN} = 20V$)	30 mV
Load Regulation ($\Delta I_L = 100 \text{ mA}$)	20 mV

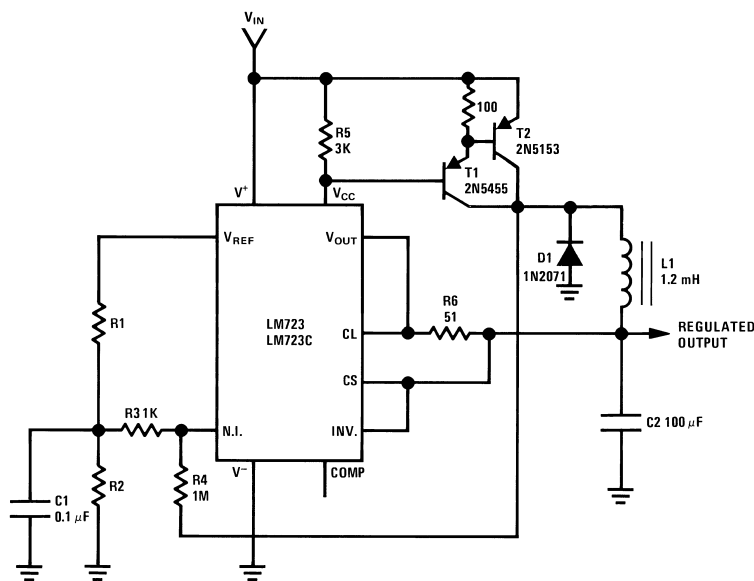


Figure 23. Positive Switching Regulator

Table 10. Positive Switching Regulator⁽¹⁾

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 30V$)	10 mV
Load Regulation ($\Delta I_L = 2A$)	80 mV

(1) L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap

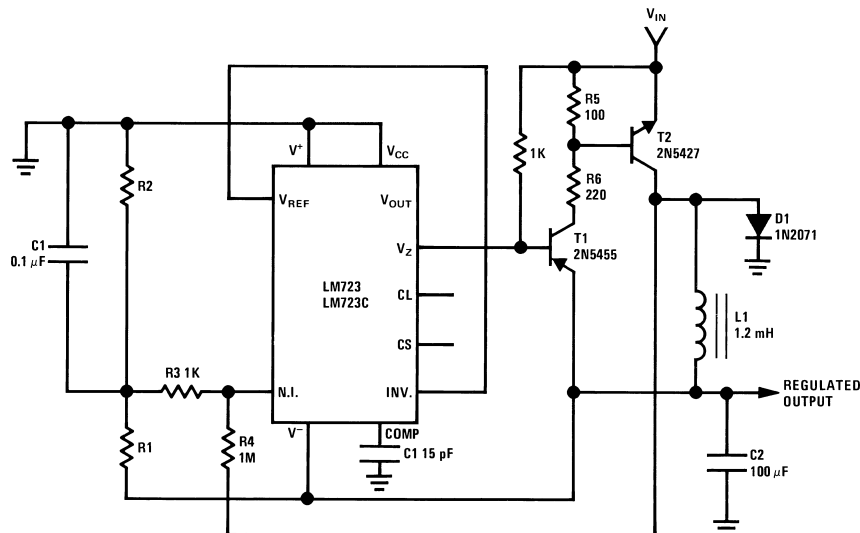
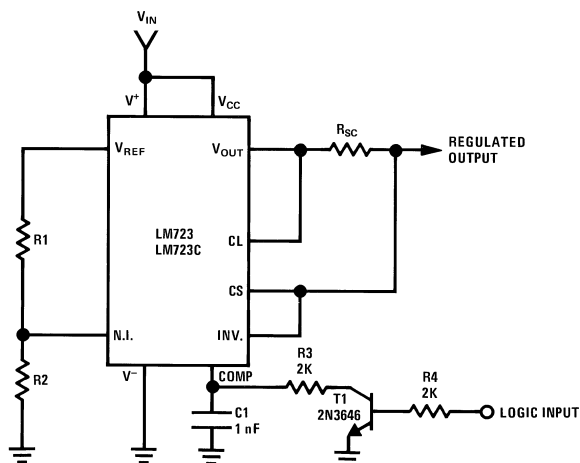


Figure 24. Negative Switching Regulator

Table 11. Negative Switching Regulator⁽¹⁾

Typical Performance	
Regulated Output Voltage	-15V
Line Regulation ($\Delta V_{IN} = 20V$)	8 mV
Load Regulation ($\Delta I_L = 2A$)	6 mV

(1) L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap



Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 25. Remote Shutdown Regulator with Current Limiting

Table 12. Remote Shutdown Regulator with Current Limiting

Typical Performance	
Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 3V$)	0.5 mV
Load Regulation ($\Delta I_L = 50 \text{ mA}$)	1.5 mV

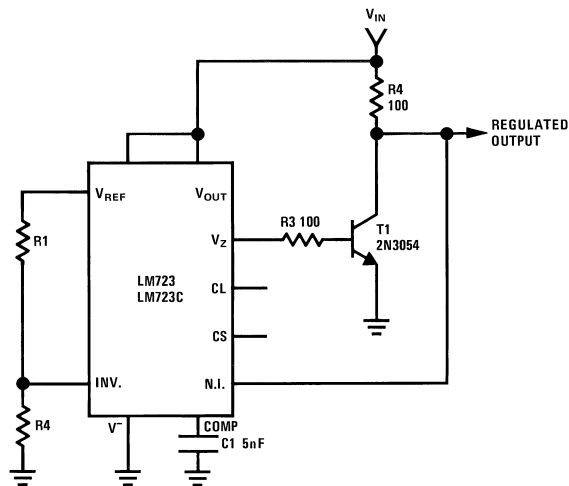
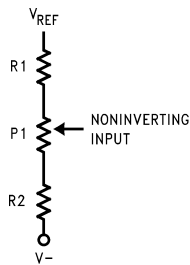


Figure 26. Shunt Regulator

Table 13. Shunt Regulator

Regulated Output Voltage	+5V
Line Regulation ($\Delta V_{IN} = 10V$)	0.5 mV
Load Regulation ($\Delta I_L = 100 \text{ mA}$)	1.5 mV



(1) Replace R1/R2 in figures with divider shown in [Figure 27](#)

Figure 27. Output Voltage Adjust

Revision History Section

Date Released	Revision	Section	Originator	Changes
02/15/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNLM723-X, Rev. 1A0. MDS data sheet will be archived. AC and Drift parameters removed from specification because they only applied to the JAN B/S devices, covered in a separate datasheet.

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM723 MD8	ACTIVE	DIE SALE	Y	0	400	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM723E/883	ACTIVE	LCCC	NAJ	20	50	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 125	LM723E /883 Q ACO /883 Q >T	Samples
LM723H/883	ACTIVE	TO-100	LME	10	20	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 125	LM723H/883 Q ACO LM723H/883 Q >T	Samples
LM723J/883	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LM723J/883 Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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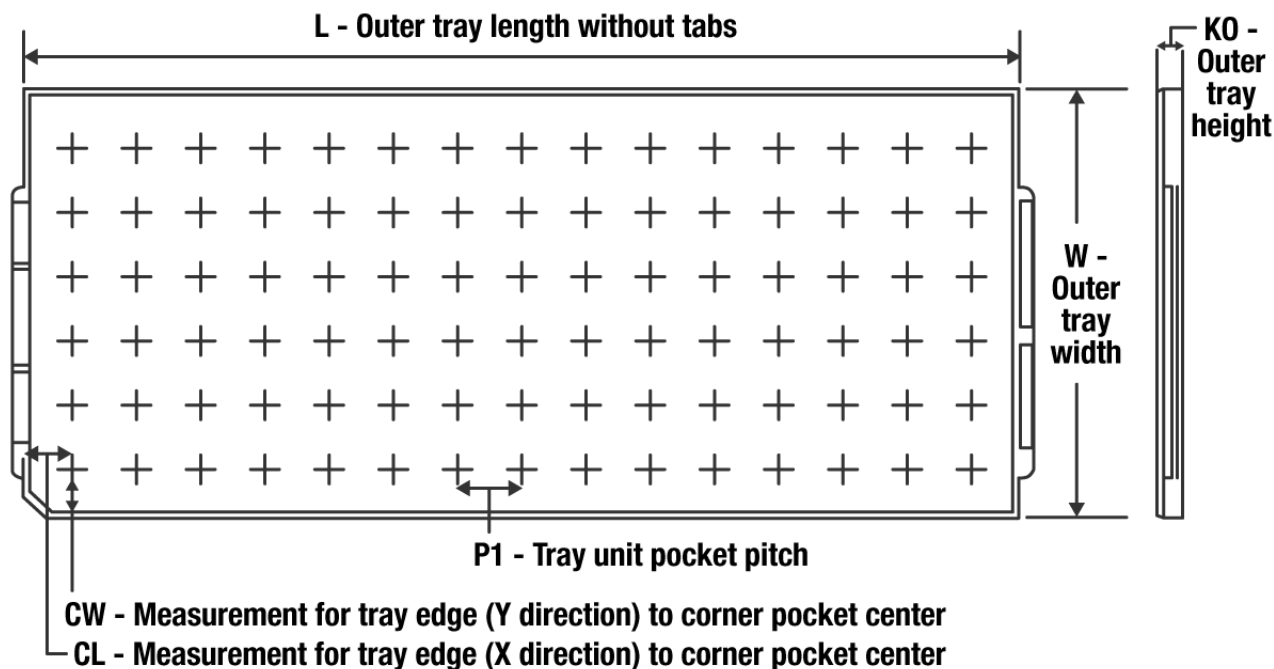
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM723E/883	NAJ	LCCC	20	50	470	11	3810	0
LM723J/883	J	CDIP	14	25	502	14	10668	4.32

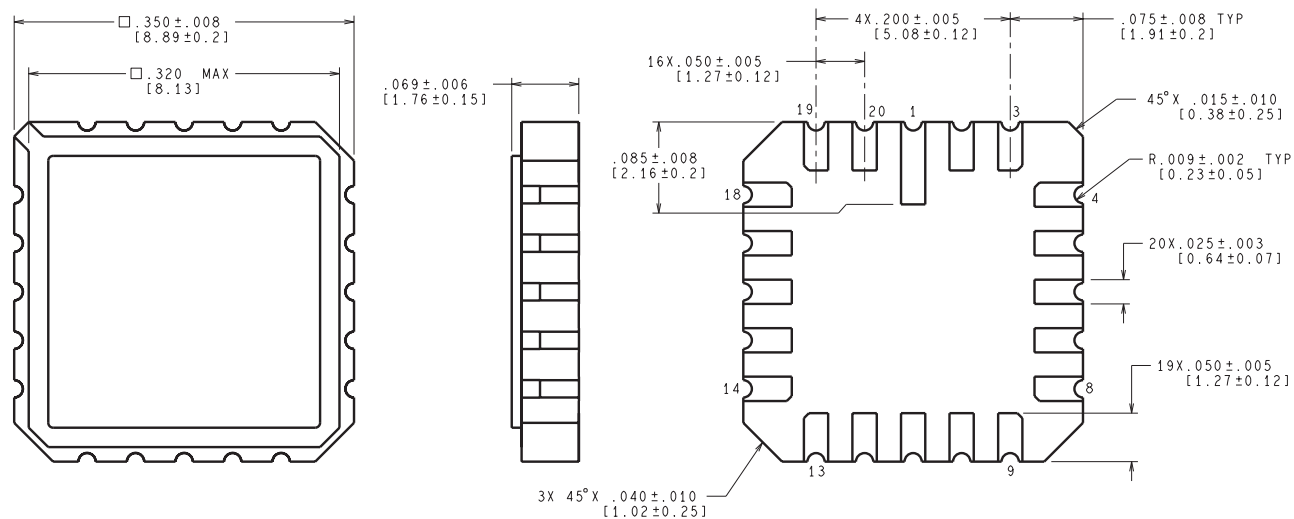
TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
LM723H/883	LME	TO-CAN	10	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

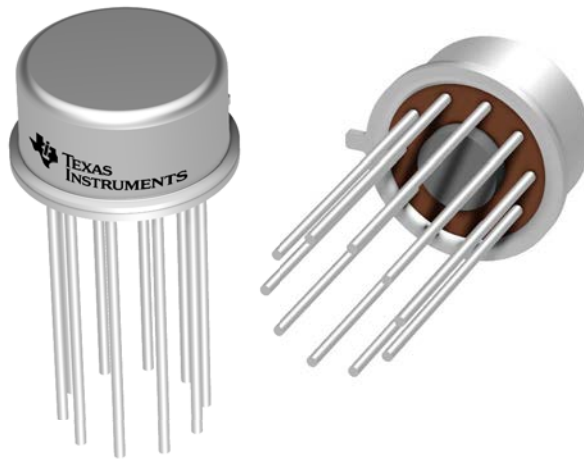
E20A (Rev F)

GENERIC PACKAGE VIEW

LME 10

TO-CAN - 5.72 mm max height

METAL CYLINDRICAL PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4202488/B

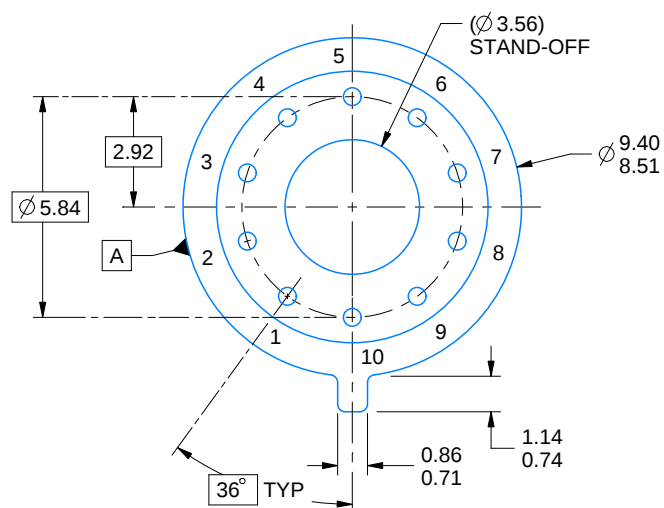
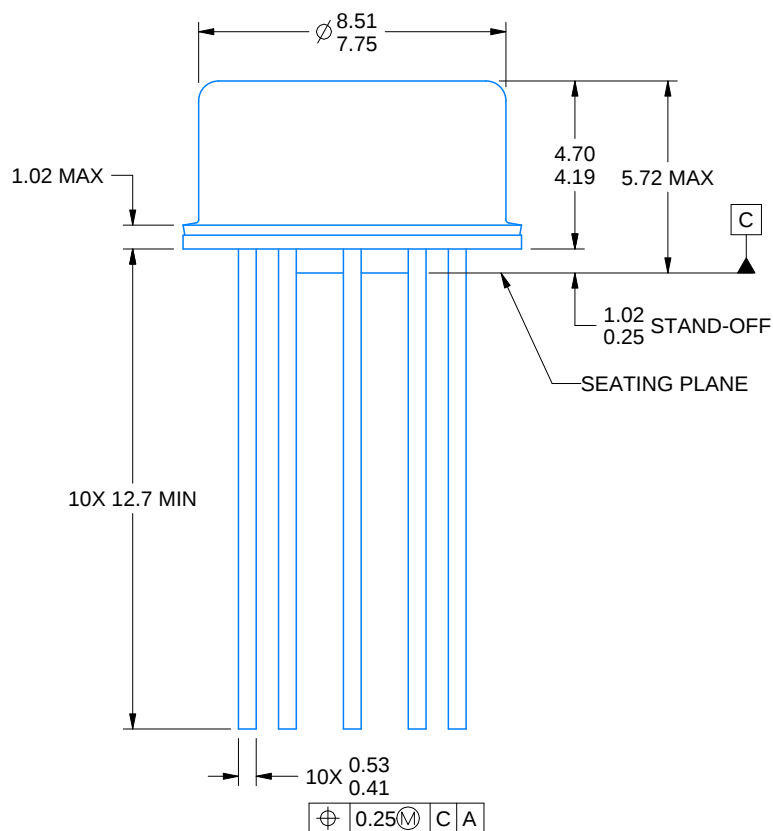


LME0010A

PACKAGE OUTLINE

TO-CAN - 5.72 mm max height

METAL CYLINDRICAL PACKAGE



4220604/A 05/2017

NOTES:

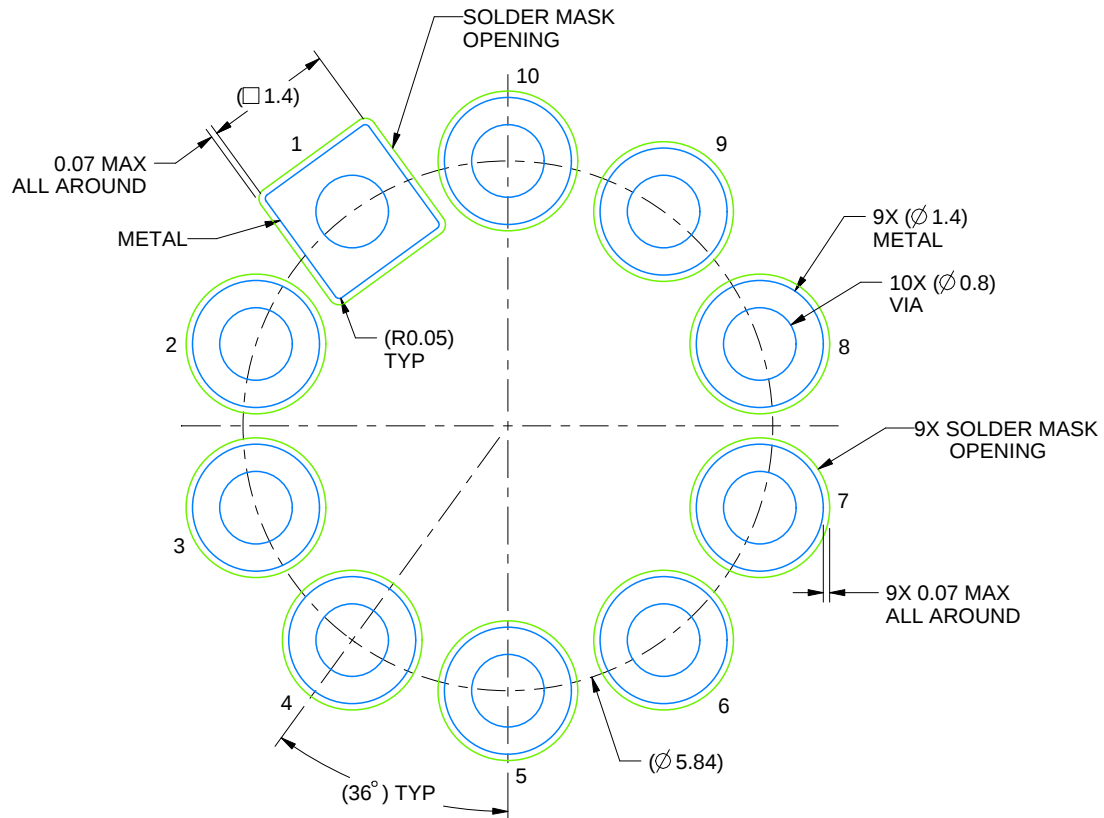
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-006/TO-100.

EXAMPLE BOARD LAYOUT

LME0010A

TO-CAN - 5.72 mm max height

METAL CYLINDRICAL PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220604/A 05/2017

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

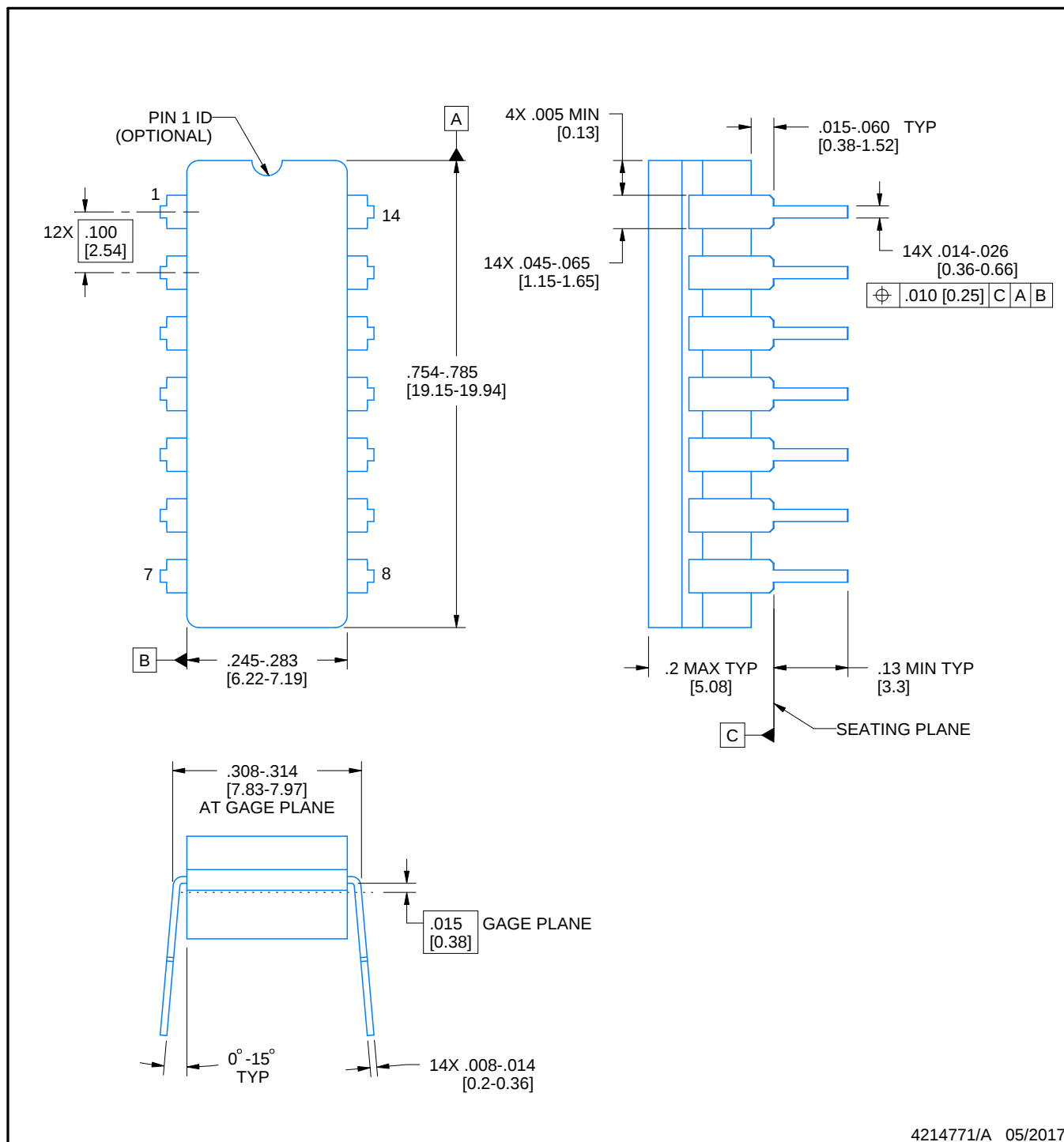


J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

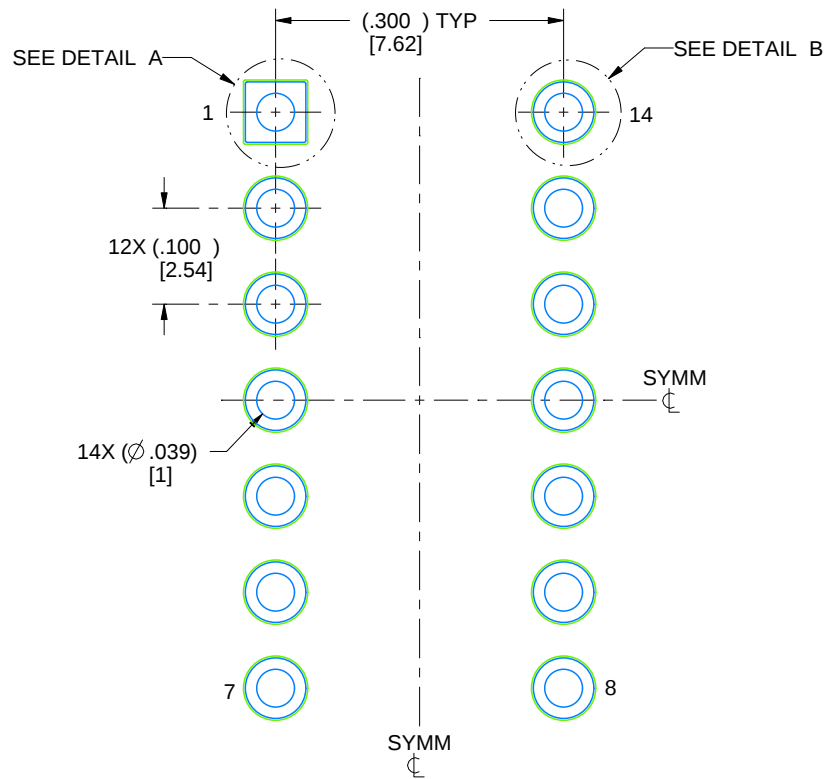
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

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