

行业标准双路运算放大器

1 特性

- 3V 至 36V 的宽电源电压范围 (B、BA 版本)
- 静态电流 : 300 μ A/通道 (B、BA 版本)
- 单位增益带宽为 1.2 MHz (B、BA 版本)
- 共模输入电压范围包括接地, 支持近地直接感测
- 25°C 时的最大输入失调电压为 2 mV (BA 版本)
- 25°C 时的最大输入失调电压为 3 mV (A、B 版本)
- 内部射频和 EMI 滤波器 (B、BA 版本)
- 对于符合 MIL-PRF-38535 标准的产品, 所有参数均经过测试, 除非另有说明。对于所有其他产品, 生产流程不一定包含对所有参数的测试。

2 应用

- 商用网络和服务器电源单元
- 多功能打印机
- 电源和移动充电器
- 电机控制 : 交流感应、有刷直流、无刷直流、高压、低压、永磁和步进电机
- 台式计算机和主板
- 室内外空调
- 洗衣机、烘干机和冰箱
- 交流逆变器、串式逆变器、中央逆变器和变频器
- 不间断电源
- 电子销售点系统

3 说明

LM358B 和 LM2904B 器件是行业标准运算放大器 LM358 和 LM2904 的下一代版本, 其中包括两个高压 (36V) 运算放大器。这些器件为成本敏感型应用提供了卓越的价值, 其特性包括低偏移 (300 μ V, 典型值)、对地共模输入范围和高差分输入电压能力。

LM358B 和 LM2904B 运算放大器利用单位增益稳定性、更低的失调电压 (最大值为 3mV ; LM358BA 和

LM2904BA 的最大值为 2mV) 和更低的静态电流 (每个放大器为 300 μ A, 典型值) 等增强型特性简化了电路设计。高 ESD (2kV, HBM) 和集成 EMI 以及射频滤波器可支持将 LM358B 和 LM2904B 器件用于更严苛、更具环境挑战性的应用。

LM358B 和 LM2904B 放大器采用微型封装 (如 SOT23-8) , 以及行业标准封装 (包括 SOIC、TSSOP 和 VSSOP) 。

器件信息

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
LM358B、LM358BA、LM2904B、LM2904BA、LM358、LM358A、LM2904、LM2904V、LM258、LM258A	SOIC (8)	4.90mm × 3.90mm
LM358B、LM358BA、LM2904B、LM2904BA、LM358、LM358A、LM2904、LM2904V	TSSOP (8)	3.00mm × 4.40mm
LM358B、LM358BA、LM2904B、LM2904BA、LM358、LM358A、LM2904、LM2904V、LM258、LM258A	VSSOP (8)	3.00mm × 3.00mm
LM358B、LM358BA、LM2904B、LM2904BA	SOT-23 (8)	2.90mm × 1.60mm
LM358、LM2904	SO (8)	5.20mm × 5.30mm
LM358、LM2904、LM358A、LM258、LM258A	PDIP (8)	9.81mm × 6.35mm
LM158、LM158A	CDIP (8)	9.60mm × 6.67mm
LM158、LM158A	LCCC (20)	8.89mm × 8.89mm

系列产品比较

技术规范	LM358B LM358BA	LM2904B LM2904BA	LM358 LM358A	LM2904	LM2904V LM2904AV	LM258 LM258A	LM158 LM158A	单位
电源电压	3 至 36	3 至 36	3 至 30	3 至 26	3 至 30	3 至 30	3 至 30	V
失调电压 (25°C 时的最大值)	± 3 ± 2	± 3 ± 2	± 7 ± 3	± 7	± 7 ± 2	± 5 ± 3	± 5 ± 2	mV
输入偏置电流 (典型值/最大值)	10/35	10/35	20/250 15/100	20/250	20/250	20/150 15/80	20/150 15/50	nA
增益带宽积	1.2	1.2	0.7	0.7	0.7	0.7	0.7	MHz
电源电流 (每通道的典型值)	0.3	0.3	0.35	0.35	0.35	0.35	0.35	mA
ESD (HBM)	2000	2000	500	500	500	500	500	V
工作环境温度	-40 至 85	-40 至 125	0 至 70	-40 至 125	-40 至 125	-25 至 85	-55 至 125	°C

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision Z (July 2021) to Revision AA (March 2022)	Page
• 在 <i>器件信息</i> 表中添加了 LM358BA 和 LM2904BA.....	1
• 向 <i>说明</i> 部分添加了 <i>系列比较表</i>	1
• Raised ESD (CDM) for B-versions and BA-versions from 1 kV to 1.5 kV in the <i>ESD Ratings</i> table	6
• Changed Input Offset Voltage Max of LM2904BA from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ from $\pm 2.5\text{ mV}$ to $\pm 3.0\text{ mV}$	11

Changes from Revision Y (February 2021) to Revision Z (July 2021)	Page
• 删除了 <i>器件信息</i> 表中 LM358B 和 LM2904B SOT-23 (8) 封装的预发布标签.....	1
• Updated DDF (SOT-23) package thermal information in the <i>Thermal Information</i> table.....	7
• Deleted <i>Related Links</i> from the <i>Device and Documentation Support</i> section.....	34

Changes from Revision X (June 2020) to Revision Y (February 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 在整个数据表中添加了 SOT23-8 (DDF) 封装信息.....	1
• 删除了 <i>器件信息</i> 表中 LM358B 和 LM2904B VSSOP (8) 封装的预发布标签.....	1
• Added SOT23-8 (DDF) package information to the <i>Pin Configuration and Functions</i> section.....	5
• Added DDF (SOT-23) package to the <i>Thermal Information</i> table.....	7

Changes from Revision W (October 2019) to Revision X (June 2020)	Page
• 向 <i>应用</i> 部分添加了应用链接.....	1
• 删除了 <i>器件信息</i> 表中 LM358B 和 LM2904B TSSOP (8) 封装的预发布标签.....	1

Changes from Revision V (September 2018) to Revision W (October 2019)	Page
• Changed CDM ESD rating for LM358B and LM2904B in <i>ESD Ratings</i>	6
• Changed V_S to V_+ in <i>Recommended Operating Conditions</i>	7
• Changed <i>Thermal Information</i> for the LM158FK and LM158JG devices.....	7
• Added <i>Typical Characteristics</i> section for the LM358B and LM2490B op amps.....	19
• Added test circuit for THD+N and small-signal step response, $G = -1$ in the <i>Parameter Measurement Information</i> section.....	28
• Changed the Functional Block Diagram	29

Changes from Revision U (January 2017) to Revision V (September 2018)	Page
• 更改了数据表标题.....	1
• 更改了 <i>特性</i> 部分中的前四项.....	1
• 更改了 <i>应用</i> 部分中的第一项并添加了四个新项.....	1
• 更改了 <i>说明</i> 部分第一段中的电压值.....	1
• 更改了 <i>说明</i> 部分第二段中的文本内容.....	1
• 在数据表中添加了器件 LM358B 和 LM2904B.....	1
• 更改了 <i>器件信息</i> 表的前三行，并为状态为预发布的器件添加了交叉参考注释.....	1
• Added a table note to the <i>Pin Functions</i> table	5
• Changed "free-air temperature" to "ambient temperature" in the <i>Absolute Maximum Ratings</i> condition statement.....	6
• Changed all entries in the <i>Absolute Maximum Ratings</i> table except T_J and T_{stg}	6
• Deleted lead temperature and case temperature from <i>Absolute Maximum Ratings</i>	6
• Changed device listings and their voltage values in the <i>ESD Ratings</i> table	6
• Changed "free-air temperature" to "ambient temperature" in the <i>Recommended Operating Conditions</i> condition statement	7
• Changed table entries for all parameters in the <i>Recommended Operating Conditions</i> table.....	7
• Added rows to the Thermal Information table, and a table note regarding device-package combinations	7
• Deleted the <i>Operating Conditions</i> table.....	18
• Added a condition statement to the <i>Typical Characteristics</i> section.....	26
• Changed specific voltages to a <i>Recommended Operating Conditions</i> reference.....	29
• Changed unity-gain bandwidth from 0.7 MHz for all devices to 1.2 MHz for B-version devices.....	30
• Changed slew rate from 3 V/ μ s for all devices to 0.5 V/ μ s for B-version devices.....	30
• Changed the 节 8.3.3 section in multiple places throughout.....	30
• Changed V_{CC} to V_S in the 节 9.1 section	31
• Subscripted the suffixes from R_I and R_F	31
• Changed <i>Operational Amplifier Board Layout for Noninverting Configuration</i> with an image that includes a dual op amp.....	33

Changes from Revision T (April 2015) to Revision U (January 2017)	Page
• 更改了数据表标题.....	1

Changes from Revision S (January 2014) to Revision T (April 2015)	Page
• 添加了 <i>应用</i> 部分、 <i>ESD</i> 等级表、 <i>特性说明</i> 部分、 <i>器件功能模式</i> 、 <i>应用和实施</i> 部分、 <i>电源相关建议</i> 部分、 <i>布局</i> 部分、 <i>器件和文档支持</i> 部分以及 <i>机械、封装和可订购信息</i> 部分.....	1

Changes from Revision R (July 2010) to Revision S (January 2014)	Page
• 使用网上的 PDF 将此数据表从 QS 格式转换为 DocZone.....	1
• 删除了 <i>订购信息</i> 表.....	1
• 更新了 <i>特性</i> 部分以包含“军用免责声明”	1

- Added Typical Characteristics section..... 26

5 Pin Configuration and Functions

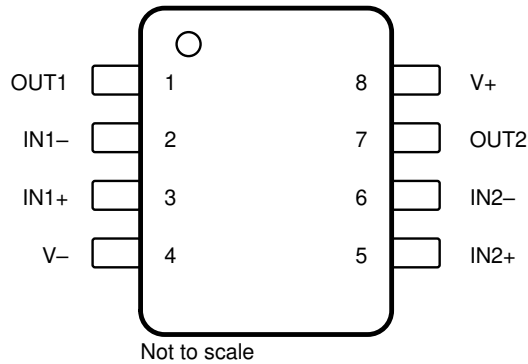
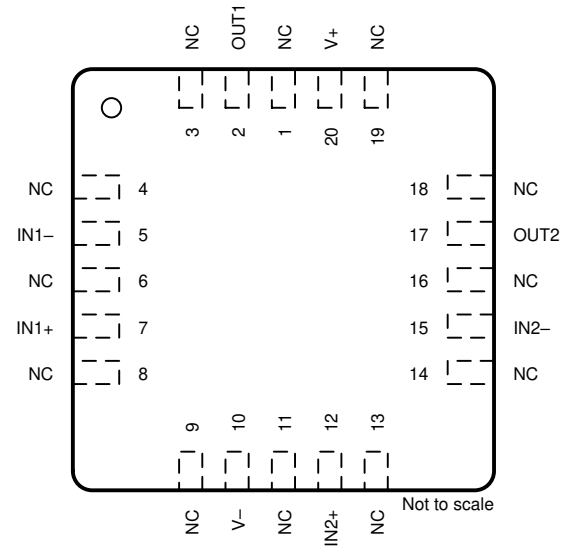


图 5-1. D, DDF, DGK, P, PS, PW, and JG Package
8-Pin SOIC, SOT23-8, VSSOP, PDIP, SO, TSSOP,
and CDIP
Top View



NC - No internal connection

图 5-2. FK Package
20-Pin LCCC
Top View

表 5-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION
	LCCC ⁽¹⁾	SOIC, SOT23-8, VSSOP, CDIP, PDIP, SO, TSSOP, CFP ⁽¹⁾		
IN1 -	5	2	I	Negative input
IN1+	7	3	I	Positive input
IN2 -	15	6	I	Negative input
IN2+	12	5	I	Positive input
OUT1	2	1	O	Output
OUT2	17	7	O	Output
V -	10	4	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	—	No internal connection
V+	20	8	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see 节 3.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
Supply voltage, $V_S = ([V+] - [V-])$	LM358B, LM358BA, LM2904B, LM2904BA		±20 or 40	V	
	LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V		±16 or 32		
	LM2904		±13 or 26		
Differential input voltage, V_{ID} ⁽²⁾	LM358B, LM358BA, LM2904B, LM2904BA, LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	- 32	32	V	
	LM2904	- 26	26		
Input voltage, V_I	Either input	LM358B, LM358BA, LM2904B, LM2904BA	- 0.3	40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	- 0.3	32	
		LM2904	- 0.3	26	
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$, $V_S \leq 15\text{ V}$ ⁽³⁾			Unlimited	s	
Operating ambient temperature, T_A	LM158, LM158A	- 55	125	°C	
	LM258, LM258A	- 25	85		
	LM358B, LM358BA	- 40	85		
	LM358, LM358A	0	70		
	LM2904B, LM2904BA, LM2904, LM2904V	- 40	125		
Operating virtual-junction temperature, T_J			150	°C	
Storage temperature, T_{stg}		- 65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages are at $IN+$, with respect to $IN-$.
- (3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction.

6.2 ESD Ratings

		VALUE	UNIT
LM358B, LM358BA, LM2904B, AND LM2904BA			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	
LM158, LM258, LM358, LM158, LM258A, LM358A, LM2904, AND LM2904V			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _S	Supply voltage, V _S = ([V+] - [V-])	LM358B, LM358BA, LM2904B, LM2904BA	3	36	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	3	30	
		LM2904	3	26	
V _{CM}	Common-mode voltage	V-	V+ - 2	V	
T _A	Operating ambient temperature	LM358B, LM358BA	- 40	85	°C
		LM2904B, LM2904BA, LM2904, LM2904V	- 40	125	
		LM358, LM358A	0	70	
		LM258, LM258A	- 20	85	
		LM158, LM158A	- 55	125	

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM258, LM258A, LM358, LM358A, LM358B, LM358BA, LM2904, LM2904B, LM2904BA, LM2904V ⁽²⁾						LM158, LM158A		UNIT	
	D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)		
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8PINS	20 PINS	8 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	124.7	181.4	80.9	116.9	171.7	164.3	84.0	112.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	66.9	69.4	70.4	62.5	68.8	98.1	56.9	63.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	67.9	102.9	57.4	68.6	99.2	82.1	57.5	100.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	19.2	11.8	40	21.9	11.5	11.4	51.7	35.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	67.2	101.2	56.9	67.6	97.9	81.7	57.1	93.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	—	10.6	22.3	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
(2) For a listing of which devices are available in what packages, see [# 3](#).

6.5 Electrical Characteristics: LM358B and LM358BA

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$
 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	LM358B			± 0.3	± 3.0	mV	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			± 4		mV
		LM358BA				± 2.0		mV
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				± 2.5	
dV_{OS}/dT	Input offset voltage drift		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(1)}$	± 3.5	11		$\mu\text{V}/^\circ\text{C}$	
PSRR	Power supply rejection ratio			± 2	15		$\mu\text{V}/\text{V}$	
	Channel separation, dc	$f = 1\text{ kHz}$ to 20 kHz		± 1			$\mu\text{V}/\text{V}$	
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	$V_S = 3\text{ V}$ to 36 V			$(V-)$	$(V+) - 1.5$	V	
		$V_S = 5\text{ V}$ to 36 V		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$(V-)$	$(V+) - 2$		V
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5\text{ V}$	$V_S = 3\text{ V}$ to 36 V		20	100	$\mu\text{V}/\text{V}$	
		$(V-) \leq V_{CM} \leq (V+) - 2.0\text{ V}$	$V_S = 5\text{ V}$ to 36 V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	25	316		
INPUT BIAS CURRENT								
I_B	Input bias current				± 10	± 35	nA	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(1)}$			± 50		
I_{OS}	Input offset current				0.5	4	nA	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(1)}$			5		
dI_{OS}/dT	Input offset current drift		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	10			$\text{pA}/^\circ\text{C}$	
NOISE								
E_n	Input voltage noise	$f = 0.1$ to 10 Hz			3		μV_{PP}	
e_n	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
INPUT IMPEDANCE								
Z_{ID}	Differential				$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$	
Z_{IC}	Common-mode				$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$	
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = 1\text{ V}$ to 11 V ; $R_L \geq 10\text{ k}\Omega$, connected to $(V-)$			70	140	V/mV	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		35			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				1.2		MHz	
SR	Slew rate	$G = +1$			0.5		V/ μs	
ϕ_m	Phase margin	$G = +1$, $R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$			56		$^\circ$	
t_{OR}	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		μs	
t_s	Settling time	To 0.1%, $V_S = 5\text{ V}$, 2-V step, $G = +1$, $C_L = 100\text{ pF}$			4		μs	
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3.53\text{ V}_{RMS}$, $V_S = 36\text{ V}$, $R_L = 100\text{ k}\Omega$, $I_{OUT} \leq \pm 50\text{ }\mu\text{A}$, BW = 80 kHz			0.001		%	
OUTPUT								
V_O	Voltage output swing from rail	Positive rail ($V+$)		$I_{OUT} = 50\text{ }\mu\text{A}$	1.35	1.42	V	
				$I_{OUT} = 1\text{ mA}$	1.4	1.48	V	
				$I_{OUT} = 5\text{ mA}^{(1)}$	1.5	1.61	V	
		Negative rail ($V-$)		$I_{OUT} = 50\text{ }\mu\text{A}$	100	150	mV	
				$I_{OUT} = 1\text{ mA}$	0.75	1	V	
			$V_S = 5\text{ V}$, $R_L \leq 10\text{ k}\Omega$ connected to $(V-)$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	5	20	mV	
I_O	Output current	$V_S = 15\text{ V}$; $V_O = V-$; $V_{ID} = 1\text{ V}$	Source ⁽¹⁾		-20	-30	mA	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-10	20		
		$V_S = 15\text{ V}$; $V_O = V+$; $V_{ID} = -1\text{ V}$	Sink ⁽¹⁾		10	20		
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	5			
I_{SC}	Short-circuit current	$V_{ID} = -1\text{ V}$; $V_O = (V-) + 200\text{ mV}$		60	100		μA	
		$V_S = 20\text{ V}$, $(V+) = 10\text{ V}$, $(V-) = -10\text{ V}$, $V_O = 0\text{ V}$		± 40	± 60		mA	

6.5 Electrical Characteristics: LM358B and LM358BA (continued)

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{k}$ connected to $V_S / 2$
(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{LOAD}	Capacitive load drive			100		pF
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$		300		Ω

6.5 Electrical Characteristics: LM358B and LM358BA (continued)

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, $R_L = 10\text{k}$ connected to $V_S / 2$
 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$V_S = 5\text{ V}; I_O = 0\text{ A}$		300	460	μA
I_Q	Quiescent current per amplifier	$V_S = 36\text{ V}; I_O = 0\text{ A}$			800	μA

(1) Specified by characterization only.

6.6 Electrical Characteristics: LM2904B and LM2904BA

$V_S = (V_+) - (V_-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	LM2904B			± 0.3	± 3.0	mV	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 4		mV
		LM2904BA					± 2.0	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					± 3.0
dV_{OS}/dT	Input offset voltage drift		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}^{(1)}$		± 3.5	12	$\mu\text{V}/^\circ\text{C}$	
PSRR	Power Supply Rejection Ratio				± 2	15	$\mu\text{V}/\text{V}$	
	Channel separation, dc	$f = 1\text{ kHz}$ to 20 kHz			± 1		$\mu\text{V}/\text{V}$	
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	$V_S = 3\text{ V}$ to 36 V			(V_-)	$(V_+) - 1.5$	V	
		$V_S = 5\text{ V}$ to 36 V		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	(V_-)	$(V_+) - 2$	V	
CMRR	Common-mode rejection ratio	$(V_-) \leq V_{CM} \leq (V_+) - 1.5\text{ V}$	$V_S = 3\text{ V}$ to 36 V		20	100	$\mu\text{V}/\text{V}$	
		$(V_-) \leq V_{CM} \leq (V_+) - 2.0\text{ V}$	$V_S = 5\text{ V}$ to 36 V	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	25	316		
INPUT BIAS CURRENT								
I_B	Input bias current				± 10	± 35	nA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}^{(1)}$			± 50		
I_{OS}	Input offset current				0.5	4	nA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}^{(1)}$			5		
dI_{OS}/dT	Input offset current drift		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		10		$\text{pA}/^\circ\text{C}$	
NOISE								
E_n	Input voltage noise	$f = 0.1$ to 10 Hz			3		μV_{PP}	
e_n	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
INPUT IMPEDANCE								
Z_{ID}	Differential				$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$	
Z_{IC}	Common-mode				$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$	
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = 1\text{ V}$ to 11 V ; $R_L \geq 10\text{ k}\Omega$, connected to (V_-)			70	140	V/mV	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		35		V/mV	
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				1.2		MHz	
SR	Slew rate	$G = +1$			0.5		$\text{V}/\mu\text{s}$	
θ_m	Phase margin	$G = +1$, $R_L = 10\text{ k}\Omega$, $C_L = 20\text{ pF}$			56		$^\circ$	
t_{OR}	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		μs	
t_s	Settling time	To 0.1%, $V_S = 5\text{ V}$, 2-V Step, $G = +1$, $C_L = 100\text{ pF}$			4		μs	
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3.53\text{ V}_{RMS}$, $V_S = 36\text{ V}$, $R_L = 100\text{ k}\Omega$, $I_{OUT} \leq \pm 50\mu\text{A}$, $\text{BW} = 80\text{ kHz}$			0.001		%	
OUTPUT								
V_O	Voltage output swing from rail	Positive Rail (V_+)	$I_{OUT} = 50\mu\text{A}$		1.35	1.42	V	
			$I_{OUT} = 1\text{ mA}$		1.4	1.48	V	
			$I_{OUT} = 5\text{ mA}^{(1)}$		1.5	1.61	V	
		Negative Rail (V_-)	$I_{OUT} = 50\mu\text{A}$		100	150	mV	
			$I_{OUT} = 1\text{ mA}$		0.75	1	V	
			$V_S = 5\text{ V}$, $R_L \leq 10\text{ k}\Omega$ connected to (V_-)	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		5	20	mV
I_O	Output current	$V_S = 15\text{ V}$; $V_O = V_-$; $V_{ID} = 1\text{ V}$	Source ⁽¹⁾		-20	-30	mA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-10			
		$V_S = 15\text{ V}$; $V_O = V_+$; $V_{ID} = -1\text{ V}$	Sink ⁽¹⁾		10	20		
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		5			
		$V_{ID} = -1\text{ V}$; $V_O = (V_-) + 200\text{ mV}$			60	100	μA	
I_{SC}	Short-circuit current	$V_S = 20\text{ V}$, $(V_+) = 10\text{ V}$, $(V_-) = -10\text{ V}$, $V_O = 0\text{ V}$			± 40	± 60	mA	
C_{LOAD}	Capacitive load drive				100		pF	

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$, $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, $R_L = 10\text{k}$ connected to $V_S/2$
 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$		300		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	$V_S = 5\text{ V}$; $I_O = 0\text{ A}$		300	460	μA
I_Q	Quiescent current per amplifier	$V_S = 36\text{ V}$; $I_O = 0\text{ A}$			800	μA

(1) Specified by characterization only

6.7 Electrical Characteristics: LM358, LM358A

For $V_S = (V_+) - (V_-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT				
OFFSET VOLTAGE											
V_{OS}	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}; V_{CM} = 0\text{ V}; V_O = 1.4\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	3	7	mV				
					9						
			LM358A	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	2	3					
					5						
dV_{OS}/dT	Input offset voltage drift		LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$				
			LM358A	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	7	20					
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5\text{ V to }30\text{ V}$			65	100	dB				
V_{O1}/V_{O2}	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$				120	dB				
INPUT VOLTAGE RANGE											
V_{CM}	Common-mode voltage range						V				
								$V_S = 5\text{ V to }30\text{ V}$	LM358	(V-)	(V+) - 1.5
								$V_S = 30\text{ V}$	LM358A		
								$V_S = 5\text{ V to }30\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	(V+) - 2
$V_S = 30\text{ V}$	LM358A										
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V to }30\text{ V}; V_{CM} = 0\text{ V}$			65	80	dB				
INPUT BIAS CURRENT											
I_B	Input bias current	$V_O = 1.4\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	-20	-250	nA				
					-500						
			LM358A	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	-15	-100					
					-200						
I_{OS}	Input offset current	$V_O = 1.4\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	2	50	nA				
					150						
			LM358A	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	2	30					
					75						
dI_{OS}/dT	Input offset current drift					10	$\text{pA}/^\circ\text{C}$				
			LM358A	$T_A = 0^\circ\text{C to }70^\circ\text{C}$		300					
NOISE											
e_n	Input voltage noise density	$f = 1\text{ kHz}$				40	$\text{nV}/\sqrt{\text{Hz}}$				
OPEN-LOOP GAIN											
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}; V_O = 1\text{ V to }11\text{ V}; R_L \geq 2\text{ k}\Omega$			25	100	V/mV				
					$T_A = 0^\circ\text{C to }70^\circ\text{C}$	15					
FREQUENCY RESPONSE											
GBW	Gain bandwidth product					0.7	MHz				
SR	Slew rate	$G = +1$				0.3	$\text{V}/\mu\text{s}$				
OUTPUT											
V_O	Voltage output swing from rail	Positive rail					V				
								$V_S = 30\text{ V}; R_L = 2\text{ k}\Omega$	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	4	
								$V_S = 30\text{ V}; R_L \geq 10\text{ k}\Omega$		2	3
		$V_S = 5\text{ V}; R_L \geq 2\text{ k}\Omega$		1.5							
Negative rail	$V_S = 5\text{ V}; R_L \leq 10\text{ k}\Omega$	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	5	20	mV						
I_O	Output current	Source	$V_S = 15\text{ V}; V_O = 0\text{ V}; V_{ID} = 1\text{ V}$				mA				
								LM358A	-60		
		Sink	$V_S = 15\text{ V}; V_O = 15\text{ V}; V_{ID} = -1\text{ V}$					-10			
								$T_A = 0^\circ\text{C to }70^\circ\text{C}$	10	20	
		$V_{ID} = -1\text{ V}; V_O = 200\text{ mV}$				12	μA				
I_{SC}	Short-circuit current	$V_S = 10\text{ V}; V_O = V_S/2$				± 40	± 60	mA			
POWER SUPPLY											
I_Q	Quiescent current per amplifier	$V_O = 2.5\text{ V}; I_O = 0\text{ A}$				350	600	μA			
		$V_S = 30\text{ V}; V_O = 15\text{ V}; I_O = 0\text{ A}$				500	1000				

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM358 and LM358A.

(2) All typical values are $T_A = 25^\circ\text{C}$.

6.8 Electrical Characteristics: LM2904, LM2904V

For $V_S = (V+) - (V-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	$V_S = 5\text{ V}$ to maximum; $V_{CM} = 0\text{ V}$; $V_O = 1.4\text{ V}$	Non-A suffix devices	$T_A = -40^\circ\text{C}$ to 125°C	3	7	mV
			A-suffix devices		1	2	
dV_{OS}/dT	Input offset voltage drift			$T_A = -40^\circ\text{C}$ to 125°C	7		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5\text{ V}$ to 30 V			65	100	dB
V_{O1}/V_{O2}	Channel separation	$f = 1\text{ kHz}$ to 20 kHz				120	dB
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	$V_S = 5\text{ V}$ to maximum			(V-)	(V+) - 1.5	V
			$T_A = -40^\circ\text{C}$ to 125°C		(V-)	(V+) - 2	
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V}$ to maximum; $V_{CM} = 0\text{ V}$			65	80	dB
INPUT BIAS CURRENT							
I_B	Input bias current	$V_O = 1.4\text{ V}$			-20	-250	nA
			$T_A = -40^\circ\text{C}$ to 125°C				
I_{OS}	Input offset current	$V_O = 1.4\text{ V}$	Non-V suffix device	$T_A = -40^\circ\text{C}$ to 125°C	2	50	nA
			V-suffix device		2	50	
dI_{OS}/dT	Input offset current drift			$T_A = -40^\circ\text{C}$ to 125°C	10		$\text{pA}/^\circ\text{C}$
NOISE							
e_n	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = 1\text{ V}$ to 11 V ; $R_L \geq 2\text{ k}\Omega$			25	100	V/mV
			$T_A = -40^\circ\text{C}$ to 125°C			15	
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				0.7		MHz
SR	Slew rate	$G = +1$			0.3		$\text{V}/\mu\text{s}$
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	$R_L \geq 10\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to 125°C	$V_S = 1.5$		V
					Non-V suffix device	$V_S = \text{maximum}$; $R_L = 2\text{ k}\Omega$	
		V-suffix device	$V_S = \text{maximum}$; $R_L \geq 10\text{ k}\Omega$		2	3	
			$V_S = \text{maximum}$; $R_L = 2\text{ k}\Omega$		6		
Negative rail	$V_S = 5\text{ V}$; $R_L \leq 10\text{ k}\Omega$	$T_A = -40^\circ\text{C}$ to 125°C	5	20	mV		
I_O	Output current	$V_S = 15\text{ V}$; $V_O = 0\text{ V}$; $V_{ID} = 1\text{ V}$	Source	$T_A = -40^\circ\text{C}$ to 125°C	-20	-30	mA
					$T_A = -40^\circ\text{C}$ to 125°C	-10	
		$V_S = 15\text{ V}$; $V_O = 15\text{ V}$; $V_{ID} = -1\text{ V}$	Sink		10	20	
					$T_A = -40^\circ\text{C}$ to 125°C	5	
$V_{ID} = -1\text{ V}$; $V_O = 200\text{ mV}$		Non-V suffix device	30		μA		
		V-suffix device	12	40			
I_{SC}	Short-circuit current	$V_S = 10\text{ V}$; $V_O = V_S/2$			± 40	± 60	mA
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$V_O = 2.5\text{ V}$; $I_O = 0\text{ A}$	$T_A = -40^\circ\text{C}$ to 125°C	350	600	μA	
		$V_S = \text{maximum}$; $V_O = \text{maximum}/2$; $I_O = 0\text{ A}$		500	1000		

- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 26 V for LM2904 and 32 V for LM2904V.
- All typical values are $T_A = 25^\circ\text{C}$.

6.9 Electrical Characteristics: LM158, LM158A

For $V_S = (V_+) - (V_-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT	
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$; $V_{CM} = 0\text{ V}$; $V_O = 1.4\text{ V}$	LM158		3	5	mV	
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$		7		
			LM158A		2	4		
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$				
dV_{OS}/dT	Input offset voltage drift		LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$	
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	7	15 ⁽³⁾		
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5\text{ V to }30\text{ V}$			65	100	dB	
V_{O1}/V_{O2}	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$				120	dB	
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range	$V_S = 5\text{ V to }30\text{ V}$	LM158		(V-)	(V+) - 1.5	V	
		$V_S = 30\text{ V}$	LM158A					
		$V_S = 5\text{ V to }30\text{ V}$	LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	(V-)	(V+) - 2		
		$V_S = 30\text{ V}$	LM158A					
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V to }30\text{ V}$; $V_{CM} = 0\text{ V}$			70	80	dB	
INPUT BIAS CURRENT								
I_B	Input bias current	$V_O = 1.4\text{ V}$	LM158		-20	-150	nA	
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$		-300		
			LM158A		-15	-50		
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$		-100		
I_{OS}	Input offset current	$V_O = 1.4\text{ V}$	LM158		2	30	nA	
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$		100		
			LM158A		2	10		
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$		30		
dI_{OS}/dT	Input offset current drift				10		$\text{pA}/^\circ\text{C}$	
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		200		
NOISE								
e_n	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = 1\text{ V to }11\text{ V}$; $R_L \geq 2\text{ k}\Omega$			50	100	V/mV	
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$	25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				0.7		MHz	
SR	Slew rate	$G = +1$			0.3		V/ μs	
OUTPUT								
V_O	Voltage output swing from rail	Positive rail	$V_S = 30\text{ V}$; $R_L = 2\text{ k}\Omega$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		4	V	
			$V_S = 30\text{ V}$; $R_L \geq 10\text{ k}\Omega$		2	3		
			$V_S = 5\text{ V}$; $R_L \geq 2\text{ k}\Omega$			1.5		
		Negative rail	$V_S = 5\text{ V}$; $R_L \leq 10\text{ k}\Omega$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		5	20	mV
I_O	Output current	$V_S = 15\text{ V}$; $V_O = 0\text{ V}$; $V_{ID} = 1\text{ V}$	Source	LM158A		-20	-30	mA
					$T_A = -55^\circ\text{C to }125^\circ\text{C}$	-10	20	
		$V_S = 15\text{ V}$; $V_O = 15\text{ V}$; $V_{ID} = -1\text{ V}$	Sink			10	20	
					$T_A = -55^\circ\text{C to }125^\circ\text{C}$	5		
	$V_{ID} = -1\text{ V}$; $V_O = 200\text{ mV}$			12	30	μA		
I_{SC}	Short-circuit current	$V_S = 10\text{ V}$; $V_O = V_S/2$			± 40	± 60	mA	

6.9 Electrical Characteristics: LM158, LM158A (continued)

For $V_S = (V+) - (V-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current per amplifier	$V_O = 2.5\text{ V}; I_O = 0\text{ A}$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		350	600	μA
		$V_S = 30\text{ V}; V_O = 15\text{ V}; I_O = 0\text{ A}$			500	1000	

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM158 and LM158A.
- (2) All typical values are $T_A = 25^\circ\text{C}$.
- (3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Electrical Characteristics: LM258, LM258A

For $V_S = (V_+) - (V_-) = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

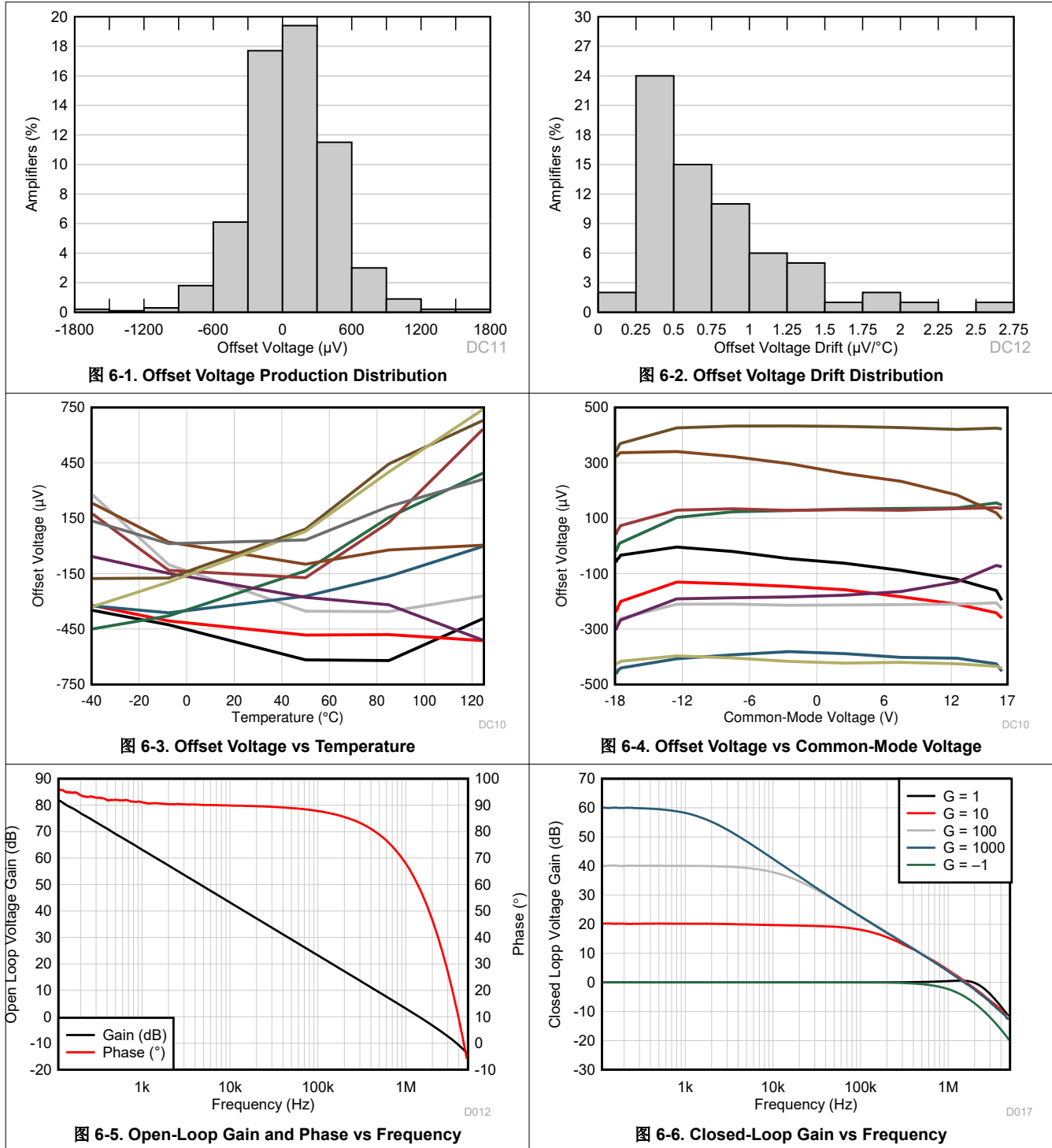
PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT	
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$; $V_{CM} = 0\text{ V}$; $V_O = 1.4\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	3	5	mV	
					7			
LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$		2	3				
			4					
dV_{OS}/dT	Input offset voltage drift		LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$	
					7	15		
LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$							
PSRR	Input offset voltage vs power supply ($\Delta V_{IO}/\Delta V_S$)	$V_S = 5\text{ V to }30\text{ V}$			65	100	dB	
V_{O1}/V_{O2}	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$				120	dB	
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range			$T_A = -25^\circ\text{C to }85^\circ\text{C}$	(V_-)	$(V_+) - 1.5$	V	
								LM258
					LM258A	$V_S = 30\text{ V}$		
								(V_-)
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V to }30\text{ V}$; $V_{CM} = 0\text{ V}$			70	80	dB	
INPUT BIAS CURRENT								
I_B	Input bias current	$V_O = 1.4\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	-20	-150	nA	
					-300			
LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$		-15	-80				
			-100					
I_{OS}	Input offset current	$V_O = 1.4\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	2	30	nA	
					100			
LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$		2	15				
			30					
dI_{OS}/dT	Input offset current drift				10		$\text{pA}/^\circ\text{C}$	
			LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$		200		
NOISE								
e_n	Input voltage noise density	$f = 1\text{ kHz}$				40	$\text{nV}/\sqrt{\text{Hz}}$	
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	$V_S = 15\text{ V}$; $V_O = 1\text{ V to }11\text{ V}$; $R_L \geq 2\text{ k}\Omega$		$T_A = -25^\circ\text{C to }85^\circ\text{C}$	50	100	V/mV	
					25			
FREQUENCY RESPONSE								
GBW	Gain bandwidth product				0.7		MHz	
SR	Slew rate	$G = +1$			0.3		V/ μs	
OUTPUT								
V_O	Voltage output swing from rail	Positive rail		$T_A = -25^\circ\text{C to }85^\circ\text{C}$	$V_S = 30\text{ V}$; $R_L = 2\text{ k}\Omega$	4	V	
					$V_S = 30\text{ V}$; $R_L \geq 10\text{ k}\Omega$	2		3
		$V_S = 5\text{ V}$; $R_L \geq 2\text{ k}\Omega$			1.5			
		Negative rail			$V_S = 5\text{ V}$; $R_L \leq 10\text{ k}\Omega$	5		20
I_O	Output current	$V_S = 15\text{ V}$; $V_O = 0\text{ V}$; $V_{ID} = 1\text{ V}$	Source	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	-20	-30	mA	
					LM258A	-60		
		$V_S = 15\text{ V}$; $V_O = 15\text{ V}$; $V_{ID} = -1\text{ V}$			Sink	10		20
						$T_A = -25^\circ\text{C to }85^\circ\text{C}$		5
$V_{ID} = -1\text{ V}$; $V_O = 200\text{ mV}$		12	30	μA				
I_{SC}	Short-circuit current	$V_S = 10\text{ V}$; $V_O = V_S/2$			± 40	± 60	mA	
POWER SUPPLY								
I_Q	Quiescent current per amplifier	$V_O = 2.5\text{ V}$; $I_O = 0\text{ A}$		$T_A = -25^\circ\text{C to }85^\circ\text{C}$	350	600	μA	
		$V_S = 30\text{ V}$; $V_O = 15\text{ V}$; $I_O = 0\text{ A}$			500	1000		

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum V_S for testing purposes is 30 V for LM258 and LM258A.

(2) All typical values are $T_A = 25^\circ\text{C}$.

6.11 Typical Characteristics: LM358B and LM2904B

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{\text{CM}} = V_S / 2$, $R_{\text{LOAD}} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

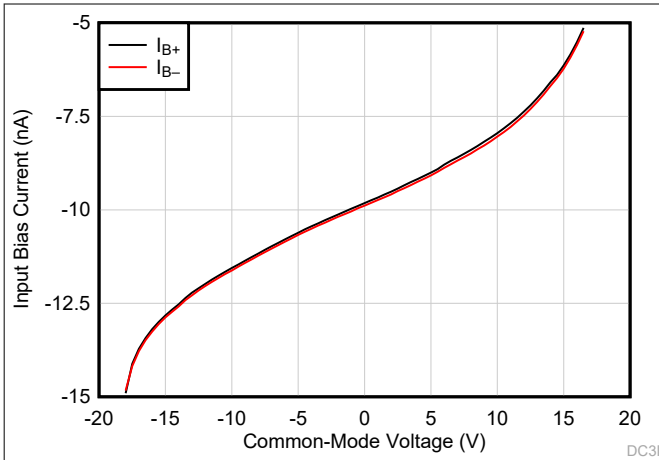


图 6-7. Input Bias Current vs Common-Mode Voltage

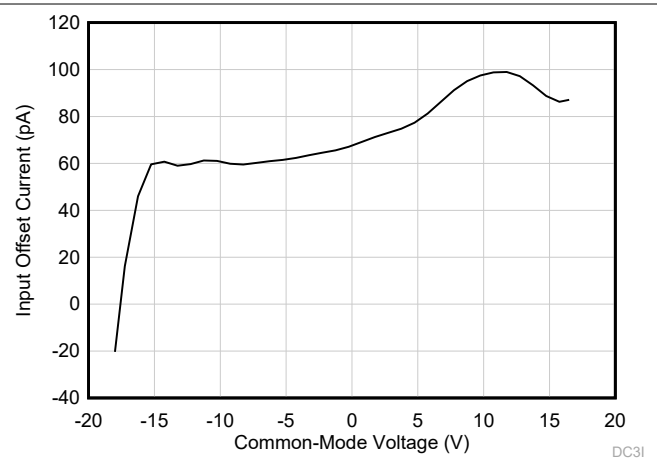


图 6-8. Input Offset Current vs Common-Mode Voltage

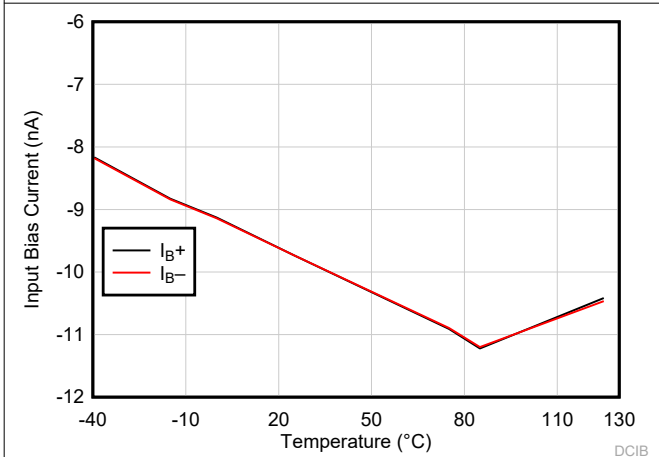


图 6-9. Input Bias Current vs Temperature

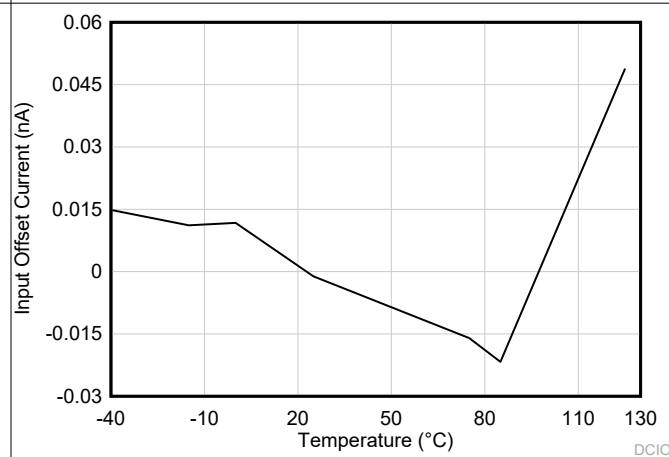


图 6-10. Input Offset Current vs Temperature

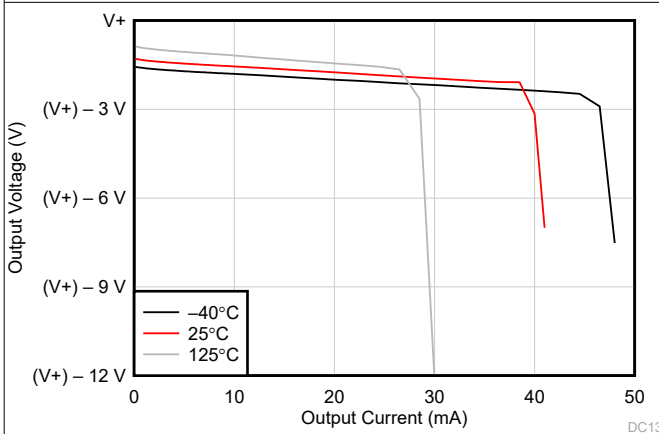


图 6-11. Output Voltage Swing vs Output Current (Sourcing)

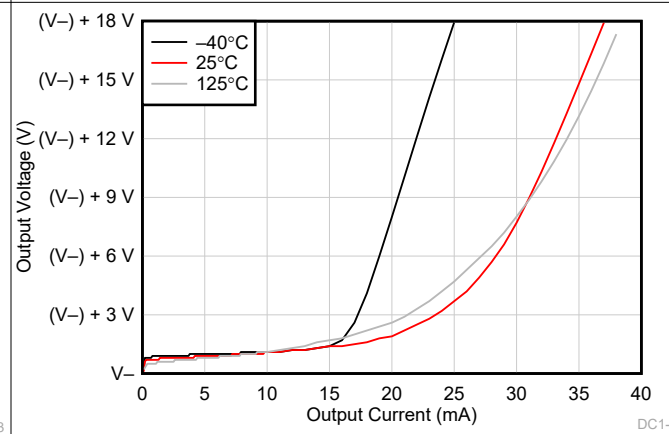


图 6-12. Output Voltage Swing vs Output Current (Sinking)

6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

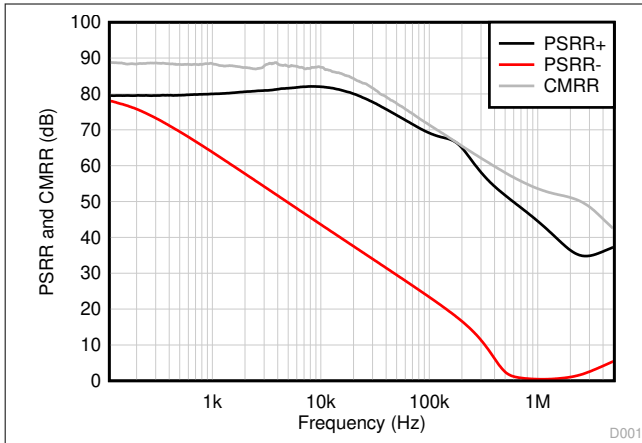


图 6-13. CMRR and PSRR vs Frequency

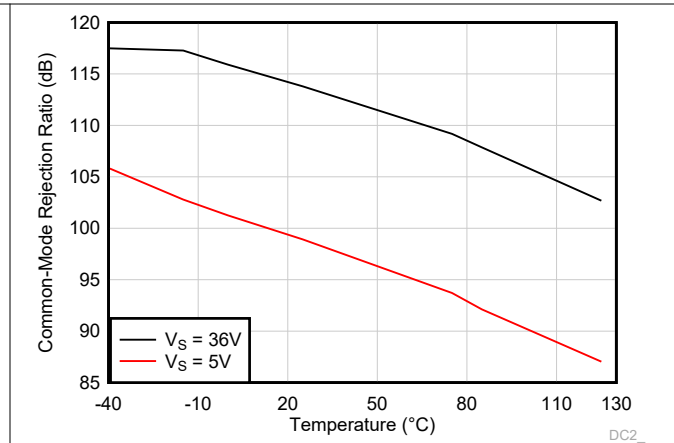


图 6-14. Common-Mode Rejection Ratio vs Temperature (dB)

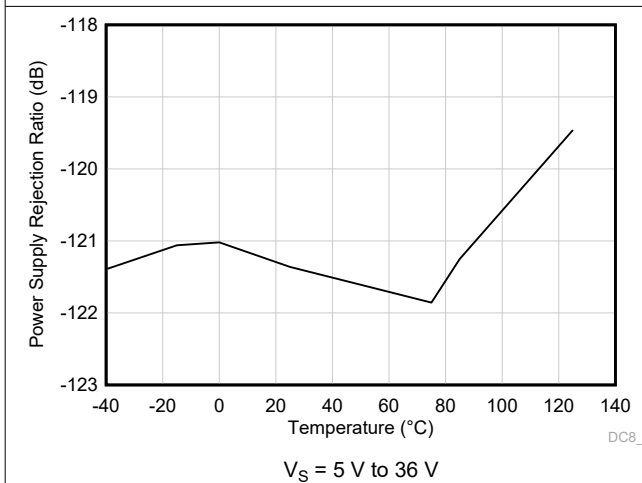


图 6-15. Power Supply Rejection Ratio vs Temperature (dB)

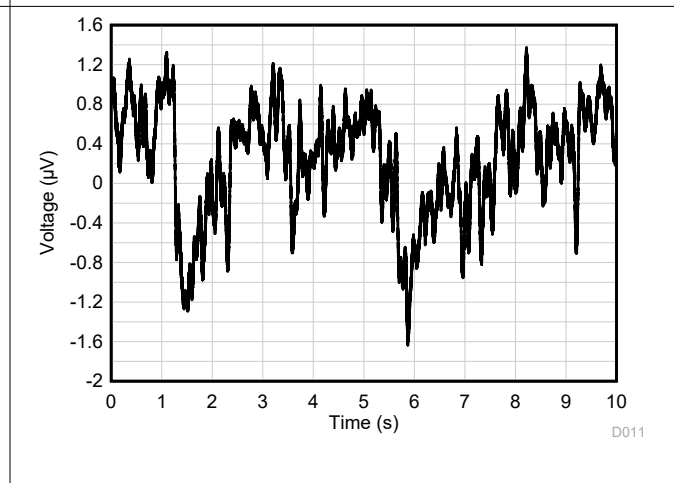


图 6-16. 0.1-Hz to 10-Hz Noise

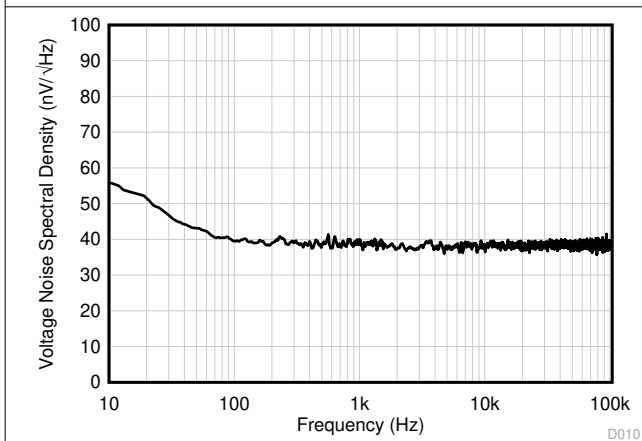
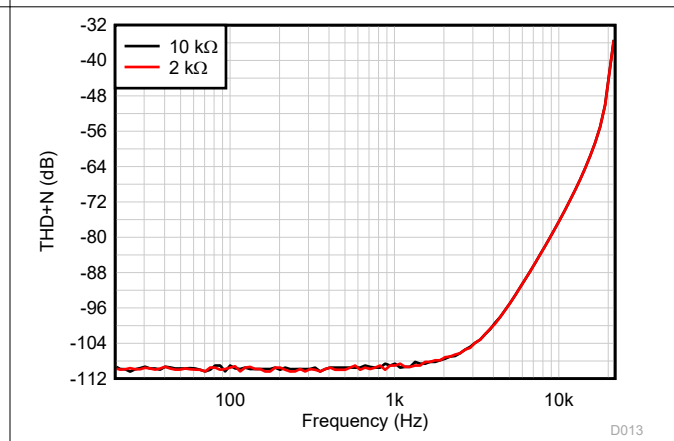


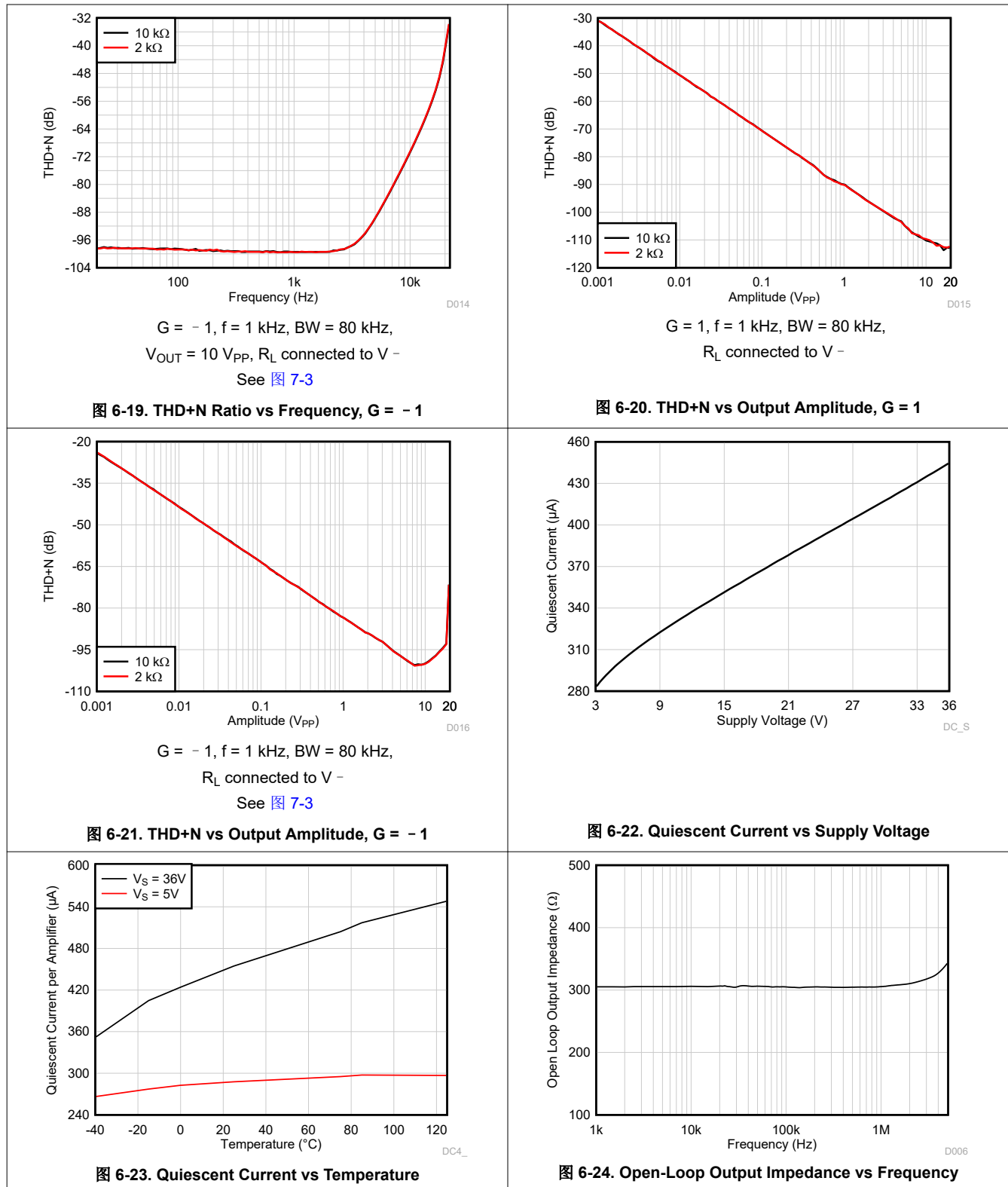
图 6-17. Input Voltage Noise Spectral Density vs Frequency



G = 1, f = 1 kHz, BW = 80 kHz,
 $V_{OUT} = 10\text{ V}_{PP}$, R_L connected to V -
 图 6-18. THD+N Ratio vs Frequency, G = 1

6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).

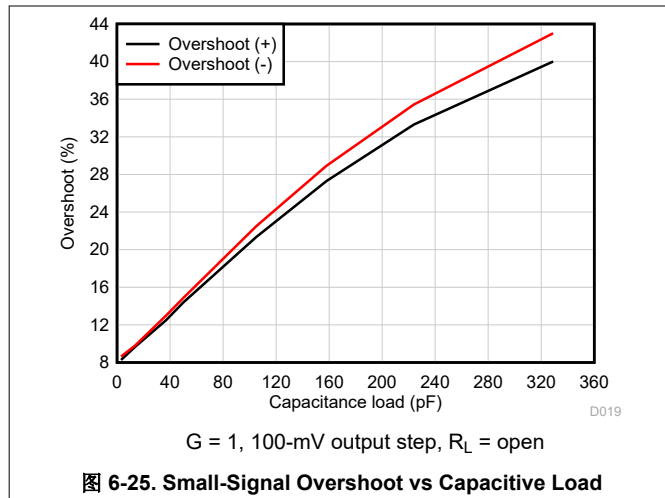


图 6-25. Small-Signal Overshoot vs Capacitive Load

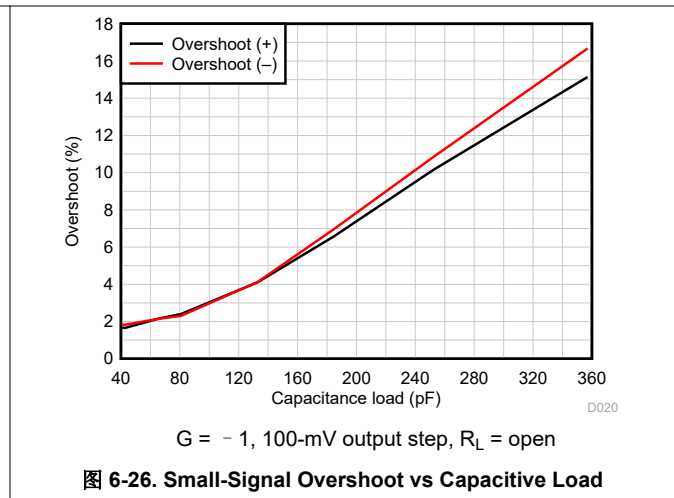


图 6-26. Small-Signal Overshoot vs Capacitive Load

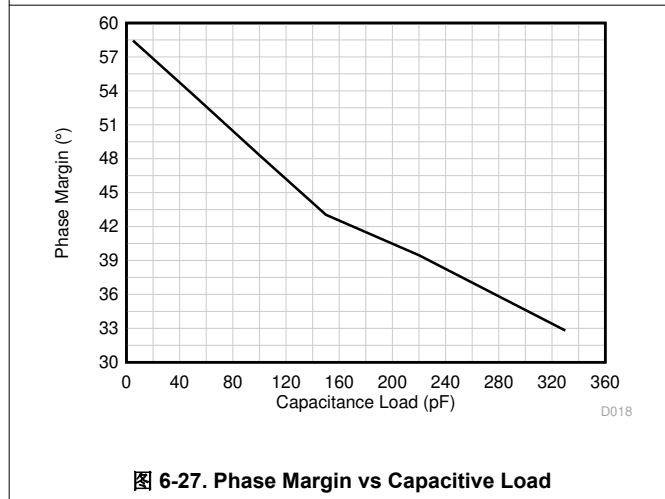


图 6-27. Phase Margin vs Capacitive Load

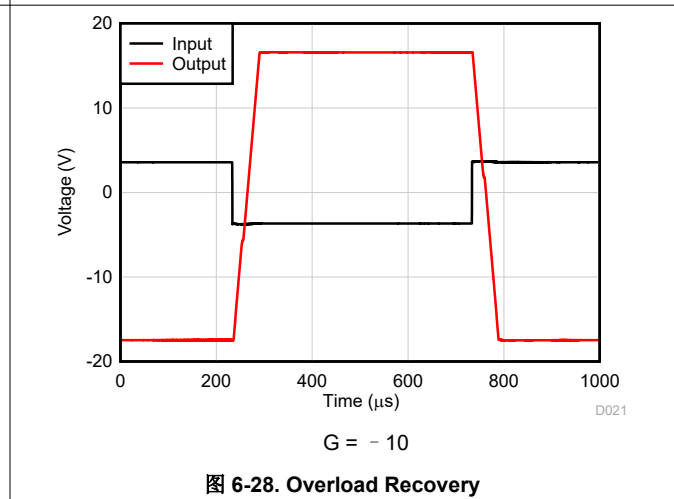


图 6-28. Overload Recovery

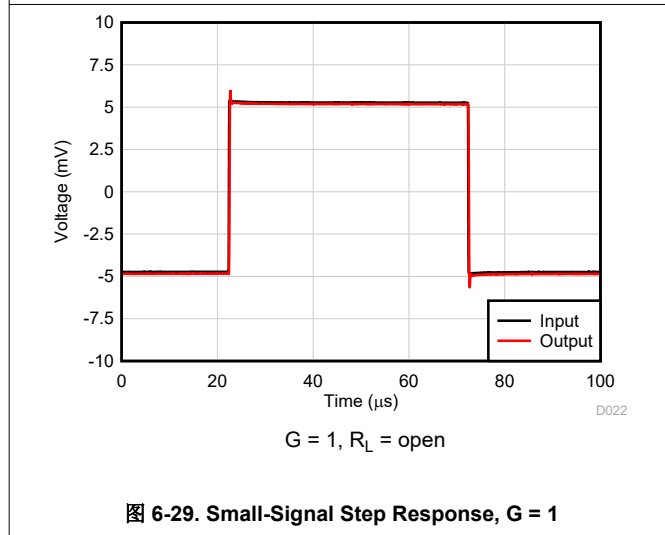


图 6-29. Small-Signal Step Response, $G = 1$

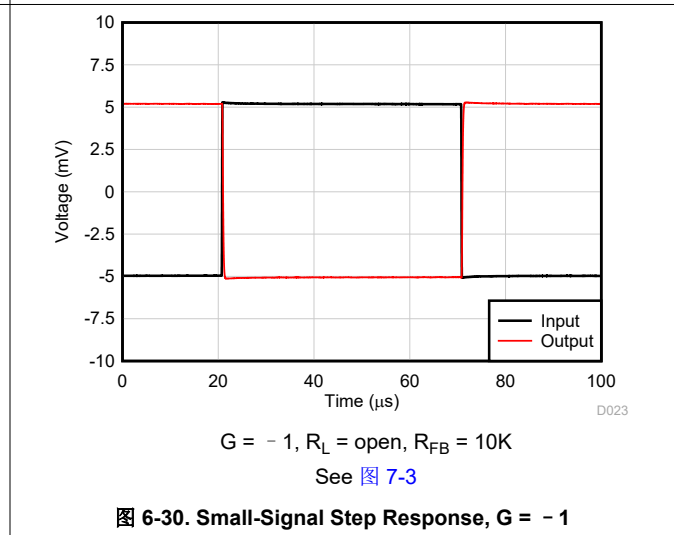
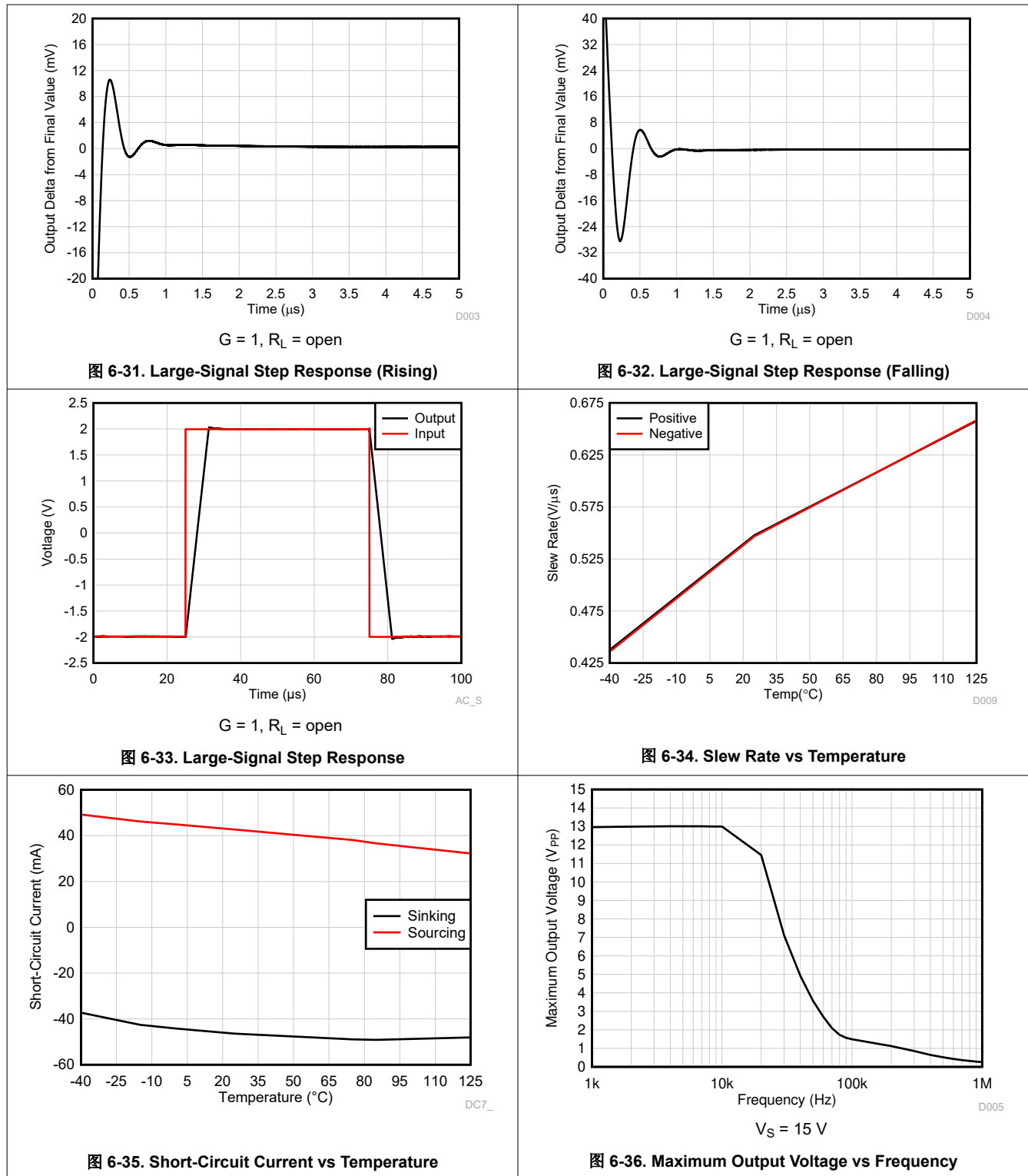


图 6-30. Small-Signal Step Response, $G = -1$

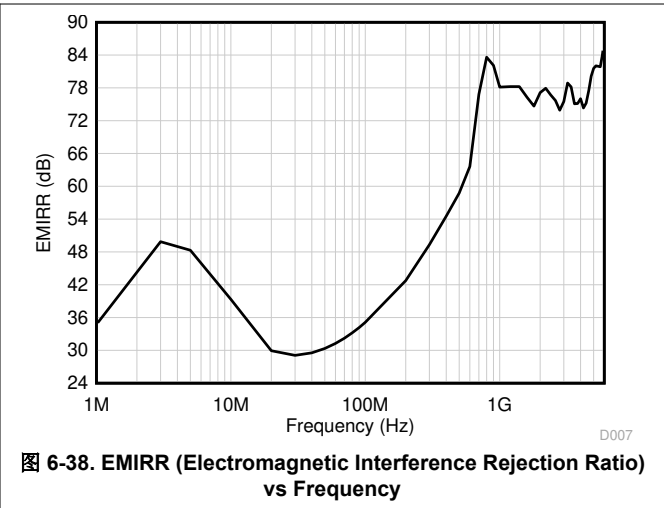
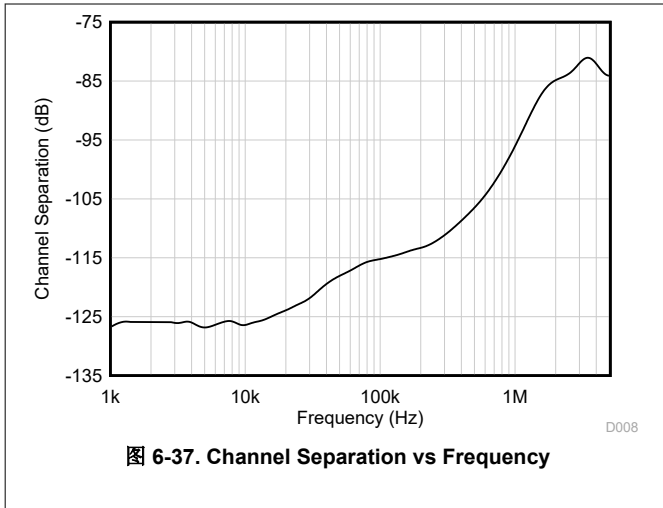
6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



6.11 Typical Characteristics: LM358B and LM2904B (continued)

This typical characteristics section is applicable for LM358B and LM2904B. Typical characteristics data in this section was taken with $T_A = 25^\circ\text{C}$, $V_S = 36\text{ V}$ ($\pm 18\text{ V}$), $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted).



6.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

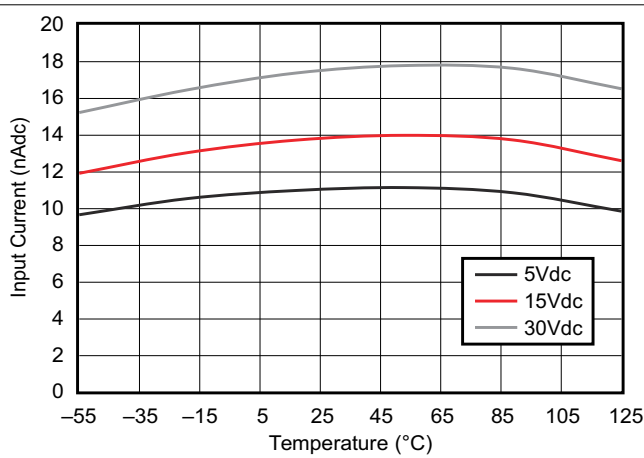


图 6-39. Input Current vs Temperature

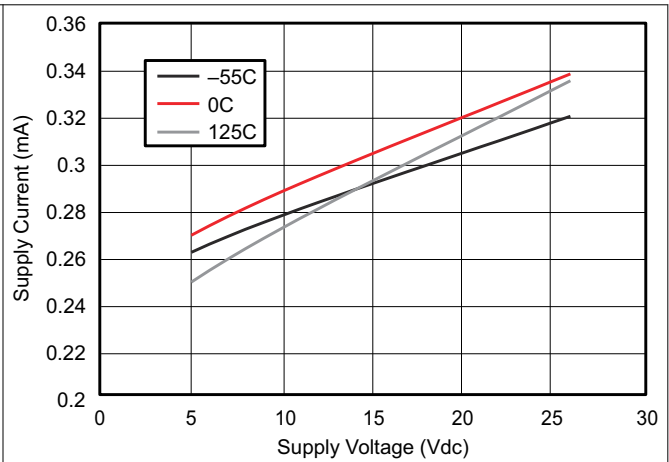


图 6-40. Supply Current vs Supply Voltage

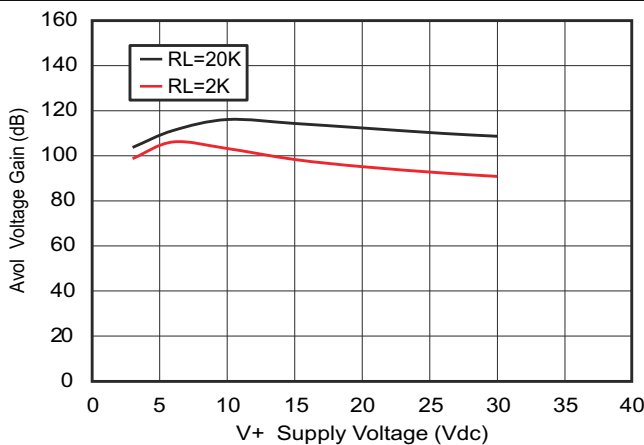


图 6-41. Voltage Gain vs Supply Voltage

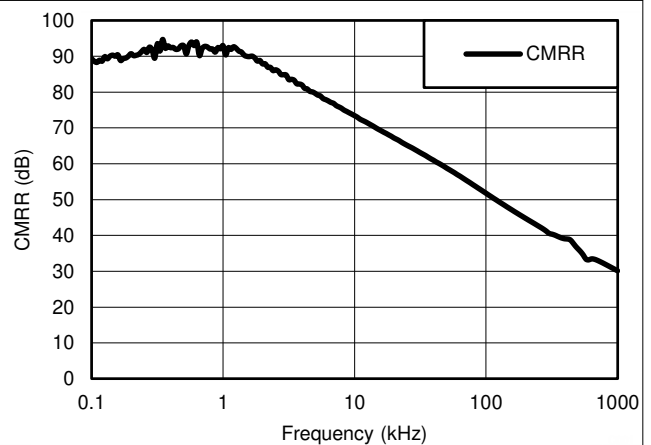


图 6-42. Common-Mode Rejection Ratio vs Frequency

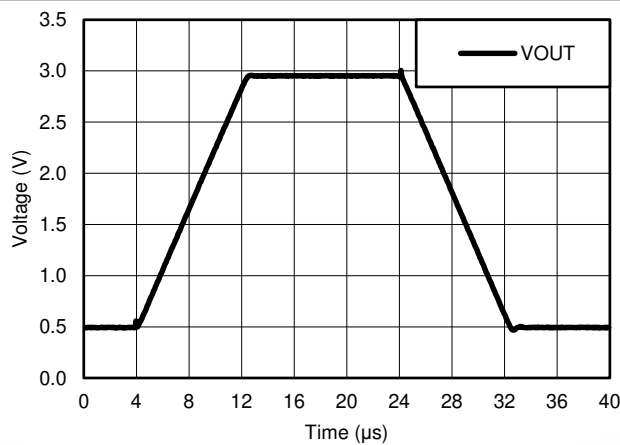


图 6-43. Voltage Follower Large Signal Response (50 pF)

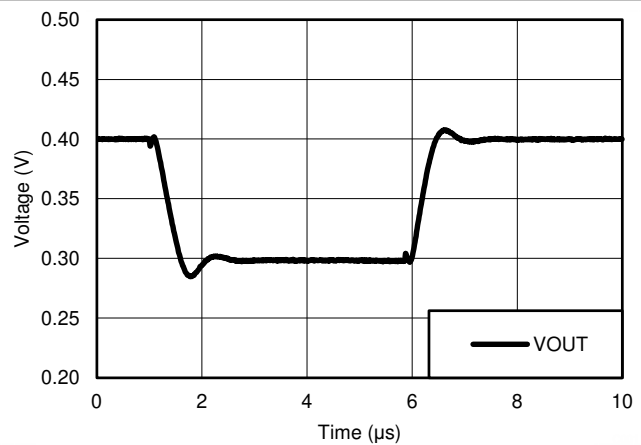


图 6-44. Voltage Follower Small Signal Response (50 pF)

6.12 Typical Characteristics: LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V (continued)

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

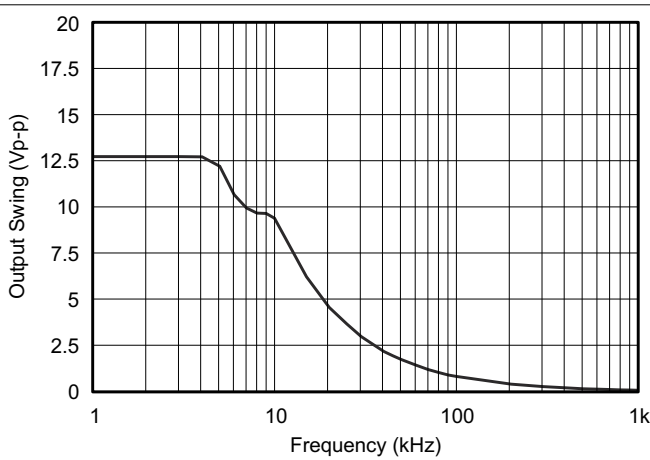


图 6-45. Maximum Output Swing vs Frequency ($V_{CC} = 15\text{ V}$)

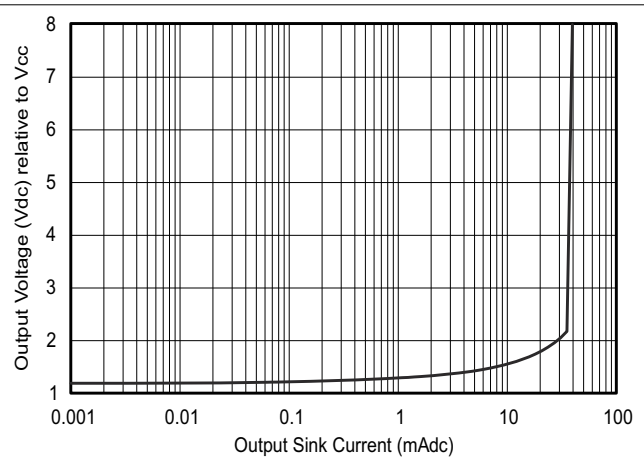


图 6-46. Output Sourcing Characteristics

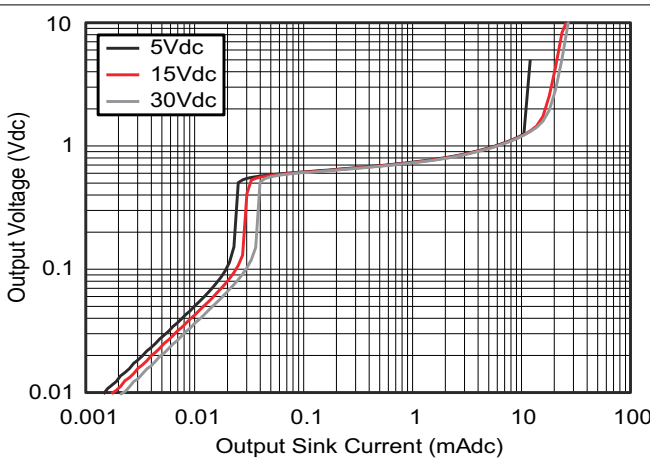


图 6-47. Output Sinking Characteristics

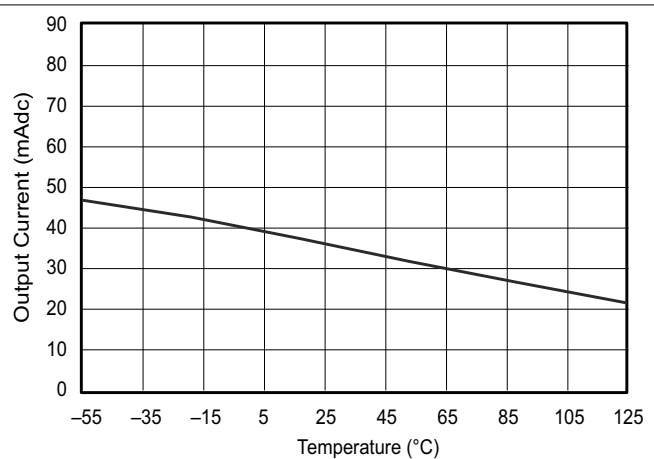


图 6-48. Source Current Limiting

7 Parameter Measurement Information

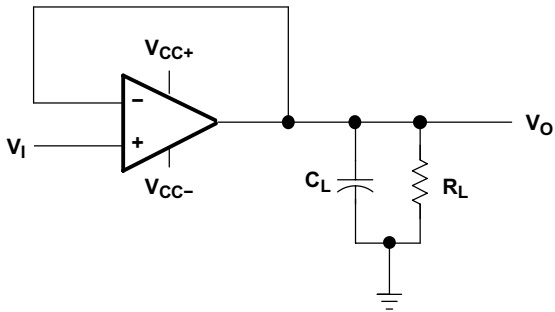


图 7-1. Unity-Gain Amplifier

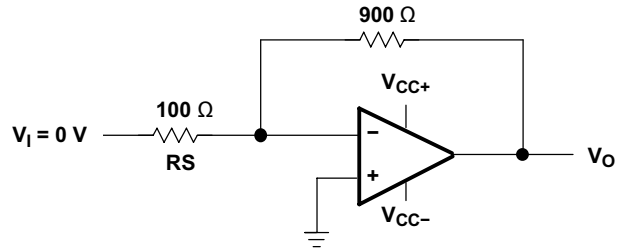


图 7-2. Noise-Test Circuit

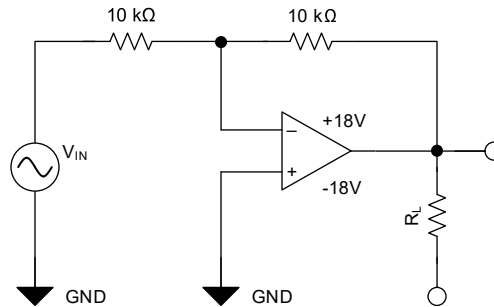


图 7-3. Test Circuit, $G = -1$, for THD+N and Small-Signal Step Response

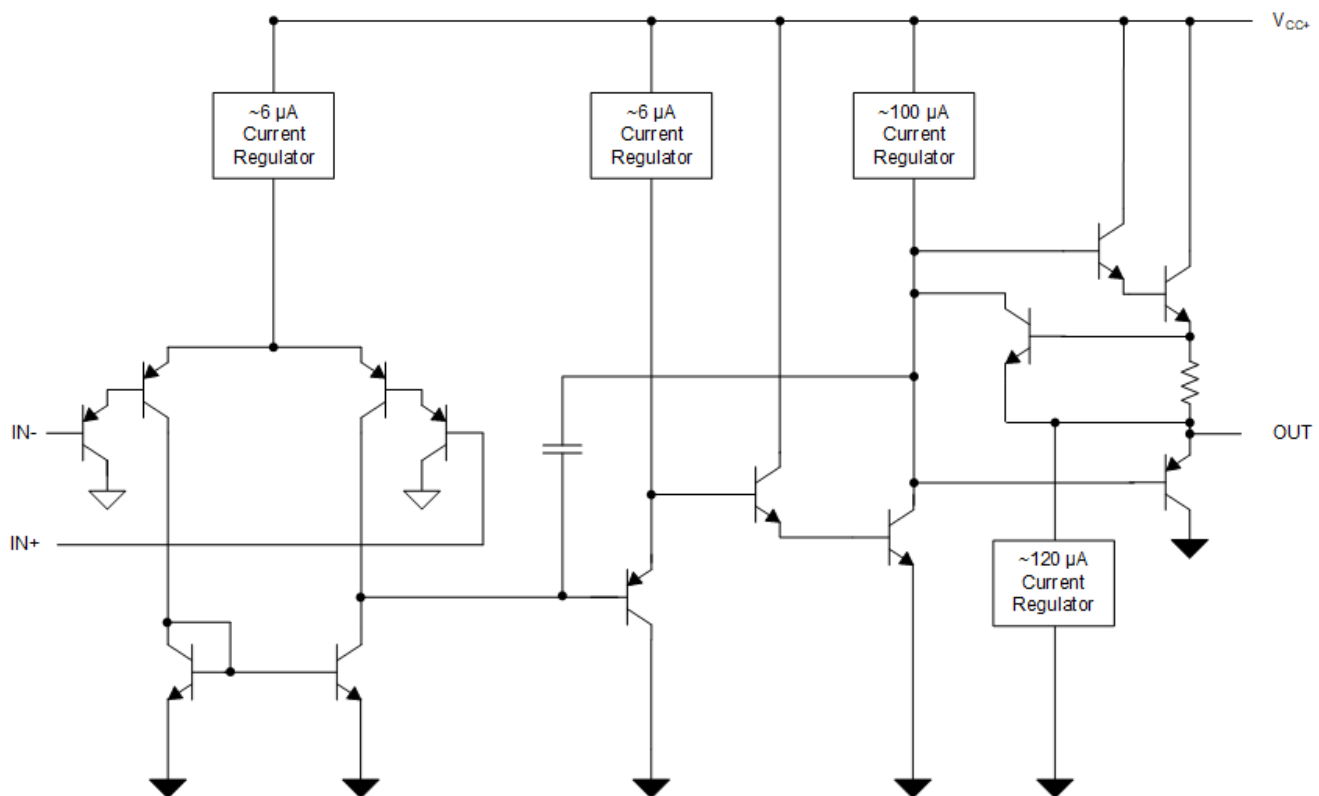
8 Detailed Description

8.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in 节 6.3 and V_S is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional ± 5 -V supplies.

8.2 Functional Block Diagram: LM358B, LM358BA, LM2904B, LM2904BA



8.3 Feature Description

8.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (B Version).

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ μ s slew rate (B Version).

8.3.3 Input Common Mode Range

The valid common mode range is from device ground to $V_S - 1.5\text{ V}$ ($V_S - 2\text{ V}$ across temperature). Inputs may exceed V_S up to the maximum V_S without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below V_- then input current should be limited to 1 mA and the output phase is undefined.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMx58 and LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before V_S for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

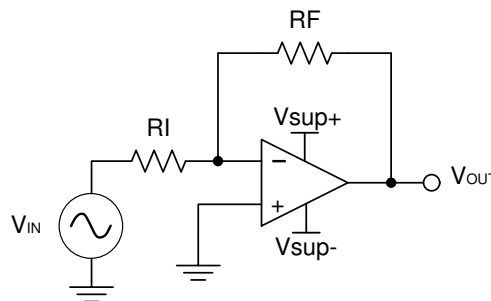


图 9-1. Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of ± 0.5 V to ± 1.8 V. Setting the supply at ± 12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [方程式 1](#) and [方程式 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for R_I or R_F . [Subscripts should be fixed in the accompanying figures and equations also.] Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamperage range. This ensures the part does not draw too much current. This example uses $10 \text{ k}\Omega$ for R_I which means $36 \text{ k}\Omega$ is used for R_F . This was determined by [方程式 3](#).

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

9.2.3 Application Curve

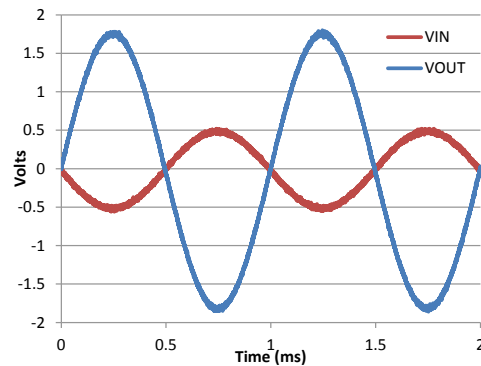


图 9-2. Input and Output Voltages of the Inverting Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see 节 6.1).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 11.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in 节 11.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

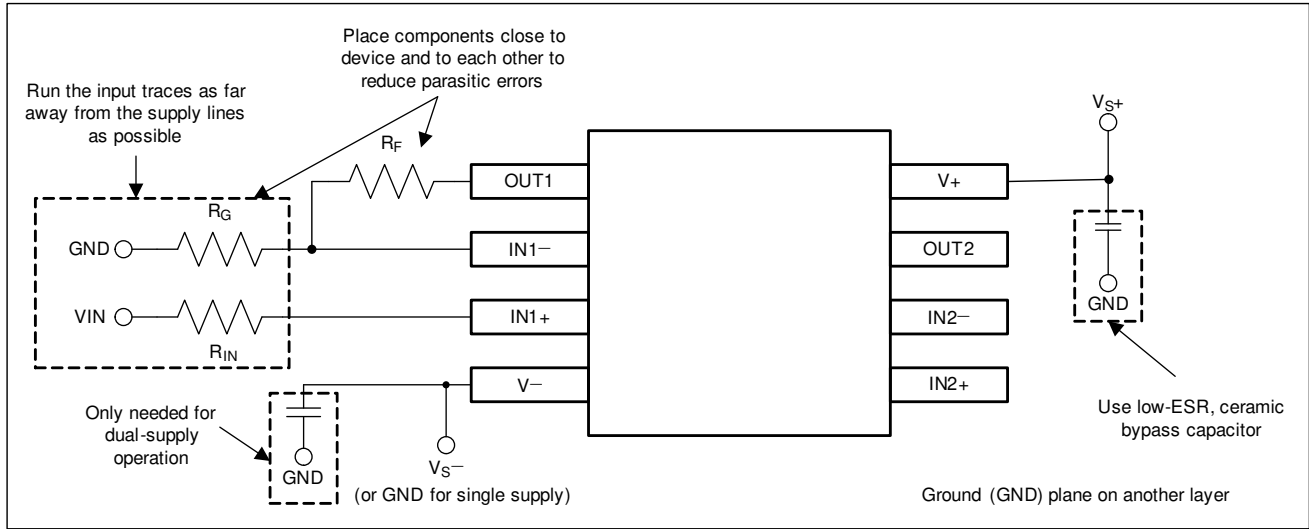


图 11-1. Operational Amplifier Board Layout for Noninverting Configuration

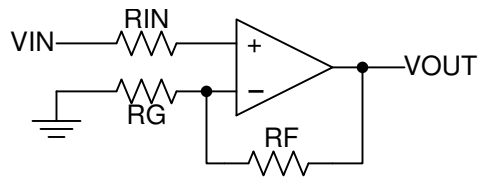


图 11-2. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87710012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710012A LM158FKB	Samples
5962-8771001PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	Samples
5962-87710022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710022A LM158AFKB	Samples
5962-8771002PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	Samples
LM158 MW8	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LM158AFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710022A LM158AFKB	Samples
LM158AJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158AJG	Samples
LM158AJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	Samples
LM158FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710012A LM158FKB	Samples
LM158JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158JG	Samples
LM158JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	Samples
LM258AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	
LM258ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M3L, M3P, M3S, M3U)	Samples
LM258ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples
LM258ADRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples
LM258ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-25 to 85	LM258AP	Samples
LM258APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	Samples
LM258D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	
LM258DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	
LM258DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2U)	Samples
LM258DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2U)	
LM258DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	Samples
LM258P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-25 to 85	LM258P	Samples
LM258PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258P	Samples
LM2904AVQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	Samples
LM2904BAIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2904A	Samples
LM2904BAIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	28CB	Samples
LM2904BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BA	Samples
LM2904BAIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904BA	Samples
LM2904BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	28BB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904B	Samples
LM2904BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904B	Samples
LM2904D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	
LM2904DE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	
LM2904DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	
LM2904DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	Samples
LM2904DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	
LM2904DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	Samples
LM2904P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-40 to 125	LM2904P	Samples
LM2904PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	Samples
LM2904PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	Samples
LM2904QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	Samples
LM2904VQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904VQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM2904VQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	Samples
LM358AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	
LM358ADE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	
LM358ADG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	
LM358ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6U)	Samples
LM358ADGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6U)	
LM358ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358ADRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	Samples
LM358AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM358AP	Samples
LM358APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	Samples
LM358APW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358APWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358APWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	Samples
LM358BAIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	358BA	Samples
LM358BAIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	28DB	Samples
LM358BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L358BA	Samples
LM358BAIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L358BA	Samples
LM358BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358	Samples
LM358BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	358B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358B	Samples
LM358BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358B	Samples
LM358D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358D-JF	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5U)	Samples
LM358DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5U)	
LM358DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	Samples
LM358P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PE3	ACTIVE	PDIP	P	8	50	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358P	Samples
LM358PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples
LM358PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM258A, LM2904, LM2904B, LM2904BA :

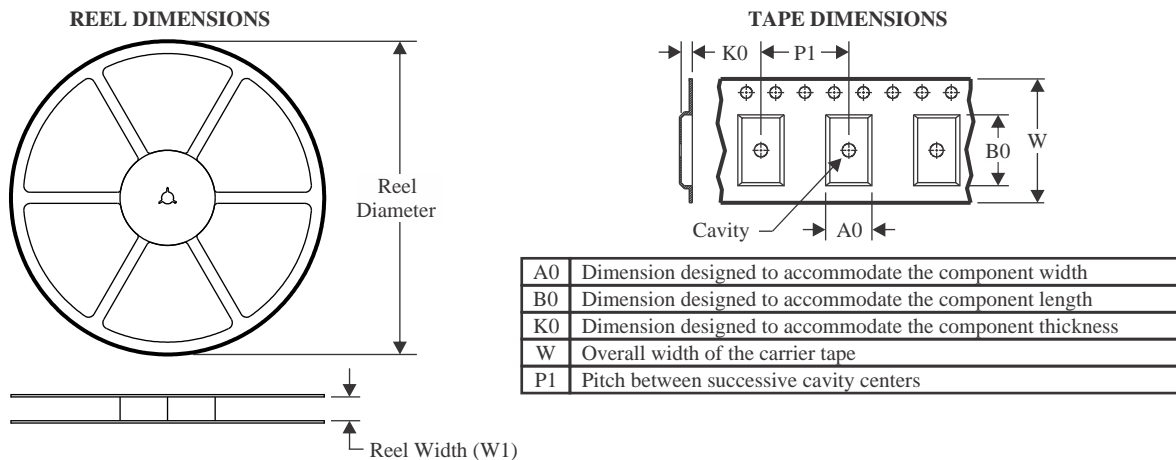
● Automotive : [LM2904-Q1](#), [LM2904B-Q1](#), [LM2904BA-Q1](#)

● Enhanced Product : [LM258A-EP](#), [LM2904-EP](#)

NOTE: Qualified Version Definitions:

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BAIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2904BAIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BAIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904BIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2904BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BAIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM358BAIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BAIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM358BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

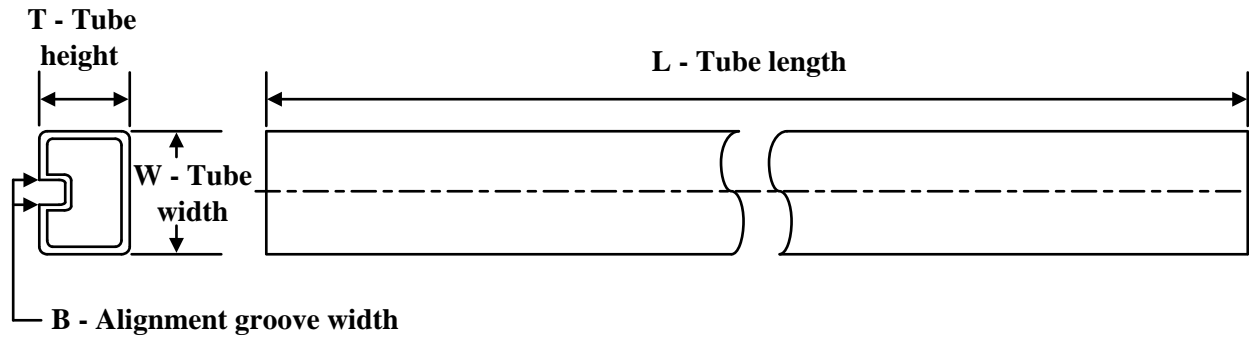

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM258ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM258ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM258ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM258ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM258DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	356.0	356.0	35.0
LM258DR	SOIC	D	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	340.5	336.1	25.0
LM258DR	SOIC	D	8	2500	340.5	336.1	25.0
LM258DR	SOIC	D	8	2500	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM258DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM258DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BAIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2904BAIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BAIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2904BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2904DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904DR	SOIC	D	8	2500	356.0	356.0	35.0
LM2904DR	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DR	SOIC	D	8	2500	356.0	356.0	35.0
LM2904DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM2904DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM2904DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM2904DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904PSR	SO	PS	8	2000	356.0	356.0	35.0
LM2904PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904PWRG4-JF	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904QDR	SOIC	D	8	2500	350.0	350.0	43.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2904VQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQDRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM358ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM358ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM358ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM358APWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358APWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358BAIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM358BAIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM358BAIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM358BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM358BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	356.0	356.0	35.0
LM358DR	SOIC	D	8	2500	356.0	356.0	35.0
LM358DR	SOIC	D	8	2500	340.5	336.1	25.0
LM358DR	SOIC	D	8	2500	340.5	336.1	25.0
LM358DR	SOIC	D	8	2500	364.0	364.0	27.0
LM358DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM358DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM358DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM358DRG4	SOIC	D	8	2500	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM358PSR	SO	PS	8	2000	356.0	356.0	35.0
LM358PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM358PWRG4-JF	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87710012A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-87710022A	FK	LCCC	20	1	506.98	12.06	2030	NA
LM158AFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
LM158FKB	FK	LCCC	20	1	506.98	12.06	2030	NA
LM258AD	D	SOIC	8	75	506.6	8	3940	4.32
LM258AD	D	SOIC	8	75	507	8	3940	4.32
LM258AP	P	PDIP	8	50	506.1	9	600	5.4
LM258AP	P	PDIP	8	50	506	13.97	11230	4.32
LM258APE4	P	PDIP	8	50	506	13.97	11230	4.32
LM258D	D	SOIC	8	75	507	8	3940	4.32
LM258D	D	SOIC	8	75	506.6	8	3940	4.32
LM258DG4	D	SOIC	8	75	507	8	3940	4.32
LM258DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM258P	P	PDIP	8	50	506	13.97	11230	4.32
LM258P	P	PDIP	8	50	506.1	9	600	5.4
LM258PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM2904D	D	SOIC	8	75	507	8	3940	4.32
LM2904D	D	SOIC	8	75	506.6	8	3940	4.32
LM2904DE4	D	SOIC	8	75	506.6	8	3940	4.32
LM2904DE4	D	SOIC	8	75	507	8	3940	4.32
LM2904DG4	D	SOIC	8	75	507	8	3940	4.32
LM2904DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM2904P	P	PDIP	8	50	506	13.97	11230	4.32
LM2904P	P	PDIP	8	50	506.1	9	600	5.4
LM2904PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM2904PW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM358AD	D	SOIC	8	75	506.6	8	3940	4.32
LM358AD	D	SOIC	8	75	507	8	3940	4.32
LM358ADE4	D	SOIC	8	75	507	8	3940	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM358ADE4	D	SOIC	8	75	506.6	8	3940	4.32
LM358ADG4	D	SOIC	8	75	507	8	3940	4.32
LM358ADG4	D	SOIC	8	75	506.6	8	3940	4.32
LM358AP	P	PDIP	8	50	506.1	9	600	5.4
LM358AP	P	PDIP	8	50	506	13.97	11230	4.32
LM358APE4	P	PDIP	8	50	506	13.97	11230	4.32
LM358APW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM358D	D	SOIC	8	75	507	8	3940	4.32
LM358D	D	SOIC	8	75	506.6	8	3940	4.32
LM358D-JF	D	SOIC	8	75	507	8	3940	4.32
LM358D-JF	D	SOIC	8	75	506.6	8	3940	4.32
LM358DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM358DG4	D	SOIC	8	75	507	8	3940	4.32
LM358P	P	PDIP	8	50	506.1	9	600	5.4
LM358P	P	PDIP	8	50	506	13.97	11230	4.32
LM358PE3	P	PDIP	8	50	506.1	9	600	5.4
LM358PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM358PW	PW	TSSOP	8	150	530	10.2	3600	3.5



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

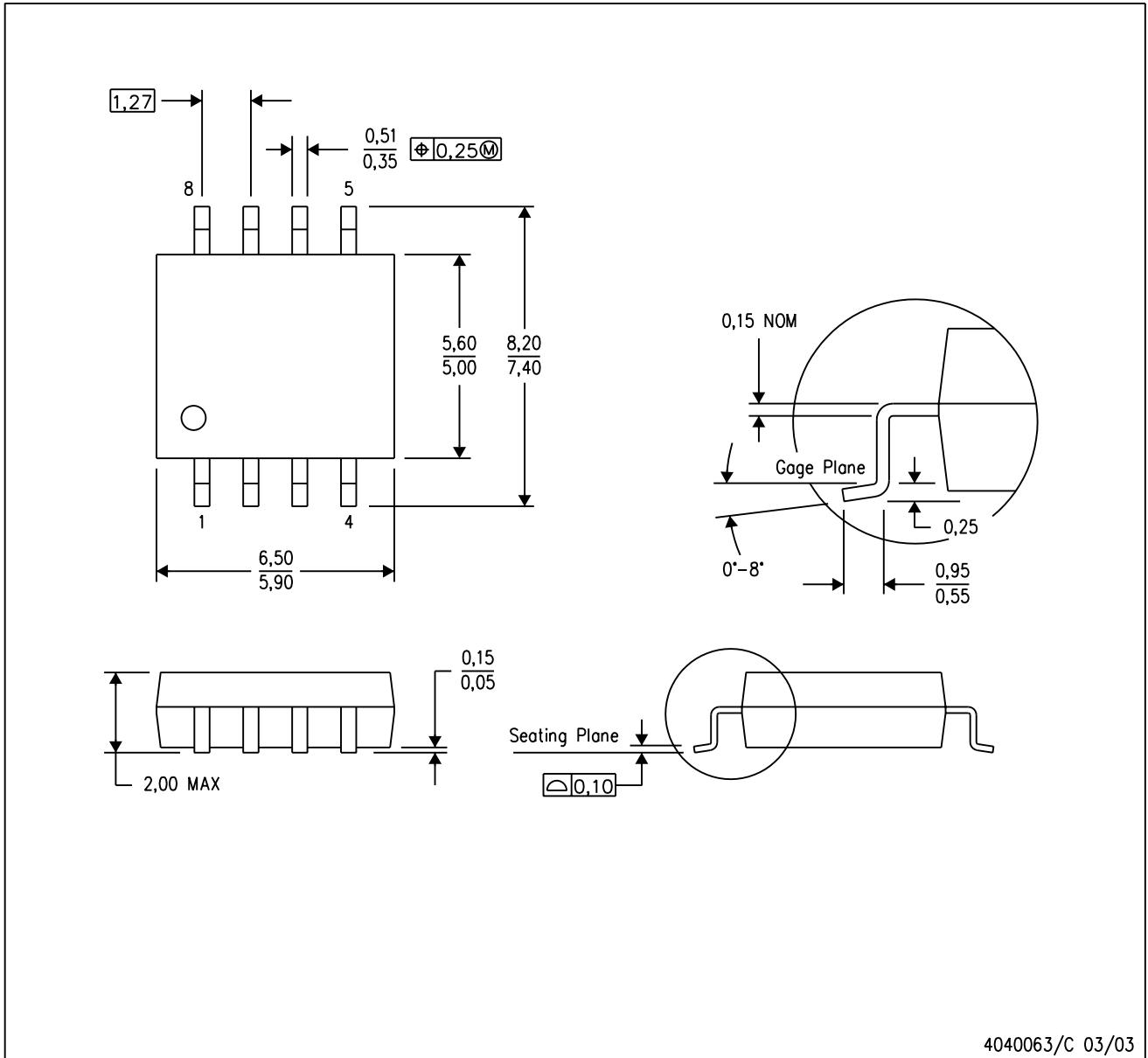
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

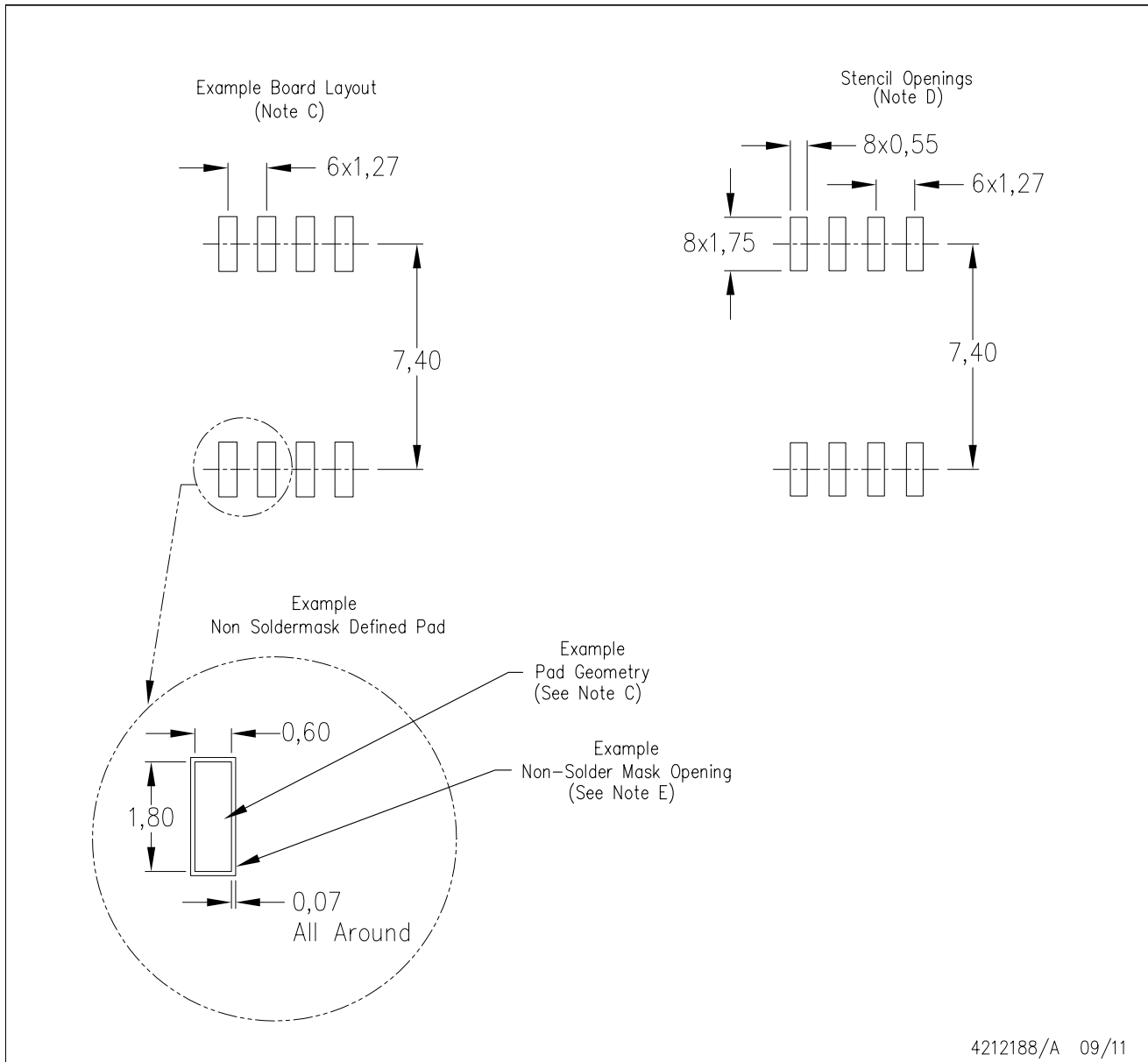
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

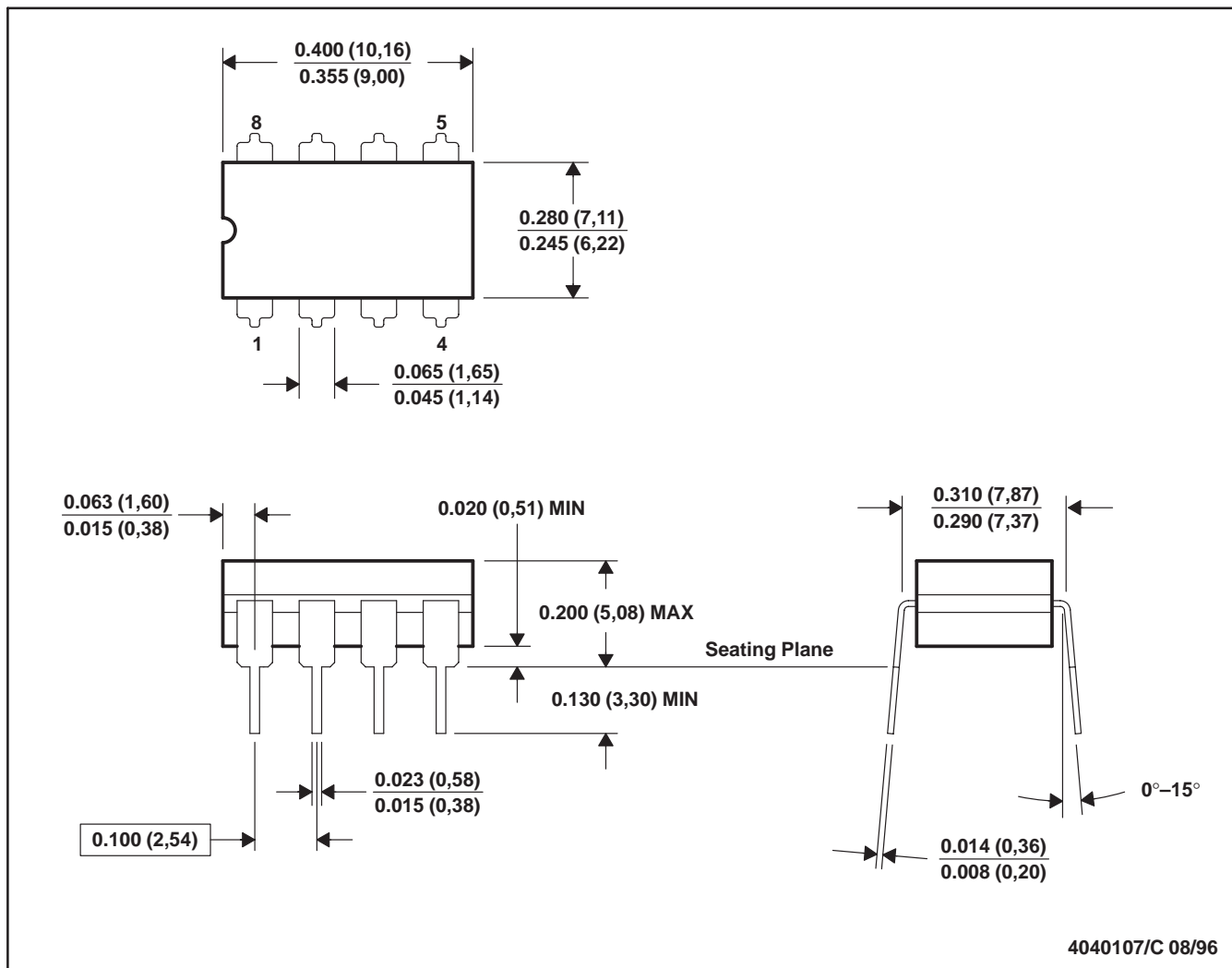
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

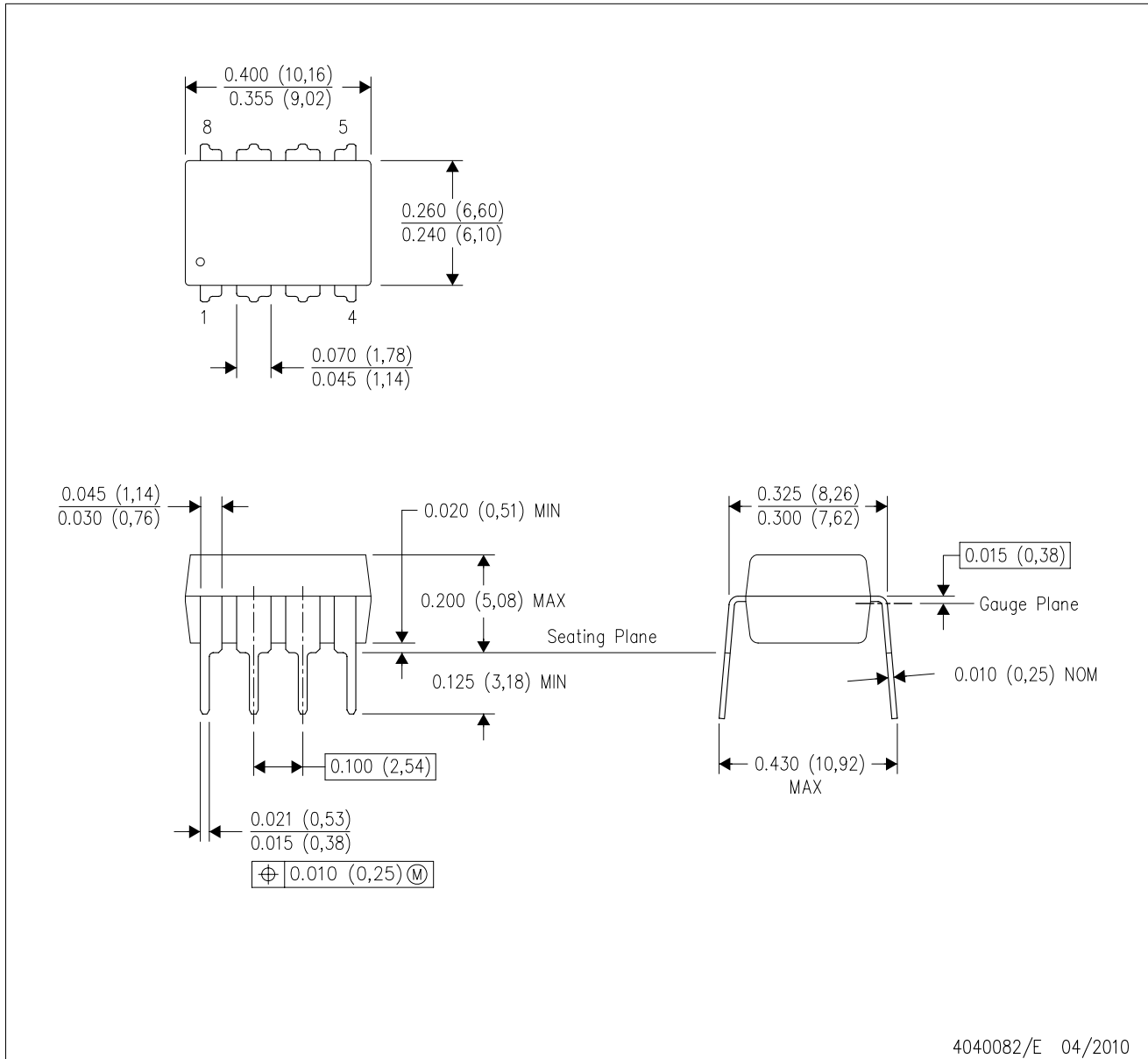
CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

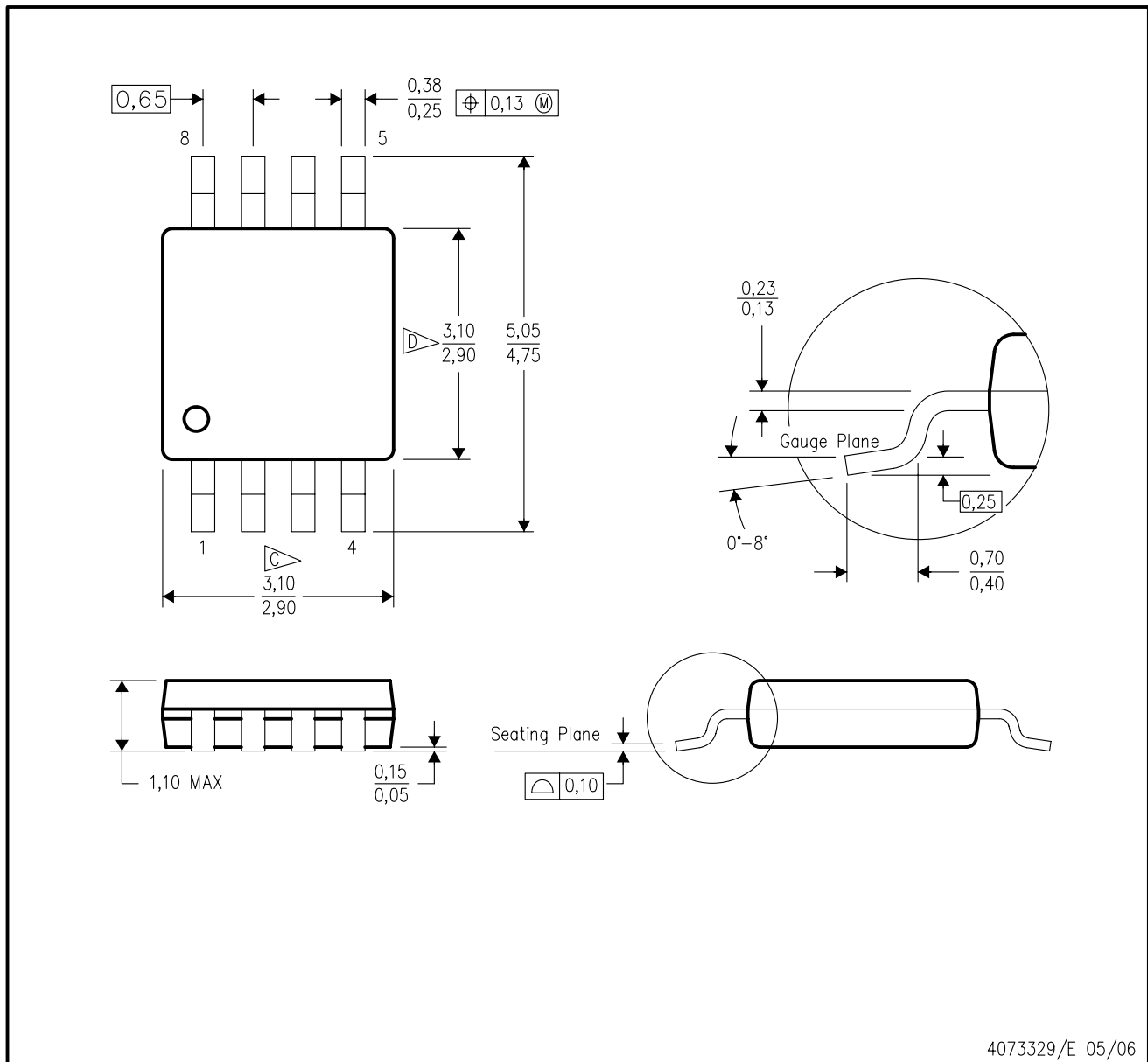
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



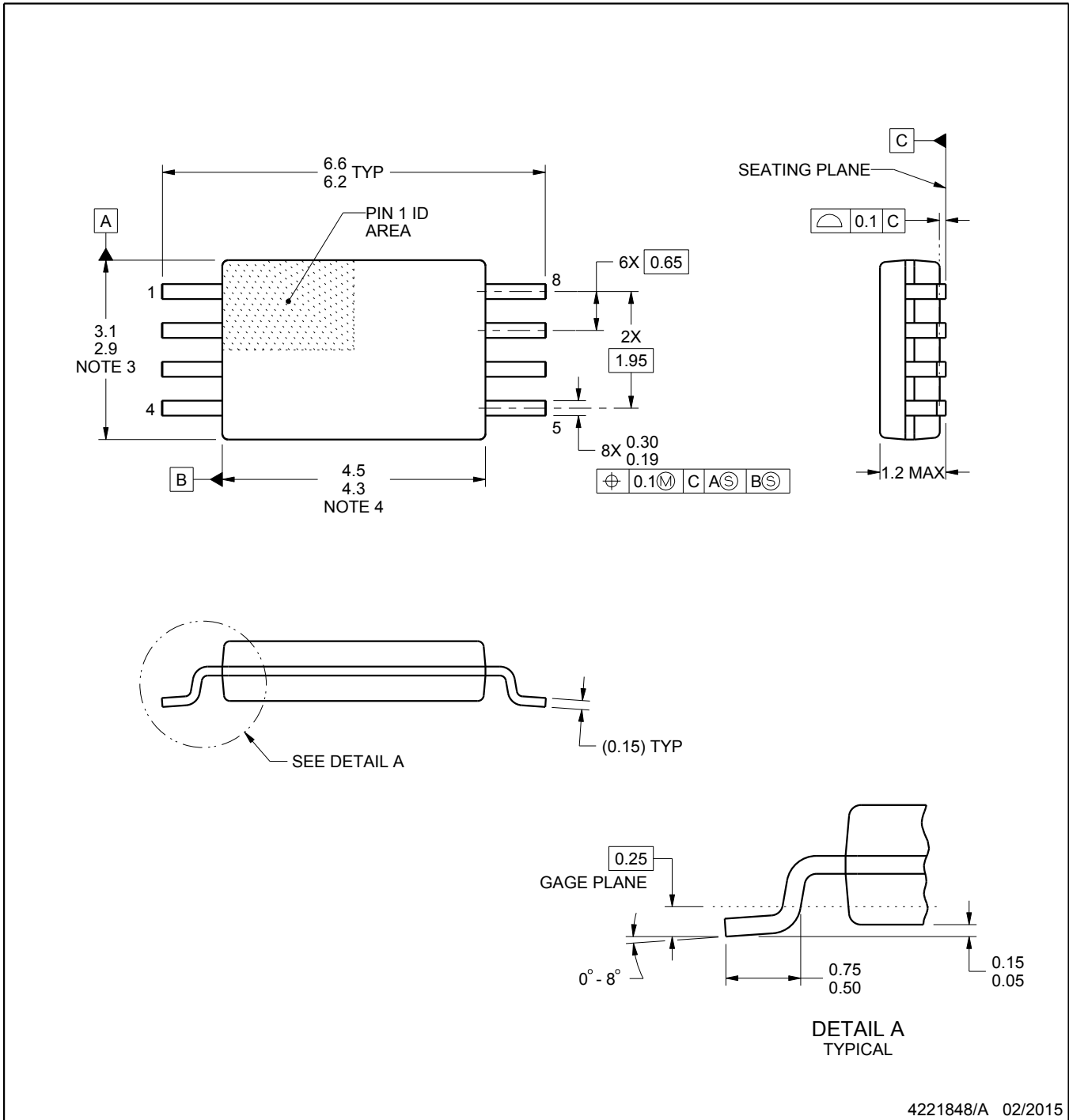
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

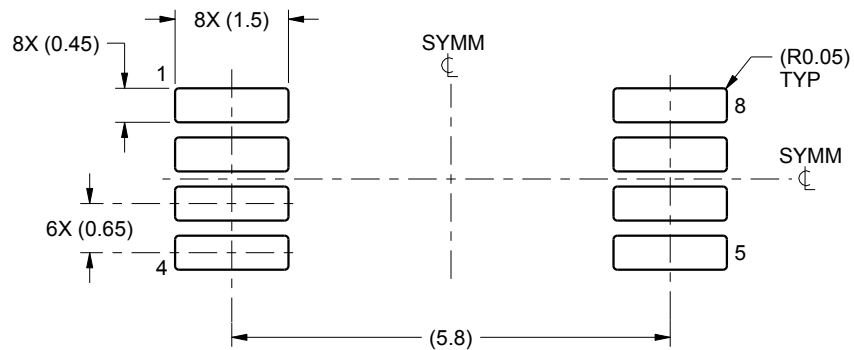
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

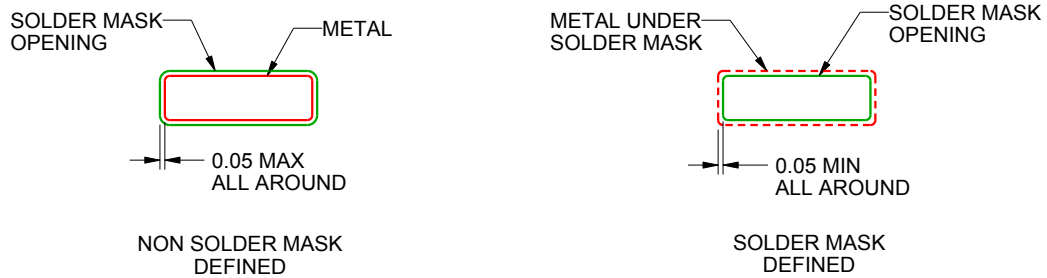
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

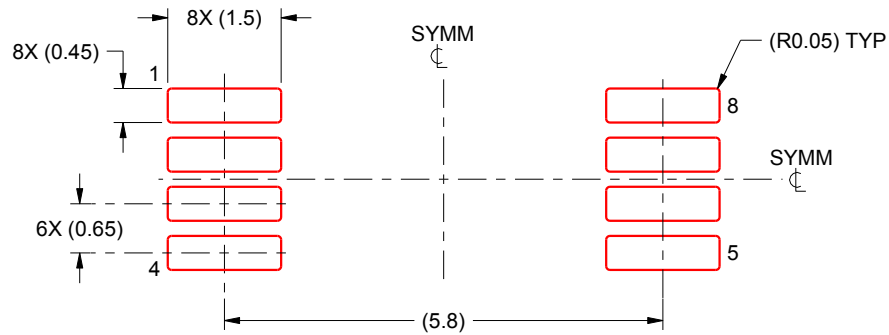
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



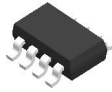
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

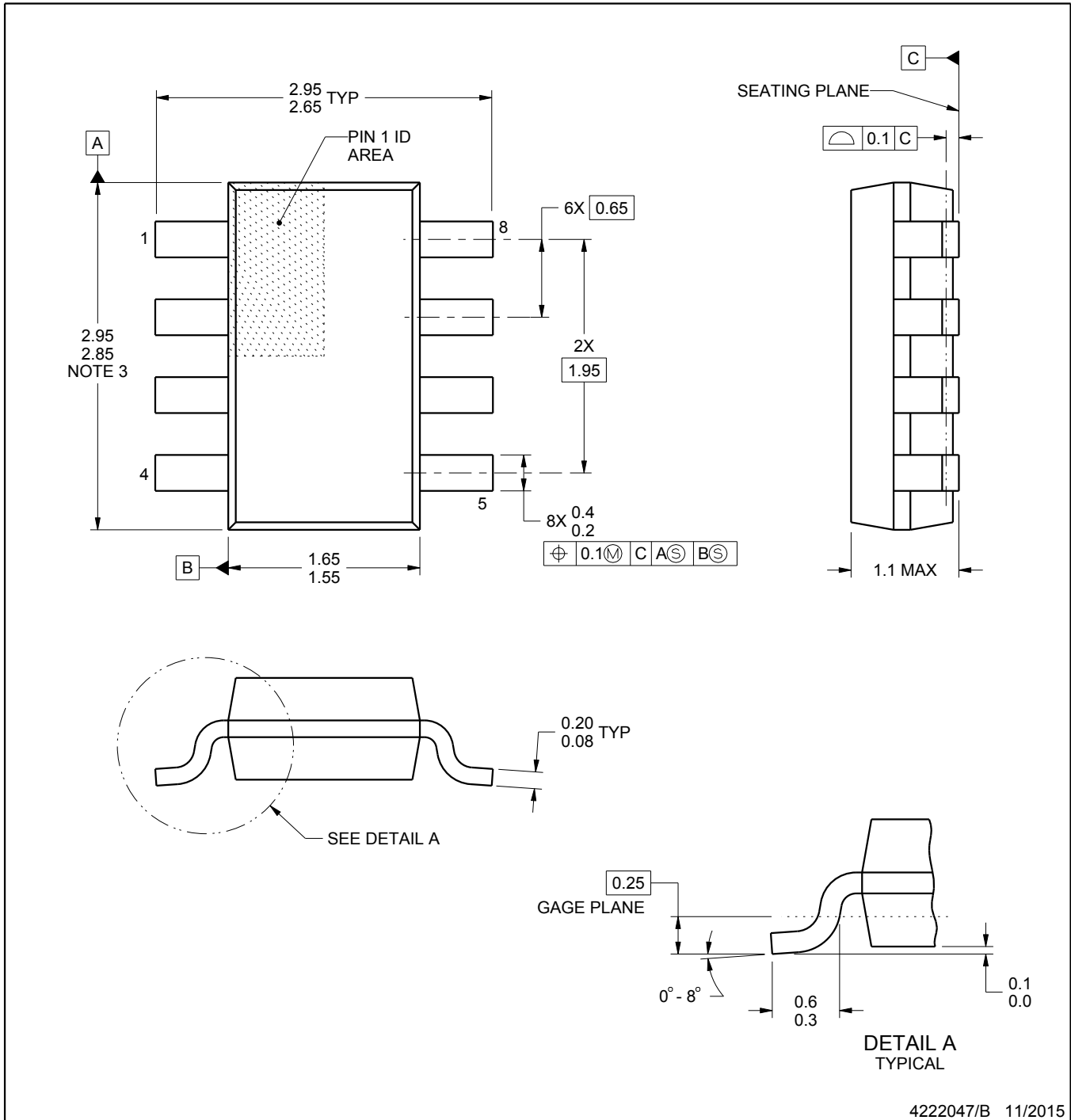
DDF0008A



PACKAGE OUTLINE

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

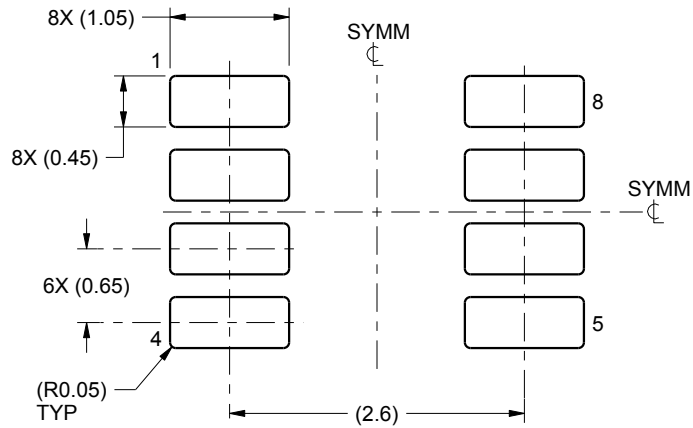
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

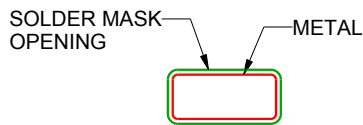
DDF0008A

SOT-23 - 1.1 mm max height

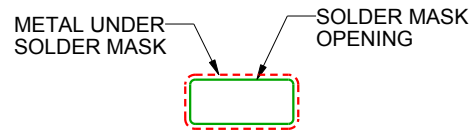
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

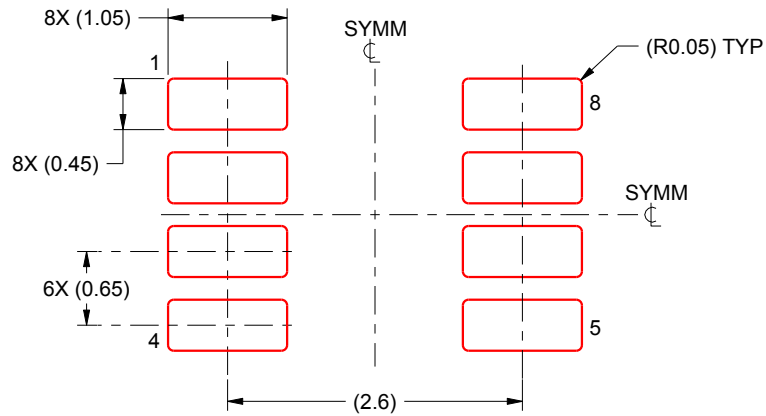
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

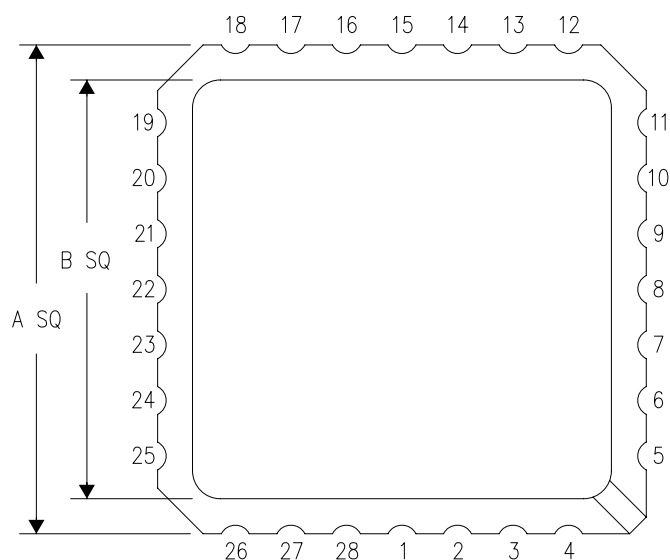
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

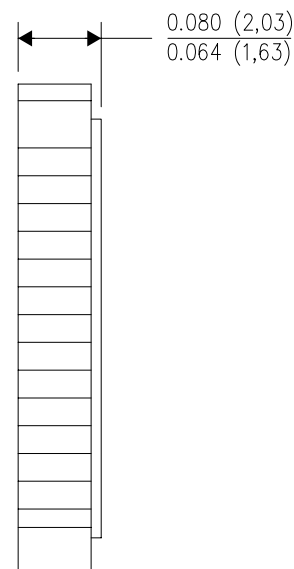
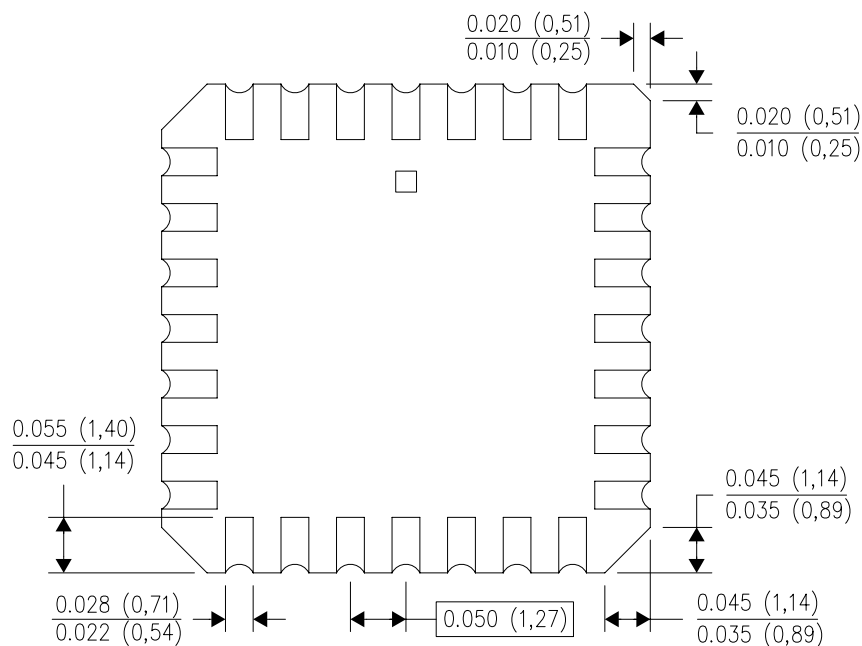
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

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