LM1084 5-A Low Dropout Positive Regulators

1 Features

- Available in 3.3-V, 5.0-V, and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 5 A
- Industrial Temperature Range −40°C to 125°C
- Line Regulation 0.015% (Typical)
- Load Regulation 0.1% (Typical)

2 Applications

- Post Regulator for Switching DC-DC Converter
- High-Efficiency Linear Regulators
- Battery Chargers

3 Description

The LM1084 is a regulator with a maximum dropout of 1.5 V at 5 A of load current. The device has the same pinout as TI's industry standard LM317.

Two resistors are required to set the output voltage of the adjustable output voltage version of the LM1084. Fixed output voltage versions integrate the adjust resistors.

The LM1084 circuit includes a zener trimmed bandgap reference, current limiting, and thermal shutdown.

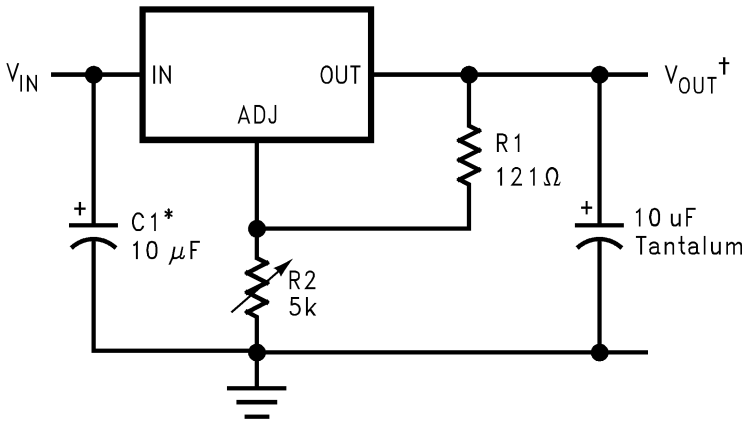
Refer to LM1085 for the 3A version, and the LM1086 for the 1.5A version.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM1084	TO-263 (3)	10.18 mm × 8.41 mm
	TO-220 (3)	14.986 mm × 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

†$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision F (March 2013) to Revision G **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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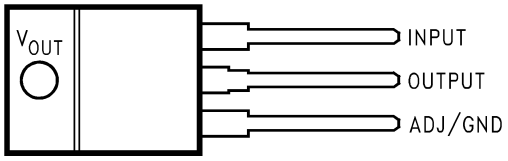
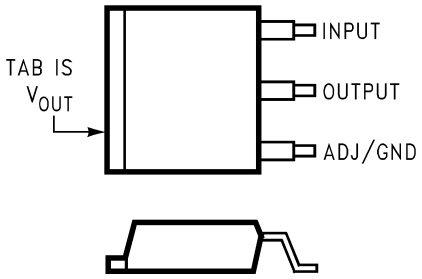
5 Pin Configuration and Functions

3-Pin
TO-220 Package
Top View



3-Pin
TO-263 Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADJ/GND	1	-	Adjust pin for the adjustable output voltage version. Ground pin for the fixed output voltage versions.
OUTPUT	2	O	Output voltage pin for the regulator.
INPUT	3	I	Input voltage pin for the regulator.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Maximum Input to Output Voltage Differential			
LM1084-ADJ		29	V
LM1084-3.3		27	V
LM1084-5.0		25	V
Power Dissipation(3)		Internally Limited	
Junction Temperature (T_J)(4)		150	°C
Lead Temperature		260, to 10 sec	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Power dissipation is kept in a safe range by current limiting circuitry. Refer to *Overload Recovery*.
(4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board. Refer to *Thermal Considerations*.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Junction Temperature Range (T_J)(2)			
Control Section	–40	125	°C
Output Section	–40	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the *Electrical Characteristics*.
(2) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board. Refer to *Thermal Considerations*.

6.4 Thermal Information

THERMAL METRIC(1)		LM1084 KTT 3 PINS	LM1084 NDE 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	22.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.6	15.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.0	4.1	
ψ_{JT}	Junction-to-top characterization parameter	9.8	2.1	
ψ_{JB}	Junction-to-board characterization parameter	22.0	4.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance: Control Section/Output Section	0.65/2.7	0.65/2.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Typicals and limits apply for T_J = 25°C unless specified otherwise.

	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{REF}	Reference Voltage	LM1084-ADJ, I_{OUT} = 10 mA, V_{IN} − V_{OUT} = 3 V, 10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5 V ≤ (V_{IN}−V_{OUT}) ≤ 25 V(3)	1.238	1.250	1.262	V
		LM1084-ADJ, I_{OUT} = 10 mA, V_{IN} − V_{OUT} = 3 V, 10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5 V ≤ (V_{IN}−V_{OUT}) ≤ 25 V(3), –40°C ≤ T_J ≤ 125°C	1.225	1.250	1.270	
V_{OUT}	Output Voltage(3)	LM1084-3.3, I_{OUT} = 0 mA, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 4.8 V ≤ V_{IN} ≤ 15 V	3.270	3.300	3.330	V
		LM1084-3.3, I_{OUT} = 0 mA, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 4.8 V ≤ V_{IN} ≤ 15 V , –40°C ≤ T_J ≤ 125°C	3.235	3.300	3.365	
		LM1084-5.0, I_{OUT} = 0 mA, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 6.5 V ≤ V_{IN} ≤ 20 V	4.950	5.000	5.050	V
		LM1084-5.0, I_{OUT} = 0 mA, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 6.5 V ≤ V_{IN} ≤ 20 V, –40°C ≤ T_J ≤ 125°C	4.900	5.000	5.100	
ΔV_{OUT}	Line Regulation(4)	LM1084-ADJ, I_{OUT} = 10 mA, 1.5 V ≤ (V_{IN} – V_{OUT}) ≤ 15 V		0.015%	0.2%	
		LM1084-ADJ, I_{OUT} = 10 mA, 1.5 V ≤ (V_{IN} – V_{OUT}) ≤ 15 V, –40°C ≤ T_J ≤ 125°C		0.035%	0.2%	
		LM1084-3.3, I_{OUT} = 0 mA, 4.8 V ≤ V_{IN} ≤ 15 V		0.5	6	mV
		LM1084-3.3, I_{OUT} = 0 mA, 4.8 V ≤ V_{IN} ≤ 15 V, –40°C ≤ T_J ≤ 125°C		1.0	6	
		LM1084-5.0, I_{OUT} = 0 mA, 6.5 V ≤ V_{IN} ≤ 20 V		0.5	10	mV
		LM1084-5.0, I_{OUT} = 0 mA, 6.5 V ≤ V_{IN} ≤ 20 V, –40°C ≤ T_J ≤ 125°C		1.0	10	
ΔV_{OUT}	Load Regulation(4)	LM1084-ADJ, (V_{IN} – V_{OUT}) = 3 V, 10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		0.1 %	0.3%	
		LM1084-ADJ, (V_{IN} – V_{OUT}) = 3 V, 10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, –40°C ≤ T_J ≤ 125°C		0.2%	0.4%	
		LM1084-3.3, V_{IN} = 5 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		3	15	mV
		LM1084-3.3, V_{IN} = 5 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, –40°C ≤ T_J ≤ 125°C		7	20	
		LM1084-5.0, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$		5	20	mV
		LM1084-5.0, V_{IN} = 8 V, 0 ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, –40°C ≤ T_J ≤ 125°C		10	35	
	Dropout Voltage(5)	LM1084-ADJ, 3.3, 5, 12, ΔV_{REF}, ΔV_{OUT} = 1%, I_{OUT} = 5A, –40°C ≤ T_J ≤ 125°C		1.3	1.5	V
I_{LIMIT}	Current Limit	LM1084-ADJ, V_{IN}− V_{OUT} = 5 V, –40°C ≤ T_J ≤ 125°C	5.5	8.0		A
		LM1084-ADJ, V_{IN}− V_{OUT} = 25 V, –40°C ≤ T_J ≤ 125°C	0.3	0.6		
		LM1084-3.3, V_{IN} = 8 V, –40°C ≤ T_J ≤ 125°C	5.5	8.0		A
		LM1084-5.0, V_{IN} = 10 V, –40°C ≤ T_J ≤ 125°C	5.5	8.0		A
	Minimum Load Current(6)	LM1084-ADJ, V_{IN} − V_{OUT} = 25 V		5	10.0	mA
	Quiescent Current	LM1084-3.3, V_{IN} = 18 V		5.0	10.0	mA
		LM1084-5.0, V_{IN} ≤ 20 V		5.0	10.0	mA
	Thermal Regulation	T_A = 25°C, 30 ms Pulse		0.003	0.015	%/W

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) $I_{FULLLOAD}$ is defined in the current limit curves. The $I_{FULLLOAD}$ Curve defines the current limit as a function of input-to-output voltage. Note that 30W power dissipation for the LM1084 is only achievable over a limited range of input-to-output voltage.
(4) Load and line regulation are measured at constant junction temperature, and are ensured up to the maximum power dissipation of 30W. Power dissipation is determined by the input/output differential and the output current. ensured maximum power dissipation will not be available over the full input/output range.
(5) Dropout voltage is specified over the full output current range of the device.
(6) The minimum output current required to maintain regulation.

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Electrical Characteristics (continued)

Typicals and limits apply for T_J = 25°C unless specified otherwise.

	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
	Ripple Rejection	f_{RIPPLE} = 120 Hz, = C_{OUT} = 25 µF Tantalum, I_{OUT} = 5A				dB
		LM1084-ADJ, C_{ADJ}, = 25 µF, (V_{IN} − V_O) = 3 V, –40°C ≤ T_J ≤ 125°C	60	75		
		LM1084-3.3, V_{IN} = 6.3 V, –40°C ≤ T_J ≤ 125°C	60	72		dB
		LM1084-5.0, V_{IN} = 8 V, –40°C ≤ T_J ≤ 125°C	60	68		dB
	Adjust Pin Current	LM1084		55		µA
		LM1084, –40°C ≤ T_J ≤ 125°C			120	
	Adjust Pin Current Change	10 mA ≤ I_{OUT} ≤ $I_{FULL\ LOAD}$, 1.5 V ≤ V_{IN} − V_{OUT} ≤ 25 V, –40°C ≤ T_J ≤ 125°C		0.2	5	µA
	Temperature Stability	–40°C ≤ T_J ≤ 125°C		0.5%		
	Long Term Stability	T_A =125°C, 1000 Hrs		0.3%	1.0%	
	RMS Output Noise (% of V_{OUT})	10 Hz ≤ f≤ 10 kHz		0.003%		

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6.6 Typical Characteristics

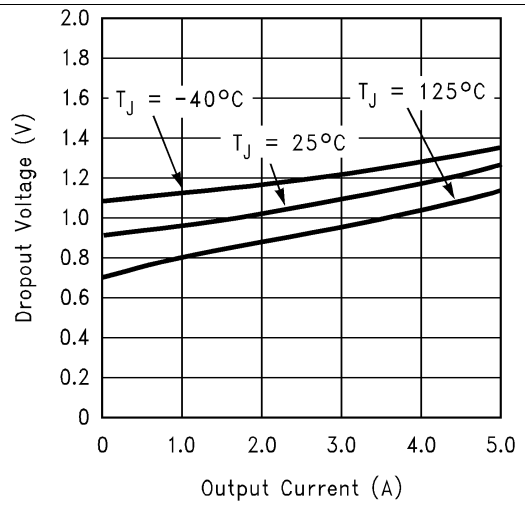

Figure 1. Dropout Voltage (V_{IN}–V_{OUT})

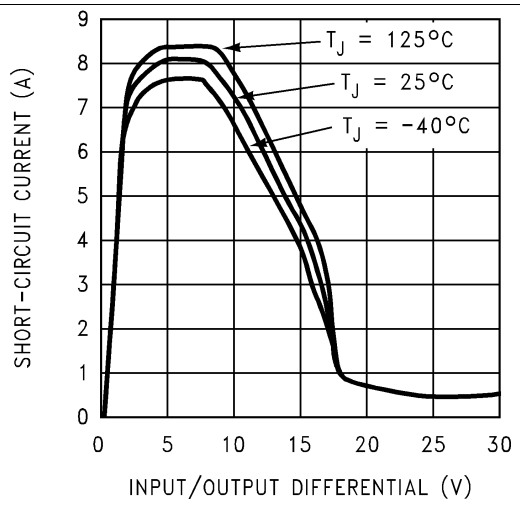

Figure 2. Short-Circuit Current

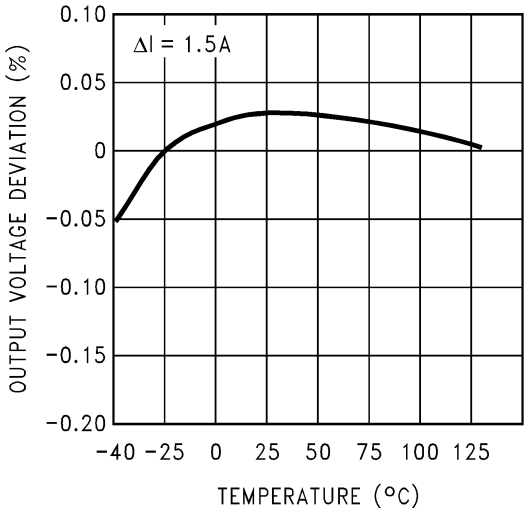

Figure 3. Load Regulation

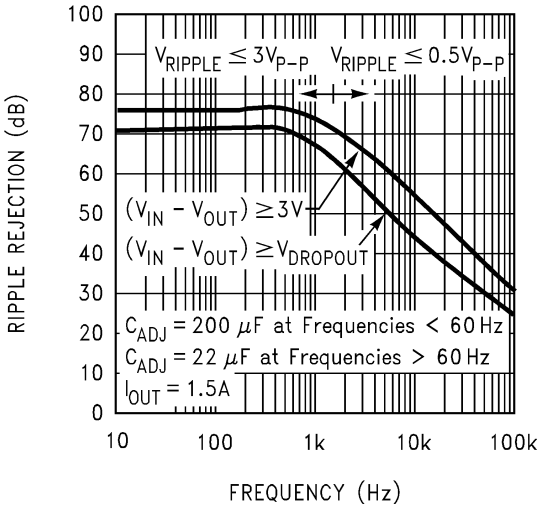

Figure 4. LM1084-ADJ Ripple Rejection

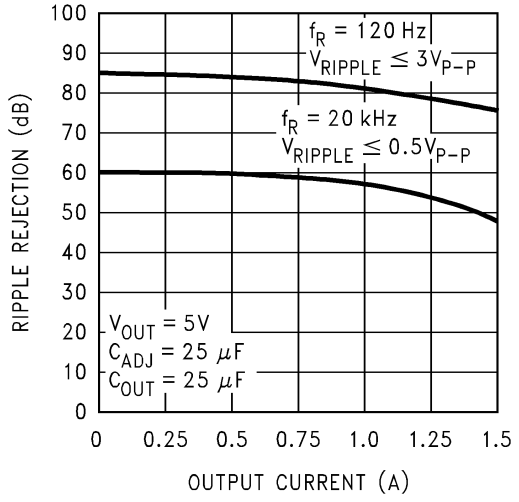

Figure 5. LM1084-ADJ Ripple Rejection vs Current

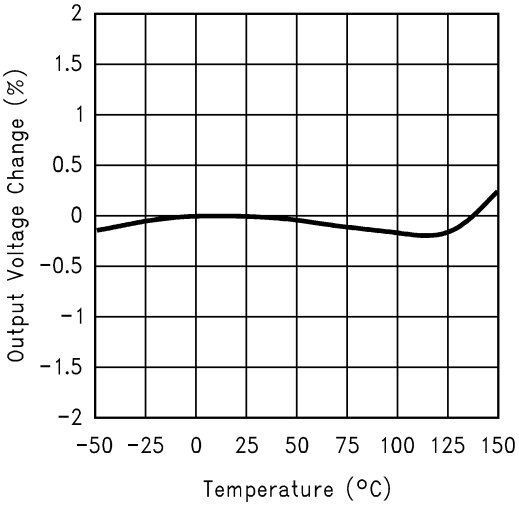

Figure 6. Temperature Stability

Typical Characteristics (continued)

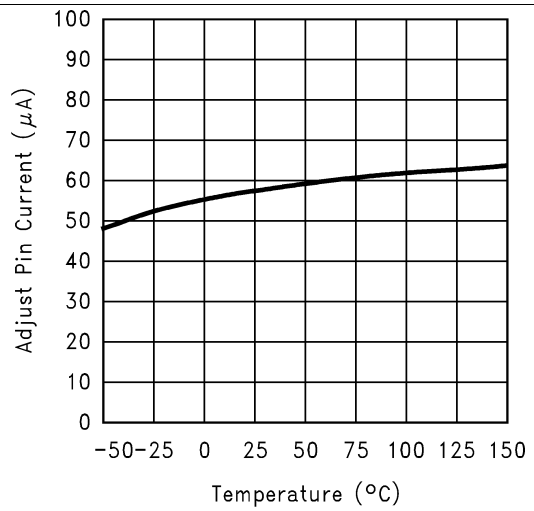

Figure 7. Adjust Pin Current

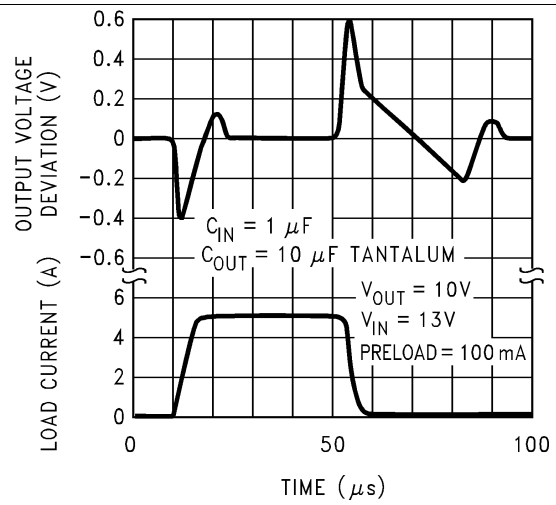

Figure 8. LM1084-ADJ Load Transient Response

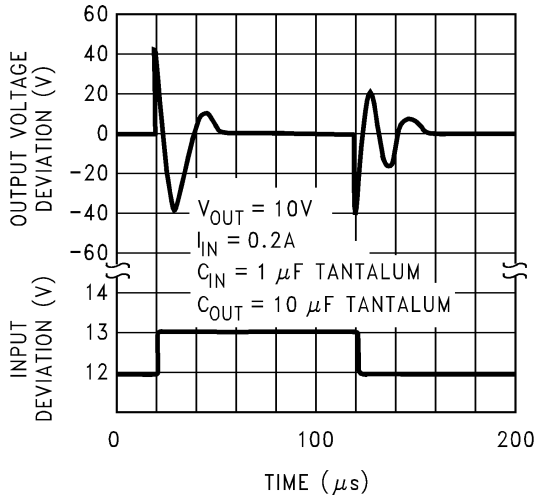

Figure 9. LM1084-ADJ LineTransient Response

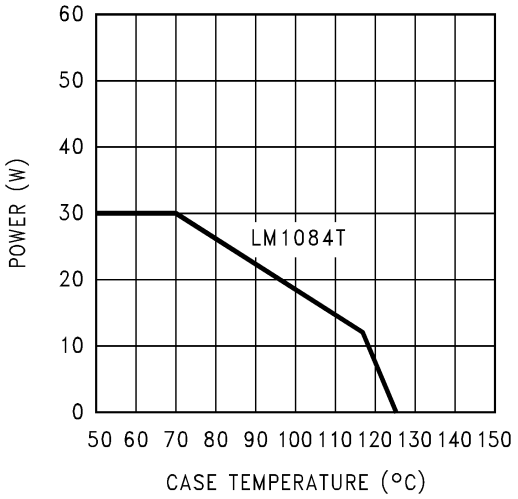

Figure 10. Maximum Power Dissipation

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Typical Applications (continued)

8.2.9 Ripple Rejection Enhancement

A very simple ripple rejection circuit is shown in Figure 24 using the LM1084-ADJ. The capacitor C1 smooths out the ripple on the output by cleaning up the feedback path and preventing excess noise from feeding back into the regulator. Please remember X_{C1} should be approximately equal to R1 at the ripple frequency.

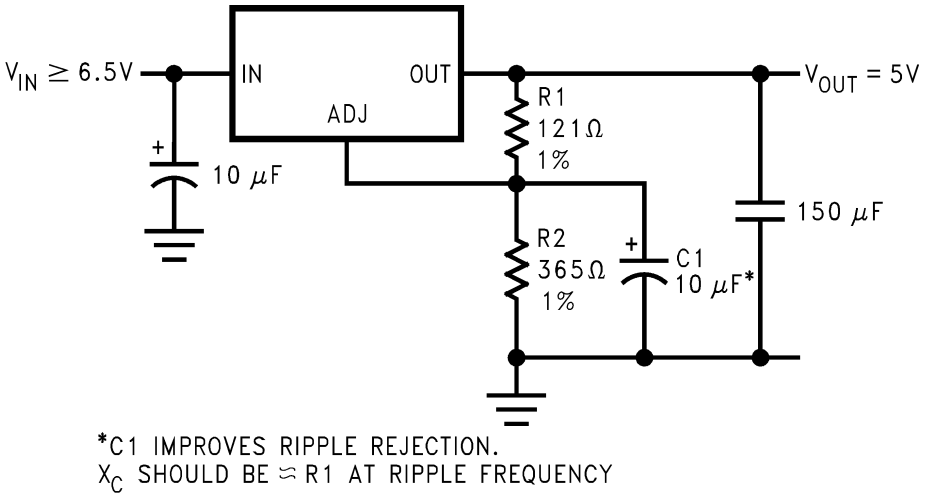

Figure 24. Ripple Rejection Enhancement

8.2.10 Automatic Light Control

A common street light control or automatic light control circuit is designed in Figure 25 based on the LM1084-ADJ. The photo transistor conducts in the presence of light and grounds the ADJ pin preventing the lamp from turning on. However, in the absence of light, the LM1084 regulates the voltage to 1.25V between OUT and ADJ, ensuring the lamp remains on.

Figure 25. Automatic Light Control

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Typical Applications (continued)

8.2.11 Generating Negative Supply Voltage

A quick inverting output rail or negative output rail is shown in Figure 26 using the LM1084 fixed output part. By tying the output to GND, the GND node is at a relatively more negative potential than the output. This is then interfaced to the negative application such as an operational amplifier or any other rail needing negative voltage.

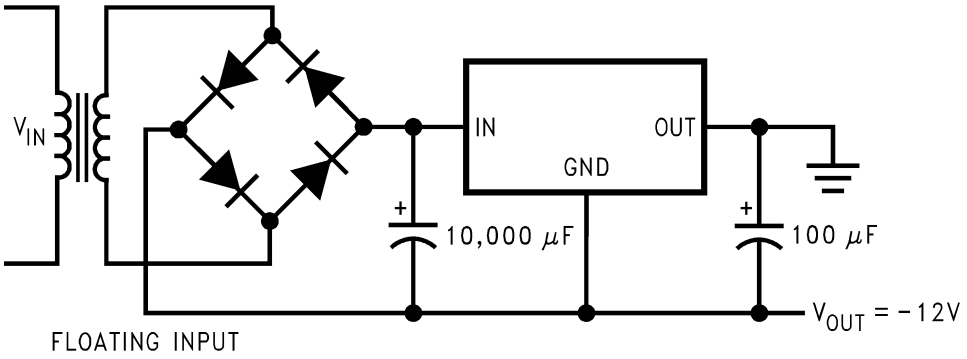

Figure 26. Generating Negative Supply Voltage

8.2.12 Remote Sensing

Remote sensing is a method of compensating the output voltage to a very precise degree by sensing the output and feeding it back through the feedback. The circuit implementing this is shown in Figure 27 using the LM1084-ADJ. The output of the regulator is fed into a voltage follower to avoid any loading effects and the output of the op-amp is injected into the top of the feedback resistor network. This has the effect of modulating the voltage to a precise degree without additional loading on the output.

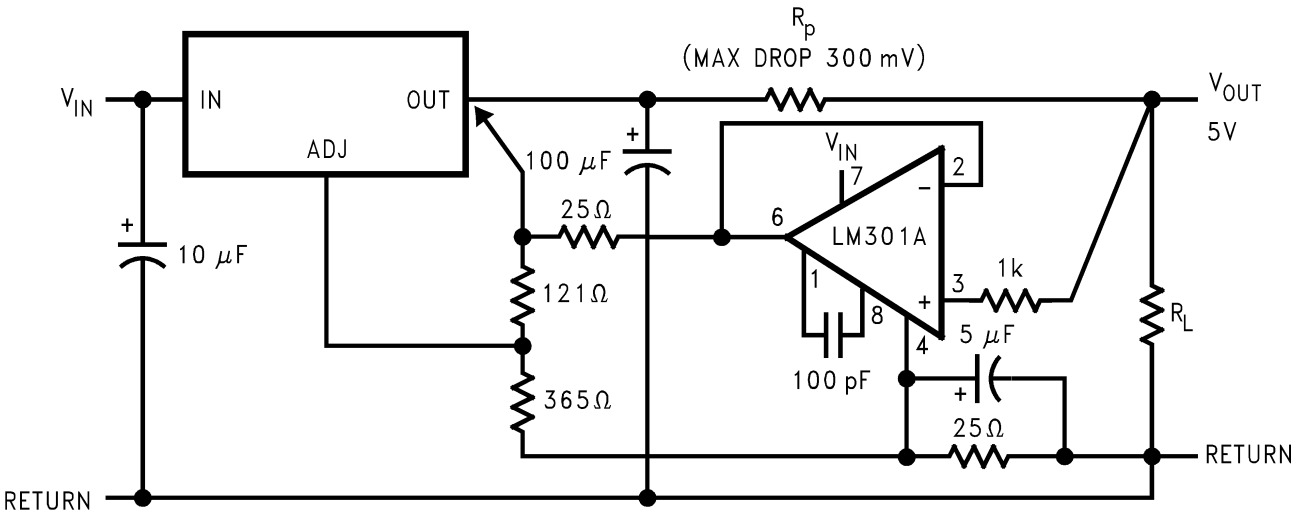

Figure 27. Remote Sensing

9 Power Supply Recommendations

The linear regulator input supply should be well regulated and kept at a voltage level such that the maximum input to output voltage differential allowed by the device is not exceeded. The minimum dropout voltage (V_{IN} – V_{OUT}) should be met with extra headroom when possible in order to keep the output well regulated. A 10 µF or higher capacitor should be placed at the input to bypass noise.

10 Layout

10.1 Layout Guidelines

For the best overall performance, some layout guidelines should be followed. Place all circuit components on the same side of the circuit board and as near as practical to the respective linear regulator pins. Traces should be kept short and wide to reduce the amount of parasitic elements into the system. The actual width and thickness of traces will depend on the current carrying capability and heat dissipation required by the end system. An array of plated vias can be placed on the pad area underneath the TAB to conduct heat to any inner plane areas or to a bottom-side copper plane.

10.2 Layout Example

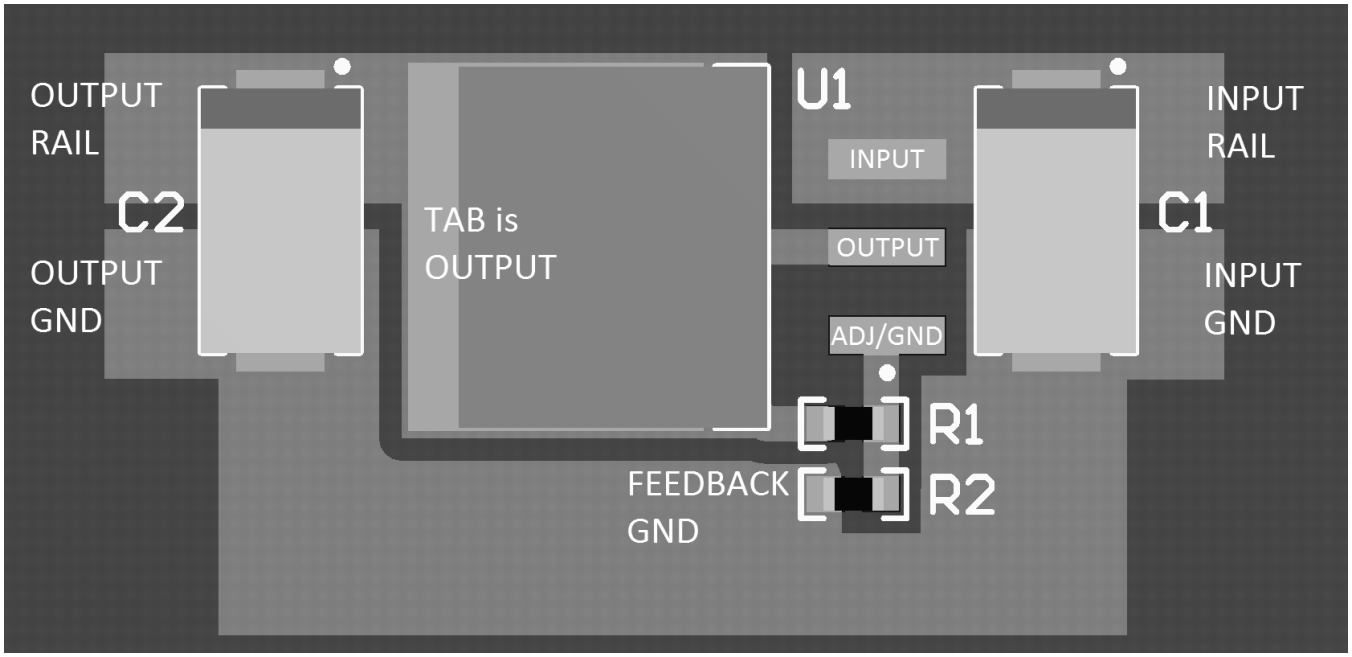

Figure 28. Layout Example

10.3 Thermal Considerations

ICs heats up when in operation, and power consumption is one factor in how hot it gets. The other factor is how well the heat is dissipated. Heat dissipation is predictable by knowing the thermal resistance between the IC and ambient (θ_{JA}). Thermal resistance has units of temperature per power (C/W). The higher the thermal resistance, the hotter the IC.

The LM1084 specifies the thermal resistance for each package as junction to case (θ_{JC}). In order to get the total resistance to ambient (θ_{JA}), two other thermal resistance must be added, one for case to heat-sink (θ_{CH}) and one for heatsink to ambient (θ_{HA}). The junction temperature can be predicted as follows:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CH} + \theta_{HA}) = T_A + P_D \theta_{JA} \quad (3)$$

T_J is junction temperature, T_A is ambient temperature, and P_D is the power consumption of the device. Device power consumption is calculated as follows:

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Thermal Considerations (continued)

$$I_{IN} = I_L + I_G \quad (4)$$

$$P_D = (V_{IN} - V_{OUT})\, I_L + V_{IN} I_G \quad (5)$$

Figure 29 shows the voltages and currents which are present in the circuit.

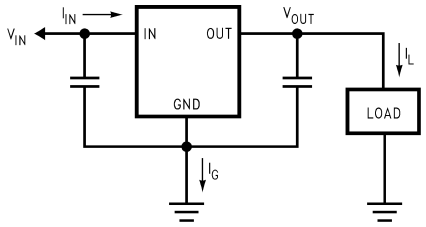

Figure 29. Power Dissipation Diagram

Once the devices power is determined, the maximum allowable ($\theta_{JA\ (max)}$) is calculated as:

$$\theta_{JA\ (max)} = T_{R(max)}/P_D = T_{J(max)} - T_{A(max)}/P_D \quad (6)$$

The LM1084 has different temperature specifications for two different sections of the IC: the control section and the output section. The *Thermal Information* table shows the junction to case thermal resistances for each of these sections, while the maximum junction temperatures ($T_{J(max)}$) for each section is listed in the *Absolute Maximum Ratings* section of the datasheet. $T_{J(max)}$ is 125°C for the control section, while $T_{J(max)}$ is 150°C for the output section.

$\theta_{JA\ (max)}$ should be calculated separately for each section as follows:

$$\theta_{JA}\ (\text{max, CONTROL SECTION}) = (125°C - T_{A(max)})/P_D \quad (7)$$

$$\theta_{JA}\ (\text{max, OUTPUT SECTION}) = (150°C - T_{A(max)})/P_D \quad (8)$$

The required heat sink is determined by calculating its required thermal resistance ($\theta_{HA\ (max)}$).

$$\theta_{HA\ (max)} = \theta_{JA\ (max)} - (\theta_{JC} + \theta_{CH}) \quad (9)$$

($\theta_{HA\ (max)}$) should also be calculated twice as follows:

$$(\theta_{HA\ (max)}) = \theta_{JA}\ (\text{max, CONTROL SECTION}) - (\theta_{JC}\ (\text{CONTROL SECTION}) + \theta_{CH}) \quad (10)$$

$$(\theta_{HA\ (max)}) = \theta_{JA}(\text{max, OUTPUT SECTION}) - (\theta_{JC}\ (\text{OUTPUT SECTION}) + \theta_{CH}) \quad (11)$$

If thermal compound is used, θ_{CH} can be estimated at 0.2 C/W. If the case is soldered to the heat sink, then a θ_{CH} can be estimated as 0 C/W.

After, $\theta_{HA\ (max)}$ is calculated for each section, choose the lower of the two $\theta_{HA\ (max)}$ values to determine the appropriate heat sink.

If PC board copper is going to be used as a heat sink, then Figure 30 can be used to determine the appropriate area (size) of copper foil required.

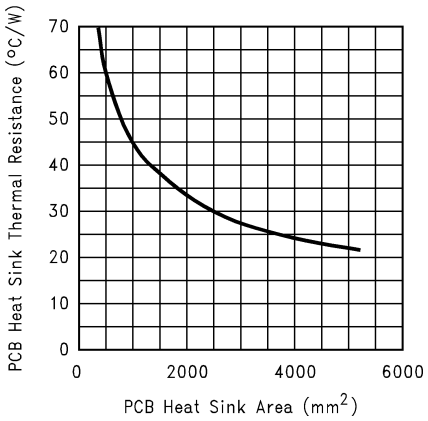

Figure 30. Heat Sink Thermal Resistance vs Area

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11 Device and Documentation Support

11.1 Trademarks

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11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1084IS-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM1084 IS-3.3	Samples
LM1084IS-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM1084 IS-5.0	Samples
LM1084IS-ADJ	NRND	DDPAK/ TO-263	KTT	3	45	TBD	Call TI	Call TI	-40 to 125	LM1084 IS-ADJ	
LM1084IS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM1084 IS-ADJ	Samples
LM1084ISX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM1084 IS-3.3	Samples
LM1084ISX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM1084 IS-5.0	Samples
LM1084ISX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM1084 IS-ADJ	Samples
LM1084IT-3.3/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM1084 IT-3.3	Samples
LM1084IT-5.0/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM1084 IT-5.0	Samples
LM1084IT-ADJ/NOPB	ACTIVE	TO-220	NDE	3	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM1084 IT-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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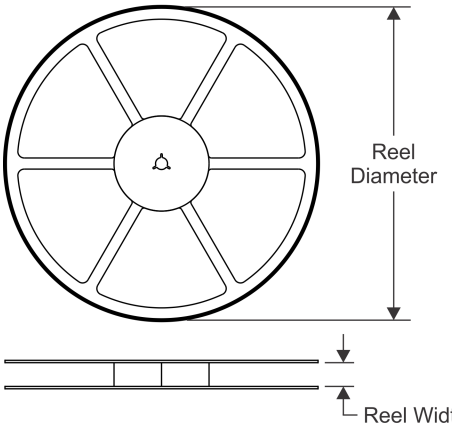
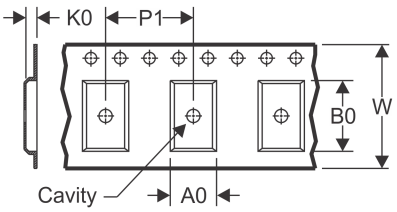
TAPE AND REEL INFORMATION

REEL DIMENSIONS

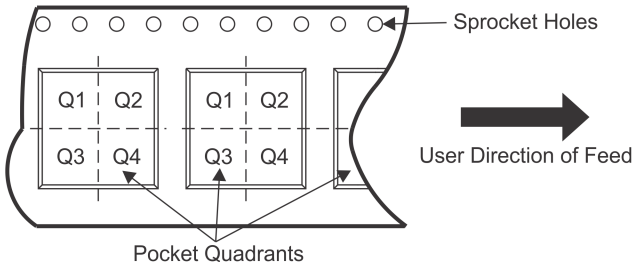


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

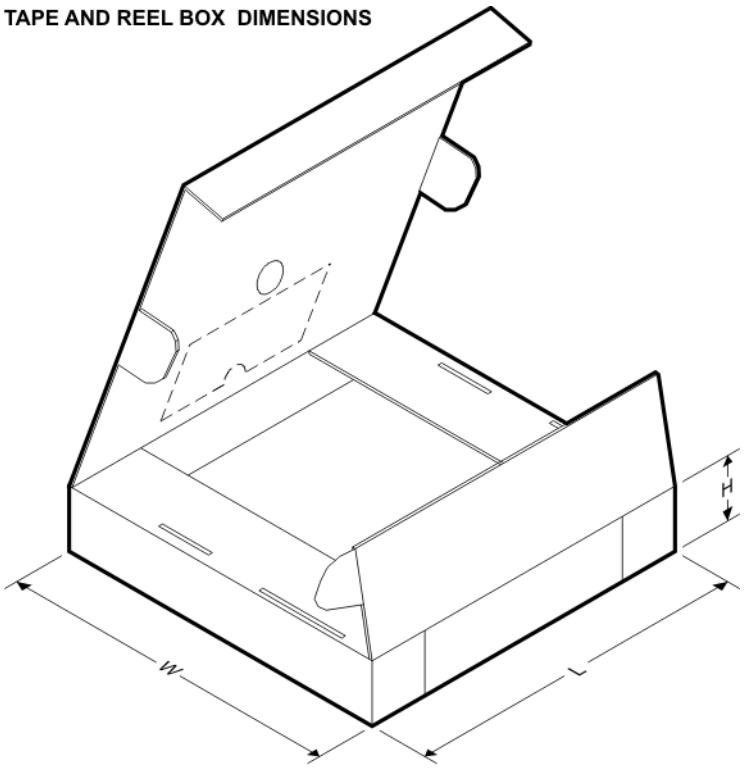
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1084ISX-3.3/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1084ISX-5.0/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM1084ISX-ADJ/NOPB	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

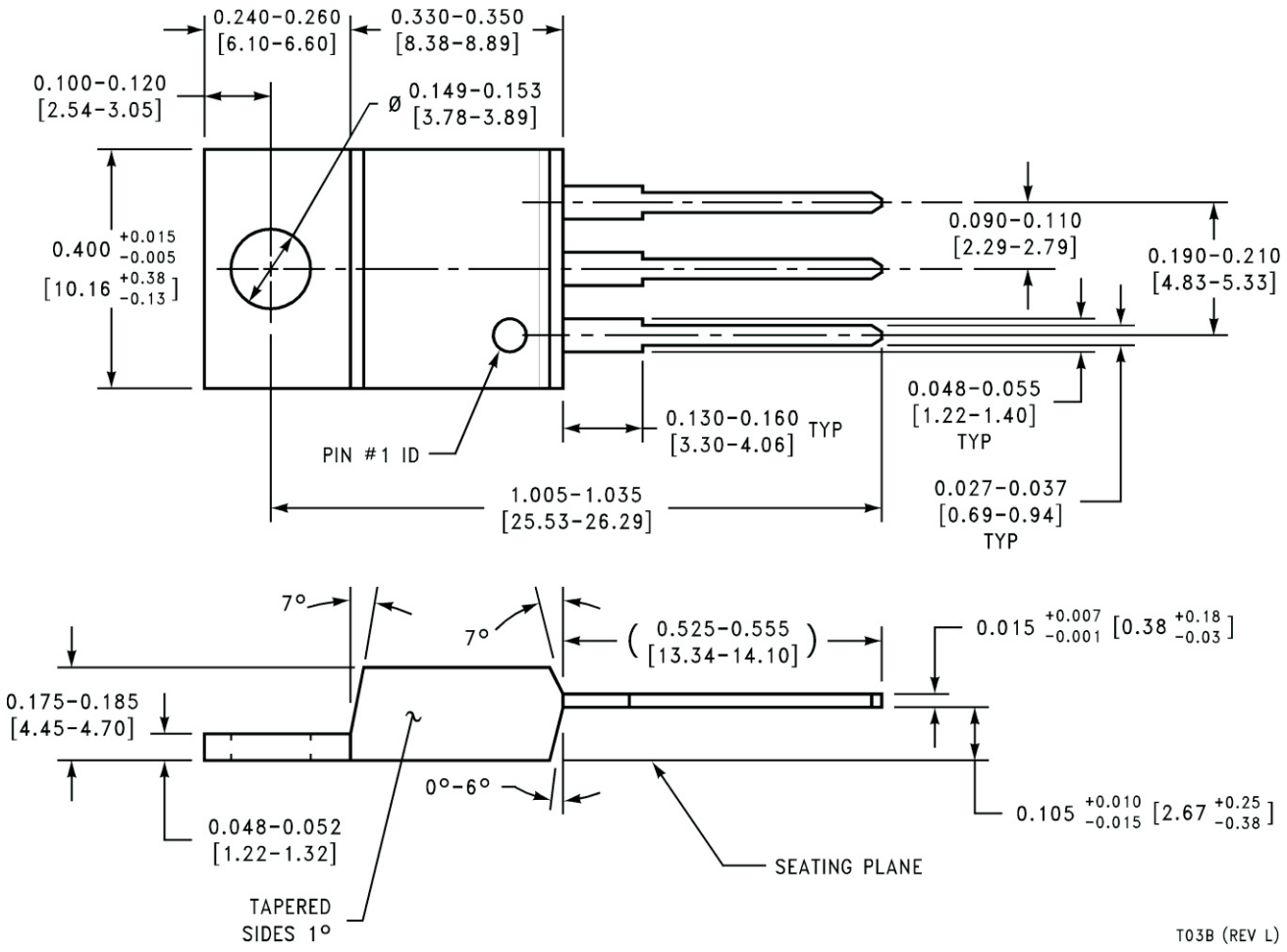
TAPE AND REEL BOX DIMENSIONS



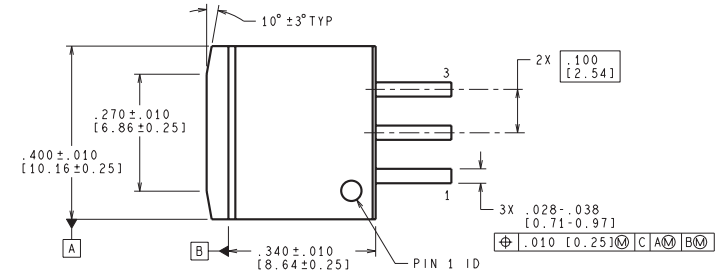
*All dimensions are nominal

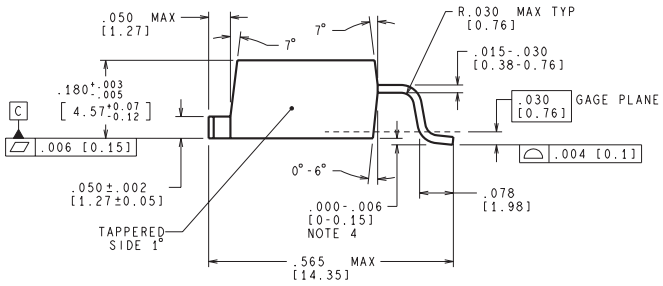
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1084ISX-3.3/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1084ISX-5.0/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0
LM1084ISX-ADJ/NOPB	DDPAK/TO-263	KTT	3	500	367.0	367.0	45.0

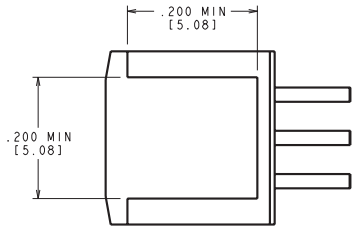
NDE0003B


0.240-0.260
[6.10-6.60]
0.330-0.350
[8.38-8.89]
0.100-0.120
[2.54-3.05]
Ø 0.149-0.153
[3.78-3.89]
0.400 +0.015 -0.005
[10.16 +0.38 -0.13]
0.090-0.110
[2.29-2.79]
0.190-0.210
[4.83-5.33]
PIN #1 ID
0.130-0.160 TYP
[3.30-4.06]
0.048-0.055
[1.22-1.40]
TYP
1.005-1.035
[25.53-26.29]
0.027-0.037
[0.69-0.94]
TYP
7°
7°
(0.525-0.555
[13.34-14.10])
0.015 +0.007 -0.001 [0.38 +0.18 -0.03]
0.175-0.185
[4.45-4.70]
0°-6°
0.105 +0.010 -0.015 [2.67 +0.25 -0.38]
0.048-0.052
[1.22-1.32]
SEATING PLANE
TAPERED
SIDES 1°
T03B (REV L)

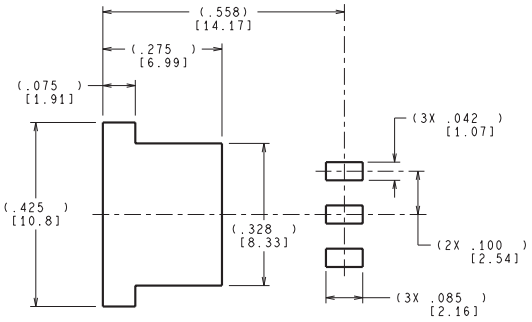
KTT0003B







BOTTOM SIDE OF PACKAGE



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