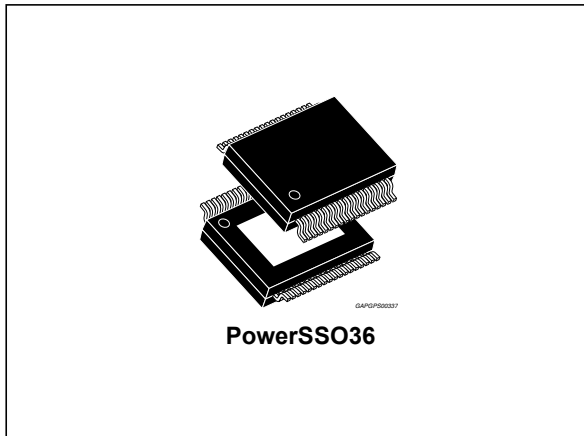


## Octal low side driver or quad low side plus quad high side driver

Data brief



### Features

- Eight integrated PowerMOS configurable as:
  - 8 low side ON-OFF with  $R_{ON(max)} = 0.3 \Omega$  @  $T_j = 175 \text{ }^\circ\text{C}$
  - High/low side PWM with  $R_{ON(max)} = 0.6 \Omega$  @  $T_j = 175 \text{ }^\circ\text{C}$  and 4 Low side with  $R_{ON(max)} = 0.3 \Omega$  @  $T_j = 175 \text{ }^\circ\text{C}$
- Operating battery supply voltage 5 V to 18 V
- Operating  $V_{dd}$  supply voltage 4.75 V to 5.25 V
- Logic inputs TTL/CMOS-compatible
- Output voltage clamping 37 V typ. in low-side configuration
- SPI interface for outputs control and for diagnosis data communication
- Additional PWM inputs for 8 outputs
- Over temperature protection
- Open load, short to GND, short to VB
- Overcurrent diagnostics in latched or unlatched mode for each channel
- Controlled SR for improved EMC behavior

### Description

The L9301 is a SPI (Serial Peripheral Interface) controlled octal channel with 4 high/low and 4 low side drivers with the possibility to use four integrated PowerMOS as recirculation diodes for PWM load driving.

L9301 contains 12 PowerMOS: 4 configurable High/Low side drivers with  $R_{ONmax} = 0.6 \Omega$  (DRN1-4, SRC1-4), 4 low side drivers with  $R_{ONmax} = 0.6 \Omega$  (OUT1-4) and 4 low side drivers with  $R_{ONmax} = 0.3 \Omega$  (OUT5-8).

The power DRN/SRC1-4 and OUT1-4 can be connected in parallel outside the device in order to get 4 low-side drivers with  $R_{ONmax} = 0.3 \Omega$ : DRN1//DRN2, DRN3//DRN4, OUT1//OUT2, OUT3//OUT4.

In this way there are a total of 8 LS channels for ON-OFF mode with  $R_{ONmax} = 0.3 \Omega$ .

There is also the possibility to connect the OUT1-4 and OUT5-8 in order to drive in PWM mode a load connected to VB or GND without the necessity of a freewheeling diode. In this case the  $R_{ONmax} = 0.6 \Omega$ .

The above configuration can be driven by parallel input or SPI command.

Through the SPI it is possible to configure the device parameters like configuration, Slew-rate, Overcurrent threshold, to send the drivers commands and to read back the diagnosis results.

**Table 1. Device summary**

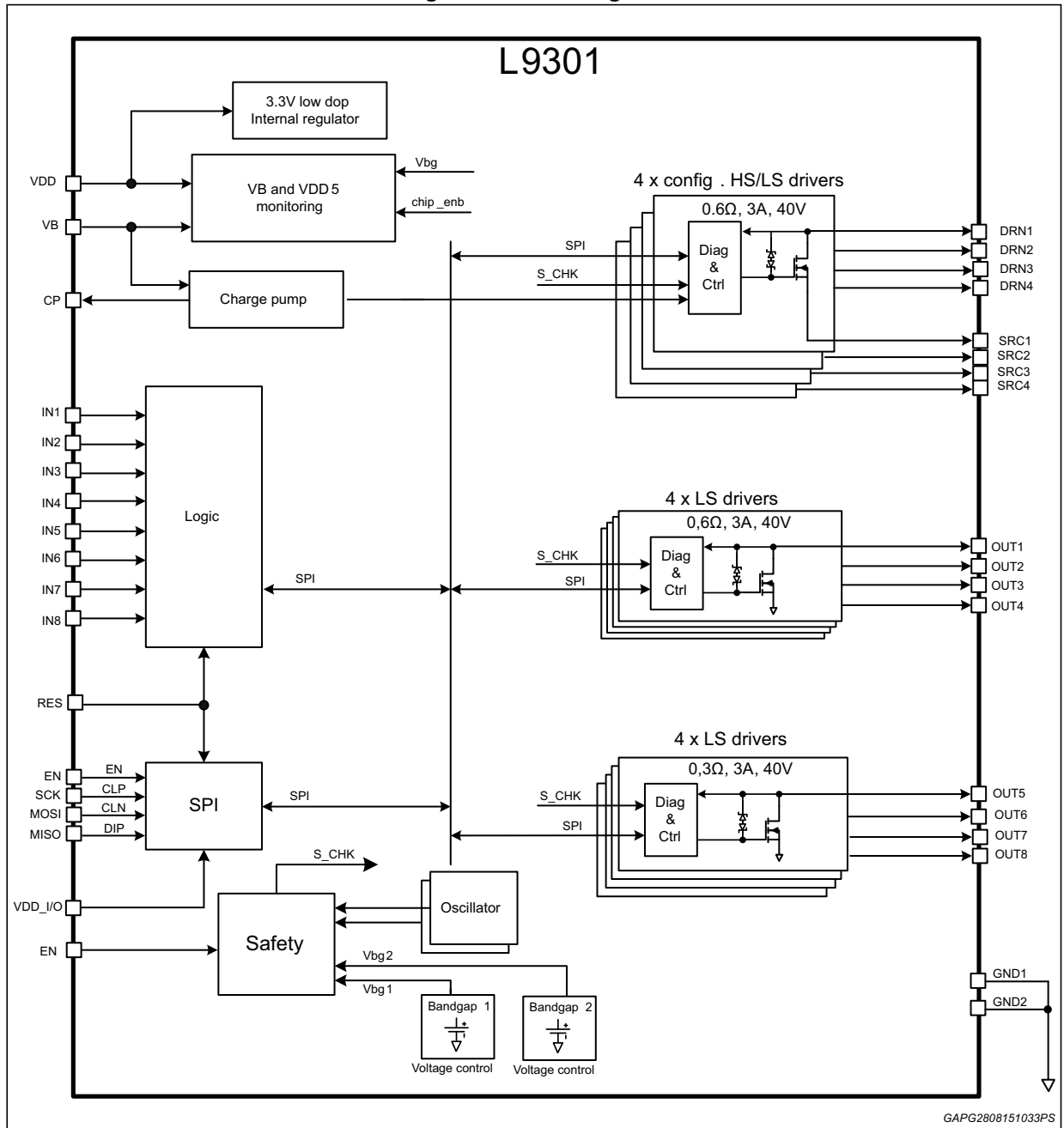
Order code	Package	Packing
L9301-TR	PowerSSO36	Tape & Reel

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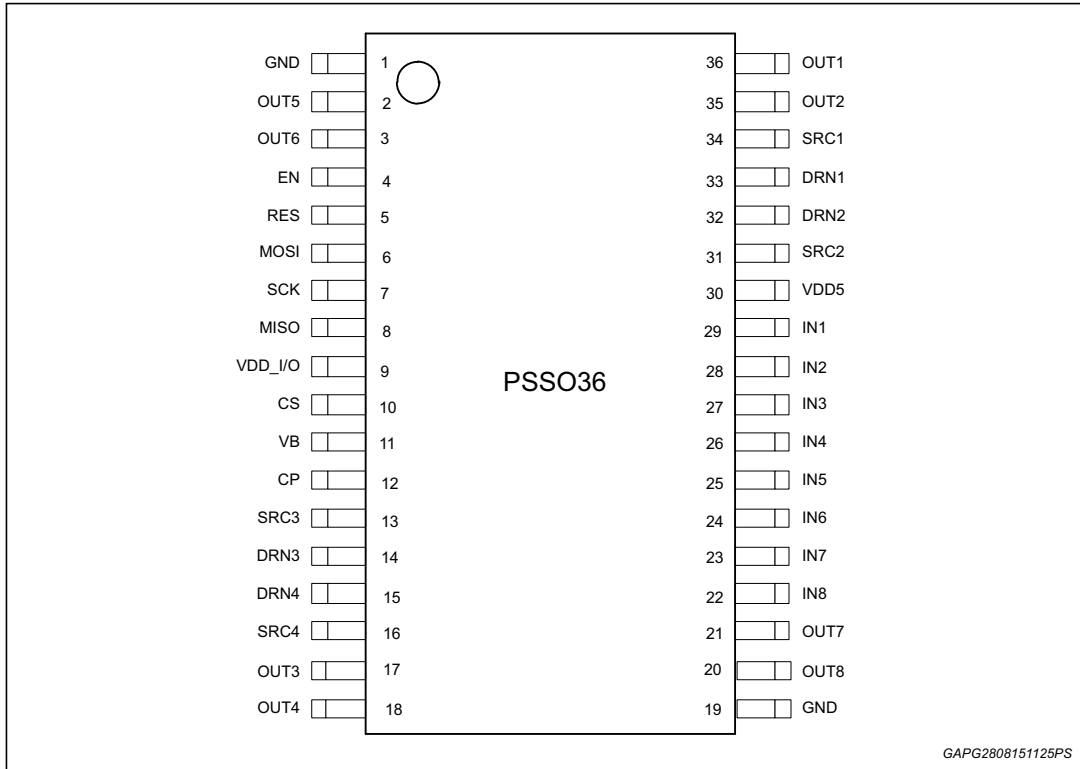
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description

Figure 2. Pin connection diagram



GAPG2808151125PS

Table 2. Pin description

Pin	Symbol	Function
1	GND	Power ground of OUT1,2,5,6
2	OUT5	Output 5
3	OUT6	Output 6
4	EN	Enable
5	RES	Reset input (active low)
6	MOSI	SPI data in
7	SCK	SPI serial clock input
8	MISO	SPI data out
9	VDD_I/O	Microcontroller logic interface voltage
10	CS	SPI chip select (active low)
11	VB	Battery supply voltage
12	CP	Charge pump
13	SRC3	Source pin of configurable driver #3
14	DRN3	Drain pin of configurable driver #3

Table 2. Pin description (continued)

Pin	Symbol	Function
15	DRN4	Drain pin of configurable driver #4
16	SRC4	Source pin of configurable driver #4
17	OUT3	Output 3
18	OUT4	Output 4
19	GND	Power ground of OUT3,4,7,8
20	OUT8	Output 8
21	OUT7	Output 7
22	IN8	Discrete input used to PWM output driver #8
23	IN7	Discrete input used to PWM output driver #7
24	IN6	Discrete input used to PWM output driver #6
25	IN5	Discrete input used to PWM output driver #5
26	IN4	Discrete input used to PWM output driver #4
27	IN3	Discrete input used to PWM output driver #3
28	IN2	Discrete input used to PWM output driver #2
29	IN1	Discrete input used to PWM output driver #1
30	VDD5	5 Volt supply input
31	SRC2	Source pin of configurable driver #2
32	DRN2	Drain pin of configurable driver #2
33	DRN1	Drain pin of configurable driver #1
34	SRC1	Source pin of configurable driver #1
35	OUT2	Output 2
36	OUT1	Output 1
EP	GND	Exposed pad: connected to GND

### 3 Electrical specifications

#### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value [DC voltage]	Unit
VB	Supply voltage	-0.3 to 35	V
VDD, VDD_I/O	Stabilized supply voltage	-0.3 to 18 <sup>(1)</sup>	V
V <sub>CS</sub> , V <sub>SCK</sub> , V <sub>MOSI</sub> , V <sub>MISO</sub> , V <sub>EN</sub> , V <sub>IN1-8</sub> , V <sub>RES</sub>	Logic input/output voltage range	-0.3 to 18 <sup>(1)</sup>	V
OUT1-8	-	-1 to VCL	V
SRC1-4	-	-1 to VB	V
DRN1-4	-	-1 to VCL	V
CP	-	-0.3 to (VB+CP_DELTA)	V
GND	-	-0.3 to +0.3	V

1. Short to 18 V for 100 h max.

*Note:* A suitable device to clamp the voltage during 'load dump' event to a value  $\leq 35$  V must be present at application level.

#### 3.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
ESD according Human Body Model (HBM), Q100-002 for pins <sup>(1)</sup> ; (100 pF/1.5 k $\Omega$ )	$\pm 4000$	V
ESD according Human Body Model (HBM), Q100-002 for all other pins; (100 pF/1.5 k $\Omega$ )	$\pm 2000$	V
ESD according Charged Device Model (CDM), Q100-011 Corner pins	$\pm 750$	V
ESD according Charged Device Model (CDM), Q100-011 Non-corner pins	$\pm 500$	V

1. VB, DRN1-4, SRC1-4, OUT1-8.

### 3.3 Operating range

Table 5. Operating range

Symbol	Parameter	Min.	Max.	Unit
VB	Supply voltage	VB_UV	18	V
VDD	Stabilized supply voltage	VDD_UV	VDD_OV	V
VDD_IO	Logic output supply voltage	3.0	5.5	V

### 3.4 Thermal data

Table 6. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{amb}^{(1)}$	Operating ambient temperature	-40	-	125	°C
$T_{stg}$	Storage temperature	-40	-	150	°C
$T_j$	Junction temperature	-40	-	175	°C
$T_{sd}$	Thermal shutdown temperature	180	-	195	°C
$T_{sd-hys}$	Thermal shutdown temperature hysteresis	-	10	-	°C
$R_{th\ j-amb}^{(2)}$	Thermal Resistance junction to ambient	-	-	24	°C/W
$R_{th\ j-case}$	Thermal Resistance junction to case	-	-	2	°C/W

1. For information only, in any case  $T_j$  limits must not exceed.
2. With 2s2p PCB thermally enhanced.

# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 4.1 PowerSSO-36 (exposed pad) package information

Figure 3. PowerSSO-36 (exposed pad) package outline

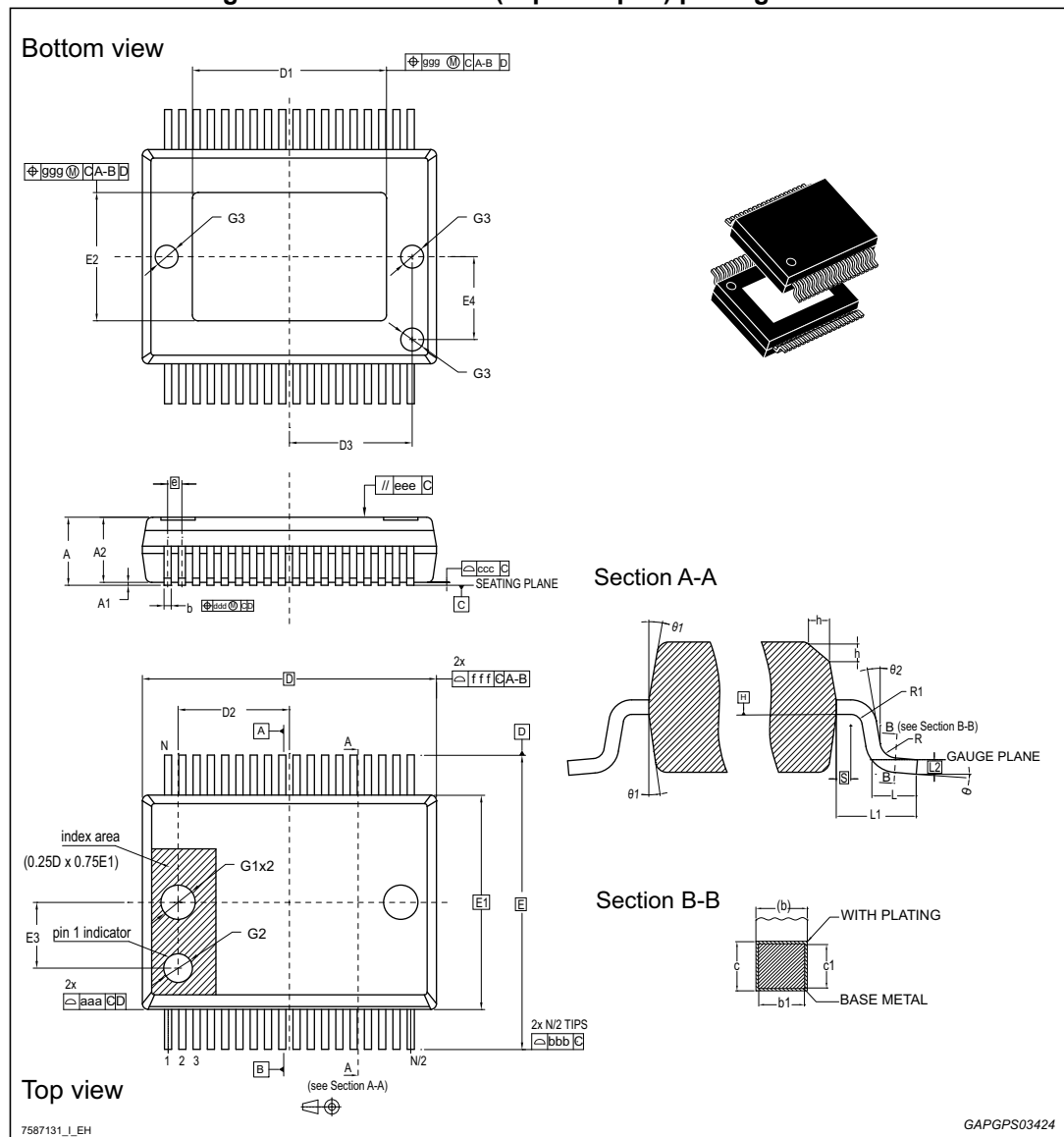


Table 7. PowerSSO-36 (exposed pad) package mechanical data

Ref	Dimensions					
	Millimeters			Inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	-	8°	0°	-	8°
Θ1	5°	-	10°	5°	-	10°
Θ2	0°	-	-	0°	-	-
A	2.15	-	2.45	0.0846	-	0.0965
A1	0.0	-	0.1	0.0	-	0.0039
A2	2.15	-	2.35	0.0846	-	0.0925
b	0.18	-	0.32	0.0071	-	0.0126
b1	0.13	0.25	0.3	0.0051	0.0098	0.0118
c	0.23	-	0.32	0.0091	-	0.0126
c1	0.2	0.2	0.3	0.0079	0.0079	0.0118
D <sup>(2)</sup>	10.30 BSC			0.4055 BSC		
D1	VARIATION					
D2	-	3.65	-	-	0.1437	-
D3	-	4.3	-	-	0.1693	-
e	0.50 BSC			0.0197 BSC		
E	10.30 BSC			0.4055 BSC		
E1 <sup>(2)</sup>	7.50 BSC			0.2953 BSC		
E2	VARIATION					
E3	-	2.3	-	-	0.0906	-
E4	-	2.9	-	-	0.1142	-
G1	-	1.2	-	-	0.0472	-
G2	-	1	-	-	0.0394	-
G3	-	0.8	-	-	0.0315	-
h	0.3	-	0.4	0.0118	-	0.0157
L	0.55	0.7	0.85	0.0217	-	0.0335
L1	1.40 REF			0.0551 REF		
L2	0.25 BSC			0.0098 BSC		
N	36			1.4173		
R	0.3	-	-	0.0118	-	-
R1	0.2	-	-	0.0079	-	-
S	0.25	-	-	0.0098	-	-

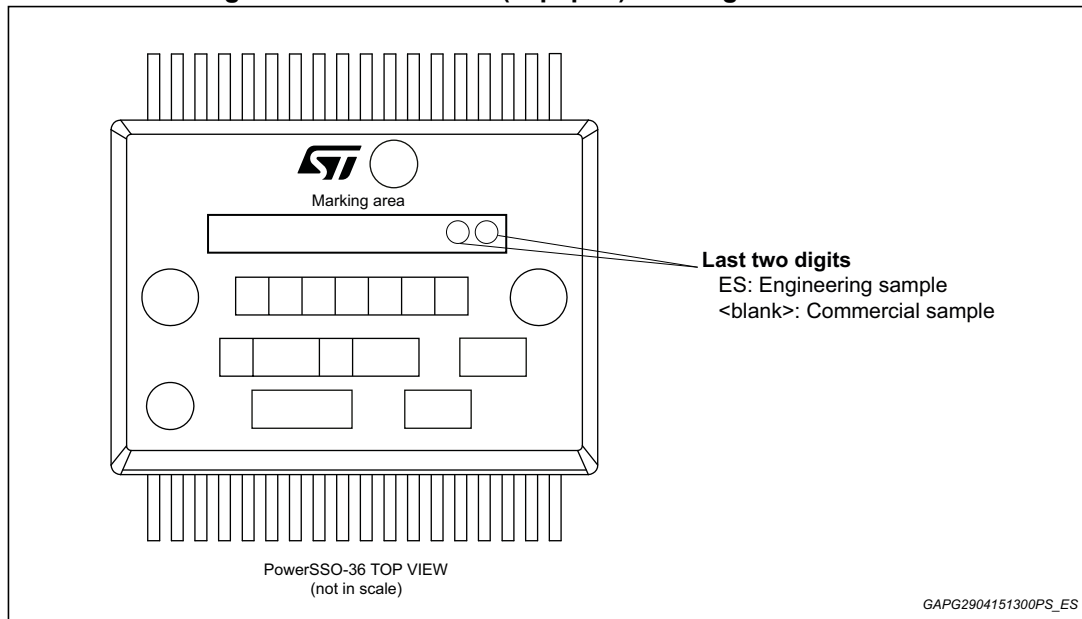
**Table 7. PowerSSO-36 (exposed pad) package mechanical data (continued)**

Ref	Dimensions					
	Millimeters			Inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
<b>Tolerance of form and position</b>						
aaa	0.2			0.0079		
bbb	0.2			0.0079		
ccc	0.1			0.0039		
ddd	0.2			0.0079		
eee	0.1			0.0039		
fff	0.2			0.0079		
ggg	0.15			0.0059		
<b>VARIATIONS</b>						
<b>Option A</b>						
D1	6.5	-	7.1	0.2559	-	0.2795
E2	4.1	-	4.7	0.1614	-	0.1850
<b>Option B</b>						
D1	4.9	-	5.5	0.1929	-	0.2165
E2	4.1	-	4.7	0.1614	-	0.1850
<b>Option C</b>						
D1	6.9	-	7.5	0.2717	-	0.2953
E2	4.3	-	5.2	0.1693	-	0.2047

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is '0.25 mm' per side D and '0.15 mm' per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

## 4.2 PowerSSO-36 (exp. pad) marking information

Figure 4. PowerSSO-36 (exp. pad) marking information



**Note:**

*Engineering Samples: these samples are clearly identified by last two digits 'ES' in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

*Commercial Samples: Fully qualified parts from ST standard production with no usage restrictions.*

## 5 Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Dec-2015	1	Initial release.

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