

# ISO7842x 高性能、8000V<sub>PK</sub> 增强型四通道数字隔离器

## 1 特性

- 信号传输速率：高达 100Mbps
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 和 5V 电平转换
- 宽温度范围：-55°C 至 +125°C
- 低功耗：电流典型值为 1.7mA/通道（1Mbps 时）
- 低传播延迟：典型值为 11ns（5V 电源供电时）
- 业界领先的共模瞬态抗扰度 (CMTI)（最小值）： $\pm 100\text{kV}/\mu\text{s}$  $\text{kV}/\mu\text{s}$
- 优异的电磁兼容性 (EMC)
- 系统级静电放电 (ESD)、瞬态放电 (EFT) 以及浪涌保护
- 低辐射
- 隔离栅寿命：> 40 年末尾新增了一段内容
- 宽体 SOIC-16 封装和超宽体 SOIC-16 封装选项
- 安全及管理批准：中的安全及管理批准列表中的安全及管理批准列表中的安全及管理批准列表
  - 8000V<sub>PK</sub> 增强型隔离，符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准
  - 符合 UL 1577 标准且长达 1 分钟的 5.7kV<sub>RMS</sub> 隔离
  - CSA 组件验收通知 5A, IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 的 CQC 认证
  - 符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证
  - 所有 DW 封装认证已完成；DWW 封装认证已完成，符合 UL、VDE、TUV 标准并计划进行 CSA 和 CQC 认证

## 2 应用

- 工业自动化
- 电机控制
- 电源
- 太阳能逆变器
- 医疗设备
- 混合动力电动汽车

## 3 说明

ISO7842x 器件是一款高性能四通道数字隔离器，隔离电压为 8000V<sub>PK</sub>。该器件已通过符合 VDE、CSA、CQC 和 TUV 标准的增强型隔离认证。在隔离互补金属氧化物半导体 (CMOS) 或者低电压互补金属氧化物半导体 (LVCMOS) 数字 I/O 时，该隔离器可提供高电磁抗扰度和低辐射，同时具备低功耗特性。每个隔离通道都有一个由二氧化硅 (SiO<sub>2</sub>) 绝缘隔栅分开的逻辑输入和输出缓冲器。

该器件配有使能引脚，可用于将多个主驱动应用中的相应输出置于高阻抗状态，也可用于降低功耗。

ISO7842 器件具有 2 个正向通道和 2 个反向通道。如果出现输入功率或信号丢失，ISO7842 器件默认输出高电平，ISO7842F 器件默认输出低电平。更多详细信息，请参见 [Device Functional Modes](#) 部分。

与隔离式电源结合使用时，该器件有助于防止数据总线或者其他电路中的噪声电流进入本地接地，进而干扰或损坏敏感电路。凭借创新的芯片设计和布线技术，ISO7842 器件的电磁兼容性得到了显著增强，可确保提供系统级 ESD、EFT 和浪涌保护并符合辐射标准。

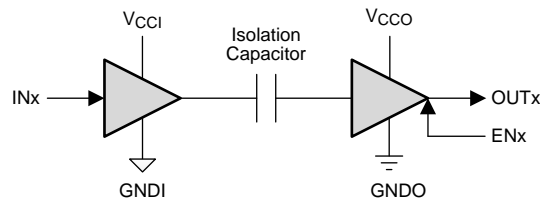
ISO7842 器件采用 16 引脚 SOIC 宽体 (DW) 和超宽体 (DWW) 封装。

器件信息<sup>(1)</sup>

产品型号	封装	封装尺寸 (标称值)
ISO7842	DW (16)	10.30mm x 7.50mm
ISO7842F	DWW (16)	10.30mm x 14.0mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



VCCI 和 GNDI 分别是输入通道的电源和接地连接。

VCCO 和 GNDO 分别是输出通道的电源和接地连接。



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision E (March 2016) to Revision F</b>	<b>Page</b>
• 已更改 隔离栅寿命年数（特性部分） .....	1
• VDE 认证现已完成 .....	1
• Changed $V_{CCO}$ to $V_{CCI}$ for the minimum value of the input threshold voltage hysteresis parameter in all electrical characteristics tables .....	8
• Added $V_{CM}$ to the test condition of the common-mode transient immunity parameter in all electrical characteristics tables .....	8
• Added the lifetime projection graphs for DW and DWW packages to the <i>Safety Limiting Values</i> section .....	18

<b>Changes from Revision D (December 2015) to Revision E</b>	<b>Page</b>
• 已更改 <b>特性</b> .....	1
• 已添加 <b>特性</b> “符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证” .....	1
• 已将 <b>说明</b> 中第一段文本从“符合 VDE、CSA 和 CQC 的认证”。更改为“符合 VDE、CSA、CQC 和 TUV 的认证。” .....	1
• Added Note 1 to <b>Table 3</b> .....	18
• Changed <b>Table 4</b> .....	19
• Added TUV to the <i>Regulatory Information</i> section and <b>Table 5</b> . Deleted Note 1 in <b>Table 5</b> .....	19
• Changed <b>Figure 17</b> .....	21

<b>Changes from Revision C (July 2015) to Revision D</b>	<b>Page</b>
• 已添加 <b>特性</b> ：DW 封装认证已完成；计划进行 DWW 认证 .....	1
• 已向 <b>说明</b> 中添加的文本：和超宽体 (DWW) 封装。 .....	1
• 已将封装“超宽 SOIC、DWW (16)”添加至器件信息表 .....	1
• Changed the MIN value of CMTI in <i>Electrical Characteristics—5-V Supply</i> , 5 V table From: 70 To: 100 kV/μs, deleted	

the TYP value of 100 kV/μs .....	8
• Added the Supply Current - ISO7842DW and ISO7842FDW section to the <i>Electrical Characteristics—5-V Supply</i> .....	8
• Added the Supply Current - ISO7842DWW and ISO7842FDWW section to the <i>Electrical Characteristics—5-V Supply</i> .....	8
• Changed the MIN value of CMTI in <i>Electrical Characteristics—3.3-V Supply</i> , 5 V table From: 70 To: 100 kV/μs, deleted the TYP value of 100 kV/μs .....	9
• Added the Supply Current - ISO7842DW and ISO7842FDW section to the <i>Electrical Characteristics—3.3-V Supply</i> .....	9
• Added the Supply Current - ISO7842DWW and ISO7842FDWW section to the <i>Electrical Characteristics—3.3-V Supply</i> ..	9
• Changed the MIN value of CMTI in <i>Electrical Characteristics—2.5-V Supply</i> , 5 V table From: 70 To: 100 kV/μs, deleted the TYP value of 100 kV/μs .....	10
• Added the Supply Current - ISO7842DW and ISO7842FDW section to the <i>Electrical Characteristics—2.5-V Supply</i> .....	10
• Added the Supply Current - ISO7842DWW and ISO7842FDWW section to the <i>Electrical Characteristics—2.5-V Supply</i> ..	10
• Added the 16-DWW Package to <a href="#">Table 2</a> .....	17
• Added the DWW package information to <a href="#">Table 3</a> .....	18
• Added the DWW package information to <a href="#">Table 5</a> .....	19
• Added text to the <i>Application Information</i> section: " isolation voltage per UL 1577." .....	22

**Changes from Revision B (April 2015) to Revision C**
**Page**

• 已添加器件 ISO7482F 至数据表 .....	1
• 已更改 <i>说明</i> 以包含“ISO7842 器件默认输出“高”电平，ISO7842F 器件默认输出“低”电平。” .....	1
• Changed From: $t_{PLH}$ and $t_{PHL}$ at 5.5V To: $t_{PLH}$ and $t_{PHL}$ at 5.0 V .....	13
• Changed <a href="#">Figure 9</a> .....	15
• Changed <a href="#">Figure 15</a> , Added <a href="#">Figure 16</a> .....	20
• Added the <i>Device I/O Schematics</i> section .....	21

**Changes from Revision A (November 2014) to Revision B**
**Page**

• 已将文档标题从“四通道数字隔离器”更改为“四通道 2/2 数字隔离器” .....	1
• 已添加 <i>特性</i> 2.25V 至 5.5V 电平转换 .....	1
• <i>特性</i> 从“宽体 SOIC-16 封装”更改为“宽体和超宽体 SOIC-16 封装选项” .....	1
• 已更改 <i>特性</i> .....	1
• VDE 认证现已完成 .....	1
• 已更改 <i>简化电路原理图</i> 并已添加注释 1 和注释 2 .....	1
• Added the <i>Power Dissipation Characteristics</i> table .....	7
• Changed <a href="#">Figure 7</a> .....	14
• Changed <a href="#">Figure 8</a> .....	14
• Changed From: $V_{CC1}$ To: $V_{CC1}$ in <a href="#">Figure 9</a> .....	15
• Changed <a href="#">Figure 10</a> .....	15
• Changed <a href="#">Table 2</a> .....	17
• Changed the Test Condition of CTI of the table in <a href="#">Table 2</a> .....	17
• Changed the MIN value of CTI From" > 600 V To: 600 V .....	17
• Changed <a href="#">Table 3</a> title From: <i>DIN V VDE 0884-10 (VDE V 0884-10) and UL 1577 Insulation Characteristics</i> To: <i>Insulation Characteristics</i> .....	18
• Changed <a href="#">Table 3</a> .....	18
• Changed the table in <i>Regulatory Information</i> .....	19
• Deleted INPUT-SIDE and OUTPUT-SIDE from columns 1 and 2 of <a href="#">Table 7</a> .....	21
• Changed the <i>Application Information</i> section .....	22
• Changed the <i>Typical Application</i> section .....	22

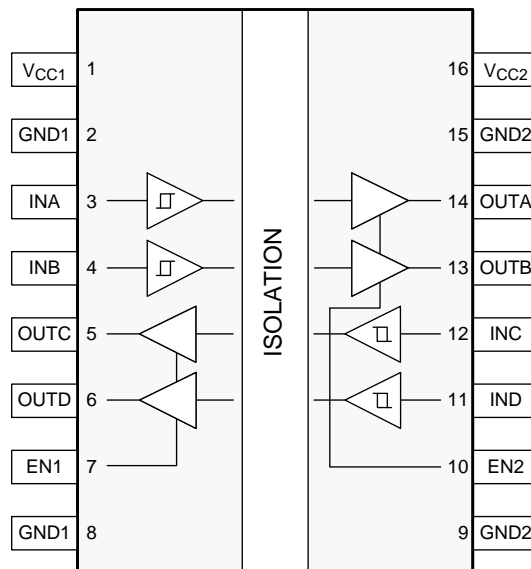
- 
- Added text and [Figure 19](#) to the *Detailed Design Procedure* section ..... [23](#)
- 

**Changes from Original (October 2014) to Revision A**
**Page**

- 
- 已将特性从：所有机构的审批正在审理中改为：所有机构的审批已通过 ..... [1](#)
  - 将 说明 部分的语句从“该器件已通过 VDE 和 CSA 认证，满足增强型隔离要求。”更改为“该器件正在就是否满足增强型隔离要求进行 VDE 和 CSA 审核认证。”..... [1](#)
  - Added Note: "This coupler..." to the *High Voltage Feature Description* section ..... [17](#)
  - Changed R<sub>IO</sub> MIN value From: 10<sup>9</sup> To: 10<sup>11</sup> in the [Table 2](#) table ..... [17](#)
  - Changed the first row of information in the *Regulatory Information* table ..... [19](#)
-

## 5 Pin Configuration and Functions

**DW and DWW Packages  
16-Pin SOIC  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V <sub>CC1</sub>
	8		
GND2	9	—	Ground connection for V <sub>CC2</sub>
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	12	I	Input, channel C
IND	11	I	Input, channel D
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	5	O	Output, channel C
OUTD	6	O	Output, channel D
V <sub>CC1</sub>	1	—	Power supply, V <sub>CC1</sub>
V <sub>CC2</sub>	16	—	Power supply, V <sub>CC2</sub>

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 See <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC1}$ , $V_{CC2}$	Supply voltage <sup>(2)</sup>	-0.5	6	V
Voltage	INx	-0.5	$V_{CCX} + 0.5$ <sup>(3)</sup>	V
	OUTx	-0.5	$V_{CCX} + 0.5$ <sup>(3)</sup>	
	ENx	-0.5	$V_{CCX} + 0.5$ <sup>(3)</sup>	
$I_O$	Output current	-15	15	mA
	Surge immunity		12.8	kV
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±6000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC1}$ , $V_{CC2}$	Supply voltage	2.25		5.5	V
$I_{OH}$	High-level output current	$V_{CCO}^{(1)} = 5\text{ V}$		-4	mA
		$V_{CCO}^{(1)} = 3.3\text{ V}$		-2	
		$V_{CCO}^{(1)} = 2.5\text{ V}$		-1	
$I_{OL}$	Low-level output current	$V_{CCO}^{(1)} = 5\text{ V}$		4	mA
		$V_{CCO}^{(1)} = 3.3\text{ V}$		2	
		$V_{CCO}^{(1)} = 2.5\text{ V}$		1	
$V_{IH}$	High-level input voltage	$0.7 \times V_{CCI}^{(1)}$		$V_{CCI}^{(1)}$	V
$V_{IL}$	Low-level input voltage	0		$0.3 \times V_{CCI}^{(1)}$	V
DR	Signaling rate	0		100	Mbps
$T_J$	Junction temperature <sup>(2)</sup>	-55		150	°C
$T_A$	Ambient temperature	-55	25	125	°C

- (1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .
- (2) To maintain the recommended operating conditions for  $T_J$ , see [Thermal Information](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO7842		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.6	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	49.5	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	15.5	15.2	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	43.1	48.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Power Dissipation Characteristics

		VALUE	UNIT
$P_D$	Maximum power dissipation by ISO78420x	200	mW
$P_{D1}$	Maximum power dissipation by side-1 of ISO78420x	100	
$P_{D2}$	Maximum power dissipation by side-2 of ISO78420x	100	

$V_{CC1} = V_{CC2} = 5.5\text{ V}$ ,  $T_J = 150^\circ\text{C}$ ,  
 $C_L = 15\text{ pF}$ , input a 50 MHz 50% duty cycle square wave

## 6.6 Electrical Characteristics–5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage $I_{OH} = -4\text{ mA}$ ; see <a href="#">Figure 7</a>	$V_{CCO}^{(1)} - 0.4$	$V_{CCO}^{(1)} - 0.2$		V
$V_{OL}$	Low-level output voltage $I_{OL} = 4\text{ mA}$ ; see <a href="#">Figure 7</a>		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CC1}^{(1)}$			V
$I_{IH}$	High-level input current $V_{IH} = V_{CC1}^{(1)}$ at INx or ENx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current $V_{IL} = 0\text{ V}$ at INx or ENx	-10			
CMTI	Common-mode transient immunity $V_I = V_{CC1}^{(1)}$ or $0\text{ V}$ , $V_{CM} = 1500\text{ V}$ ; see <a href="#">Figure 10</a>	100			kV/ $\mu\text{s}$

 (1)  $V_{CC1}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

## 6.7 Supply Current Characteristics–5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
<b>ISO7842DW AND ISO7842FDW</b>						
Supply current	Disable	$EN1 = EN2 = 0\text{ V}$ , $V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	1	1.5	mA
		$EN1 = EN2 = 0\text{ V}$ , $V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	3.4	4.8	mA
	DC signal	$V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	2	2.7	mA
		$V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	4.4	6.1	mA
	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$	3.3	4.6	mA
		10 Mbps	$I_{CC1}, I_{CC2}$	4.2	5.6	mA
100 Mbps		$I_{CC1}, I_{CC2}$	13.7	16.6	mA	
<b>ISO7842DWW AND ISO7842FDWW</b>						
Supply current	Disable	$EN1 = EN2 = 0\text{ V}$ , $V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	1	1.5	mA
		$EN1 = EN2 = 0\text{ V}$ , $V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	3.4	4.8	mA
	DC signal	$V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	2	2.8	mA
		$V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	4.4	6.3	mA
	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$	3.4	4.7	mA
		10 Mbps	$I_{CC1}, I_{CC2}$	4.3	5.9	mA
100 Mbps		$I_{CC1}, I_{CC2}$	14	17.3	mA	

 (1)  $V_{CC1}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

## 6.8 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage $I_{OH} = -2\text{ mA}$ ; see <a href="#">Figure 7</a>	$V_{CCO}^{(1)} - 0.4$	$V_{CCO}^{(1)} - 0.2$		V
$V_{OL}$	Low-level output voltage $I_{OL} = 2\text{ mA}$ ; see <a href="#">Figure 7</a>		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}^{(1)}$			V
$I_{IH}$	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current $V_{IL} = 0\text{ V}$ at INx or ENx	-10			$\mu\text{A}$
CMTI	Common-mode transient immunity $V_I = V_{CCI}^{(1)}$ or $0\text{ V}$ , $V_{CM} = 1500\text{ V}$ ; see <a href="#">Figure 10</a>	100			kV/ $\mu\text{s}$

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

## 6.9 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
<b>ISO7842DW AND ISO7842FDW</b>						
Supply current	Disable	$EN1 = EN2 = 0\text{ V}$ , $V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CCI}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	1	1.5	$\text{mA}$
		$EN1 = EN2 = 0\text{ V}$ , $V_I = V_{CCI}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	3.4	4.8	$\text{mA}$
	DC signal	$V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CCI}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	2	2.7	$\text{mA}$
		$V_I = V_{CCI}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	4.4	6.1	$\text{mA}$
	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$	3.3	4.5	$\text{mA}$
		10 Mbps	$I_{CC1}, I_{CC2}$	4	5.2	$\text{mA}$
100 Mbps		$I_{CC1}, I_{CC2}$	10.8	12.9	$\text{mA}$	
<b>ISO7842DWW and ISO7842FDWW</b>						
Supply current	Disable	$EN1 = EN2 = 0\text{ V}$ , $V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CCI}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	1	1.5	$\text{mA}$
		$EN1 = EN2 = 0\text{ V}$ , $V_I = V_{CCI}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	3.4	4.8	$\text{mA}$
	DC signal	$V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CCI}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$	2	2.8	$\text{mA}$
		$V_I = V_{CCI}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$	4.4	6.3	$\text{mA}$
	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$	3.4	4.7	$\text{mA}$
		10 Mbps	$I_{CC1}, I_{CC2}$	4.1	5.5	$\text{mA}$
100 Mbps		$I_{CC1}, I_{CC2}$	11	13.6	$\text{mA}$	

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

## 6.10 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{ mA}$ ; see <a href="#">Figure 7</a>	$V_{CCO}^{(1)} - 0.4$	$V_{CCO}^{(1)} - 0.2$		V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1\text{ mA}$ ; see <a href="#">Figure 7</a>		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CC1}^{(1)}$			V
$I_{IH}$	High-level input current	$V_{IH} = V_{CC1}^{(1)}$ at INx or ENx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at INx or ENx	-10			$\mu\text{A}$
CMTI	Common-mode transient immunity	$V_I = V_{CC1}^{(1)}$ or $0\text{ V}$ , $V_{CM} = 1500\text{ V}$ ; see <a href="#">Figure 10</a>	100			kV/ $\mu\text{s}$

 (1)  $V_{CC1}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

## 6.11 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
<b>ISO7842DW AND ISO7842FDW</b>							
Supply current	Disable	$EN1 = EN2 = 0\text{ V}$ , $V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$		1	1.5	$\text{mA}$
		$EN1 = EN2 = 0\text{ V}$ , $V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$		3.4	4.8	$\text{mA}$
	DC signal	$V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$		2	2.7	$\text{mA}$
		$V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$		4.4	6.1	$\text{mA}$
	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$		3.2	4.5	$\text{mA}$
		10 Mbps	$I_{CC1}, I_{CC2}$		3.7	5.1	$\text{mA}$
100 Mbps		$I_{CC1}, I_{CC2}$		8.9	10.8	$\text{mA}$	
<b>ISO7842DWW AND ISO7842FDWW</b>							
Supply current	Disable	$EN1 = EN2 = 0\text{ V}$ , $V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$		1	1.5	$\text{mA}$
		$EN1 = EN2 = 0\text{ V}$ , $V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$		3.4	4.8	$\text{mA}$
	DC signal	$V_I = 0\text{ V}$ (ISO7842F), $V_I = V_{CC1}^{(1)}$ (ISO7842)	$I_{CC1}, I_{CC2}$		2	2.8	$\text{mA}$
		$V_I = V_{CC1}^{(1)}$ (ISO7842F), $V_I = 0\text{ V}$ (ISO7842)	$I_{CC1}, I_{CC2}$		4.4	6.3	$\text{mA}$
	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$		3.3	4.6	$\text{mA}$
		10 Mbps	$I_{CC1}, I_{CC2}$		3.8	5.3	$\text{mA}$
100 Mbps		$I_{CC1}, I_{CC2}$		9	11.5	$\text{mA}$	

 (1)  $V_{CC1}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

## 6.12 Switching Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See Figure 7	6	11	16	ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $		0.55	4.1	ns	
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			2.5	ns
$t_{sk(pp)}$	Part-to-part skew time <sup>(3)</sup>				4.5	ns
$t_r$	Output signal rise time	See Figure 7		1.7	3.9	ns
$t_f$	Output signal fall time			1.9	3.9	ns
$t_{PHZ}$	Disable propagation delay, high-to-high impedance output	See Figure 8		12	20	ns
$t_{PLZ}$	Disable propagation delay, low-to-high impedance output			12	20	ns
$t_{PZH}$	Enable propagation delay, high impedance-to-high output for ISO7842			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7842F			2	2.5	$\mu\text{s}$
$t_{PZL}$	Enable propagation delay, high impedance-to-low output for ISO7842			2	2.5	$\mu\text{s}$
	Enable propagation delay, high impedance-to-low output for ISO7842F			10	20	ns
$t_{is}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.7 V. See Figure 9		0.2	9	$\mu\text{s}$
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.90		ns

- (1) Also known as pulse skew.
- (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.13 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See Figure 7	6	10.8	16	ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $		0.7	4.2	ns	
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time <sup>(3)</sup>				4.5	ns
$t_r$	Output signal rise time	See Figure 7		0.8	3	ns
$t_f$	Output signal fall time			0.8	3	ns
$t_{PHZ}$	Disable propagation delay, high-to-high impedance output	See Figure 8		17	32	ns
$t_{PLZ}$	Disable propagation delay, low-to-high impedance output			17	32	ns
$t_{PZH}$	Enable propagation delay, high impedance-to-high output for ISO7842			17	32	ns
	Enable propagation delay, high impedance-to-high output for ISO7842F			2	2.5	$\mu\text{s}$
$t_{PZL}$	Enable propagation delay, high impedance-to-low output for ISO7842			2	2.5	$\mu\text{s}$
	Enable propagation delay, high impedance-to-low output for ISO7842F			17	32	ns
$t_{is}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.7 V. See Figure 9		0.2	9	$\mu\text{s}$
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.91		ns

- (1) Also known as Pulse Skew.
- (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.14 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	Propagation delay time	See Figure 7	7.5	11.7	17.5	ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $		0.66	4.2		ns
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same-direction Channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time <sup>(3)</sup>				4.5	ns
$t_r$	Output signal rise time	See Figure 7		1	3.5	ns
$t_f$	Output signal fall time			1.2	3.5	ns
$t_{PHZ}$	Disable propagation delay, high-to-high impedance output	See Figure 8		22	45	ns
$t_{PLZ}$	Disable propagation delay, low-to-high impedance output			22	45	ns
$t_{PZH}$	Enable propagation delay, high impedance-to-high output for ISO7842			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7842F			2	2.5	$\mu\text{s}$
$t_{PZL}$	Enable propagation delay, high impedance-to-low output for ISO7842			2	2.5	$\mu\text{s}$
	Enable propagation delay, high impedance-to-low output for ISO7842F			18	45	ns
$t_{fs}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.7 V. See Figure 9		0.2	9	$\mu\text{s}$
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.91		ns

- (1) Also known as pulse skew.
- (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

### 6.15 Typical Characteristics

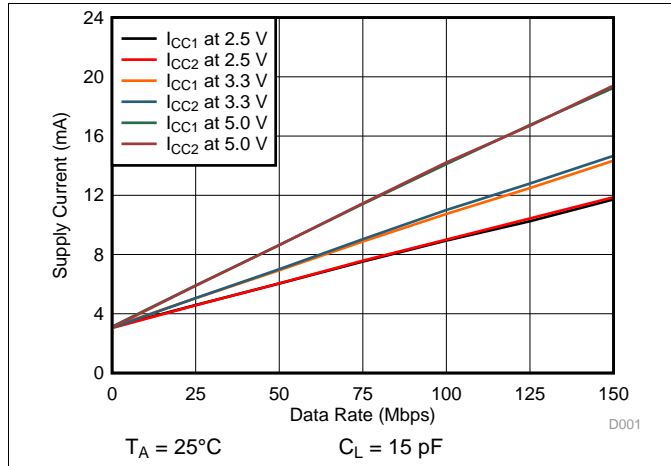


Figure 1. Supply Current vs Data Rate (With 15-pF Load)

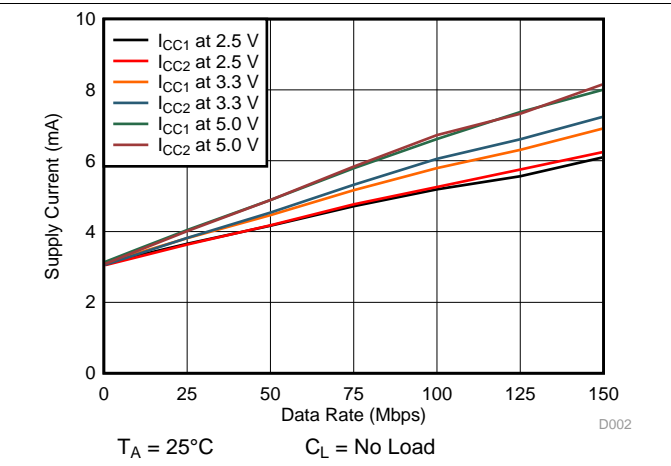


Figure 2. Supply Current vs Data Rate (With No Load)

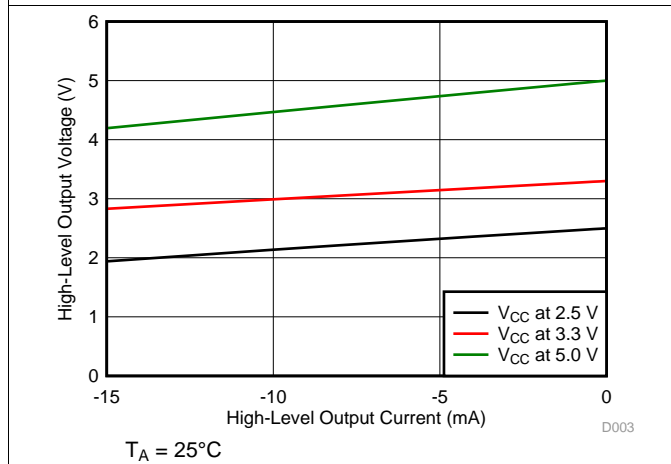


Figure 3. High-Level Output Voltage vs High-level Output Current

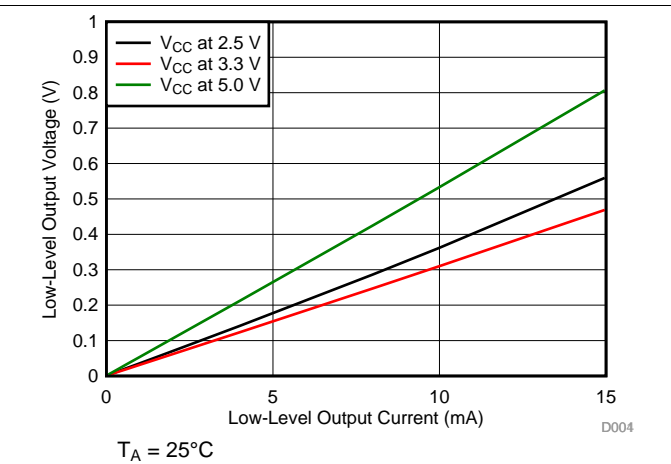


Figure 4. Low-Level Output Voltage vs Low-Level Output Current

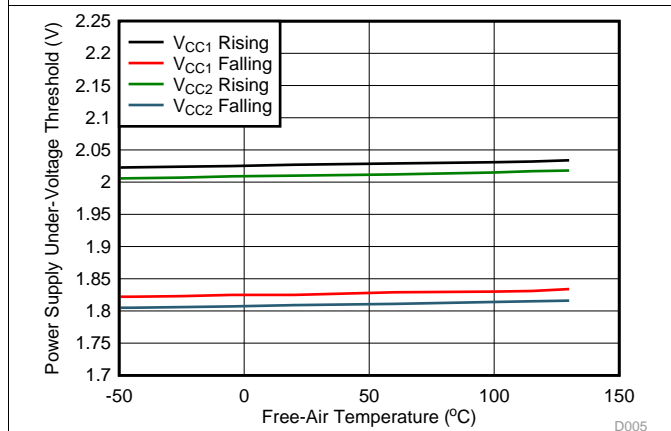


Figure 5. Power Supply Undervoltage Threshold vs Free-Air Temperature

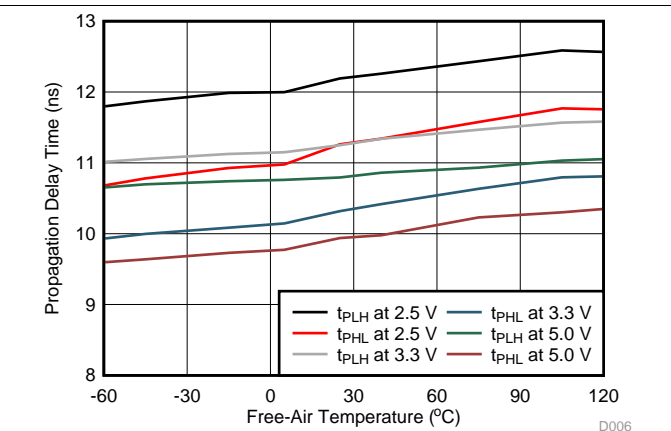
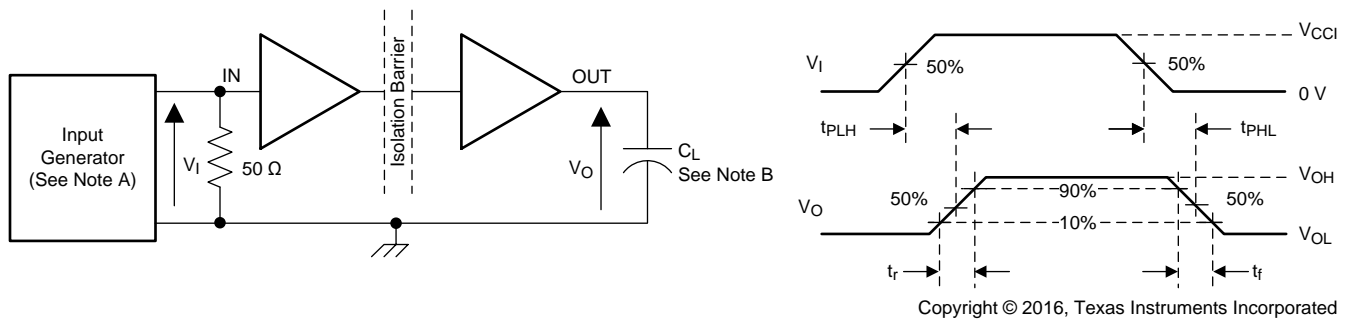


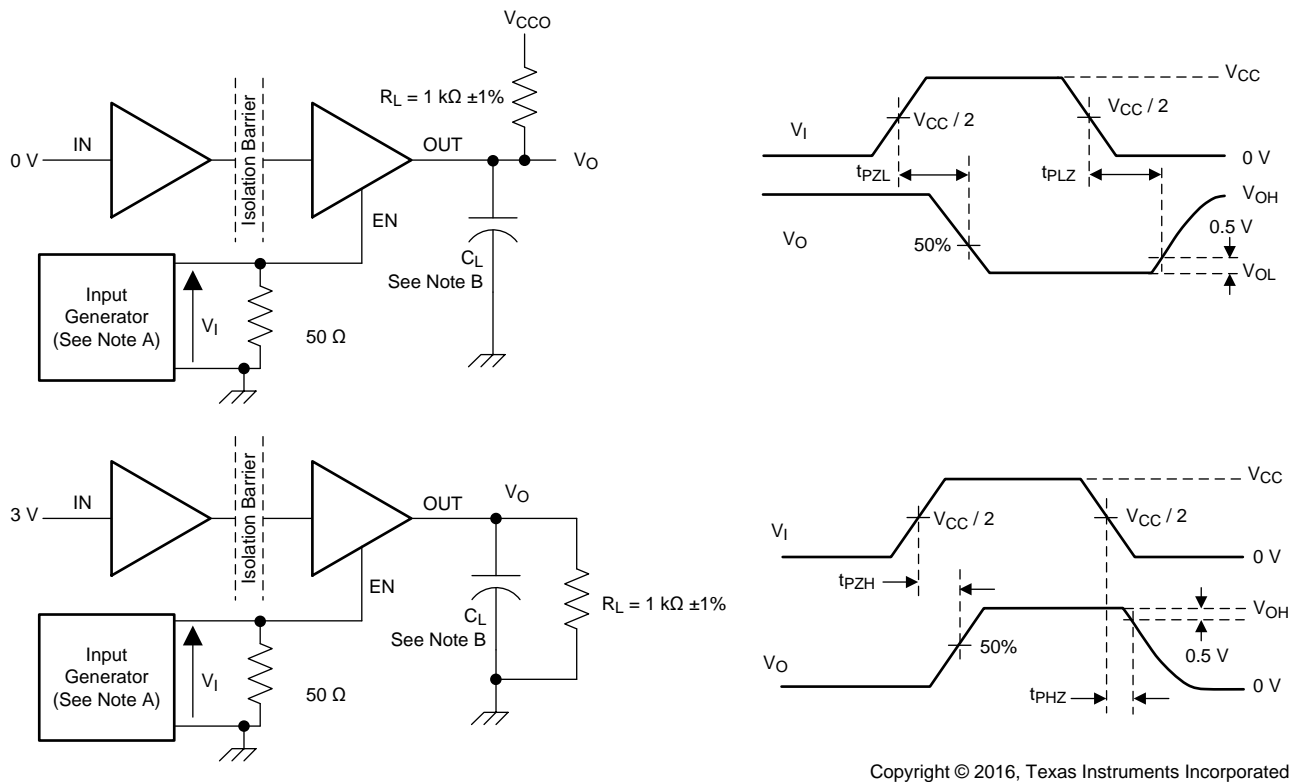
Figure 6. Propagation Delay Time vs Free-Air Temperature

## 7 Parameter Measurement Information



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50 \Omega$ . At the input, 50  $\Omega$  resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

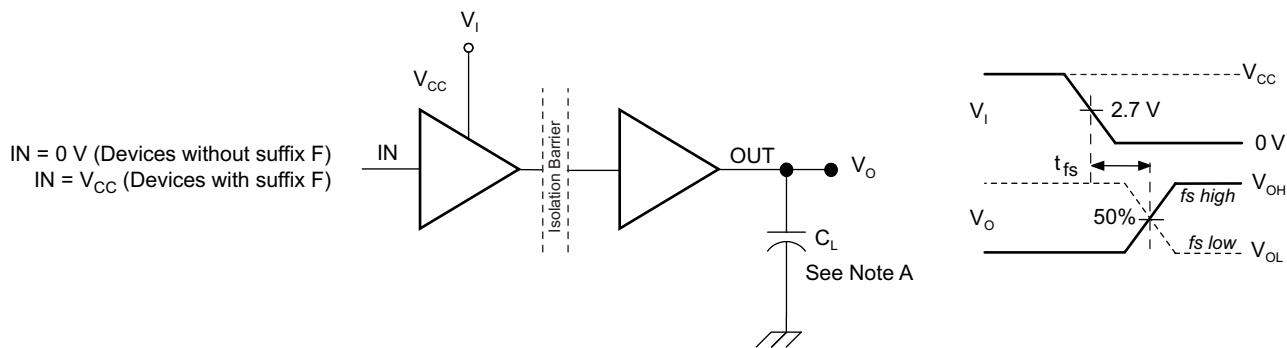
**Figure 7. Switching Characteristics Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  10 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50 \Omega$ .
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 8. Enable/Disable Propagation Delay Time Test Circuit and Waveform**

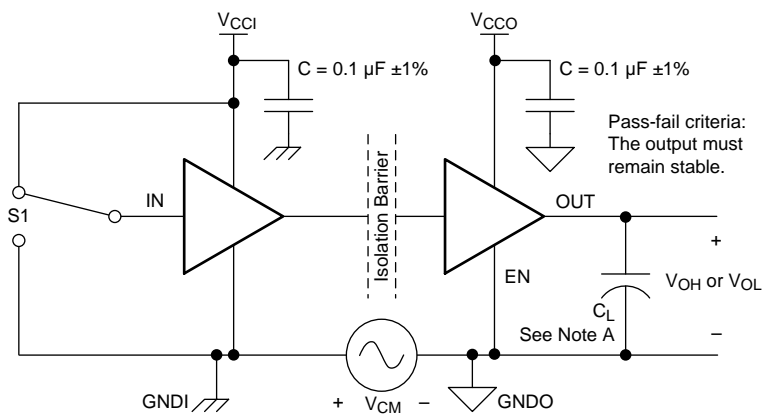
Parameter Measurement Information (continued)



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- A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 9. Default Output Delay Time Test Circuit and Voltage Waveforms



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- A.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

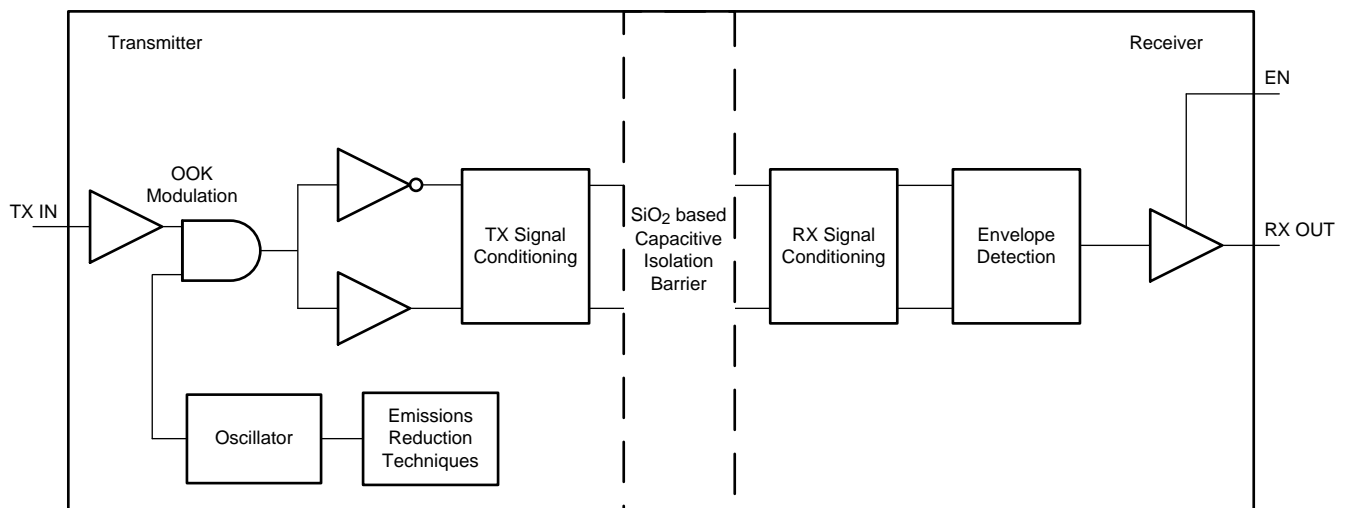
Figure 10. Common-Mode Transient Immunity Test Circuit

## 8 Detailed Description

### 8.1 Overview

The ISO7842 device uses an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. The ISO7842 device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 11](#), shows a functional block diagram of a typical channel.

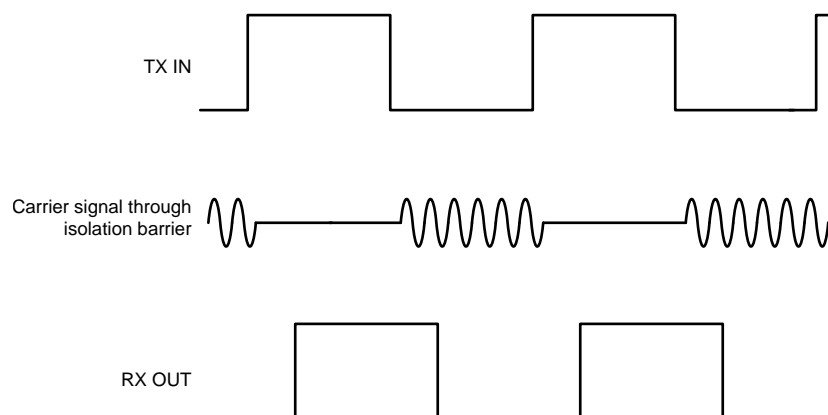
### 8.2 Functional Block Diagram



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**Figure 11. Conceptual Block Diagram of a Digital Capacitive Isolator**

[Figure 12](#) shows a conceptual detail of how the ON-OFF keying scheme works.



**Figure 12. On-Off Keying (OOK) Based Modulation Scheme**

### 8.3 Feature Description

Table 1 lists the device features.

**Table 1. Device Features**

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7842	2 Forward,	5700 V <sub>RMS</sub> / 8000 V <sub>PK</sub> <sup>(1)</sup>	100 Mbps	High
	2 Reverse			
ISO7842F	2 Forward,	5700 V <sub>RMS</sub> / 8000 V <sub>PK</sub> <sup>(1)</sup>	100 Mbps	Low
	2 Reverse			

(1) See [Regulatory Information](#) for detailed isolation ratings.

#### 8.3.1 High Voltage Feature Description

**NOTE**

This coupler is suitable for 'safe electrical insulation' only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

**Table 2. Package Insulation and Safety-Related Specifications over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLR	External clearance	Shortest terminal-to-terminal distance through air	16-DW Package	8		mm
			16-DWW Package	14.5		
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	16-DW Package	8		mm
			16-DWW Package	14.5		
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	600			V
R <sub>IO</sub>	Isolation resistance, input to output <sup>(1)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	10 <sup>12</sup>			Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ max	10 <sup>11</sup>			Ω
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(1)</sup>	V <sub>IO</sub> = 0.4 × sin(2πft), f = 1 MHz		2		pF
C <sub>I</sub>	Input capacitance <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> /2 + 0.4 × sin(2πft), f = 1 MHz, V <sub>CC</sub> = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.

(2) Measured from input pin to ground.

**NOTE**

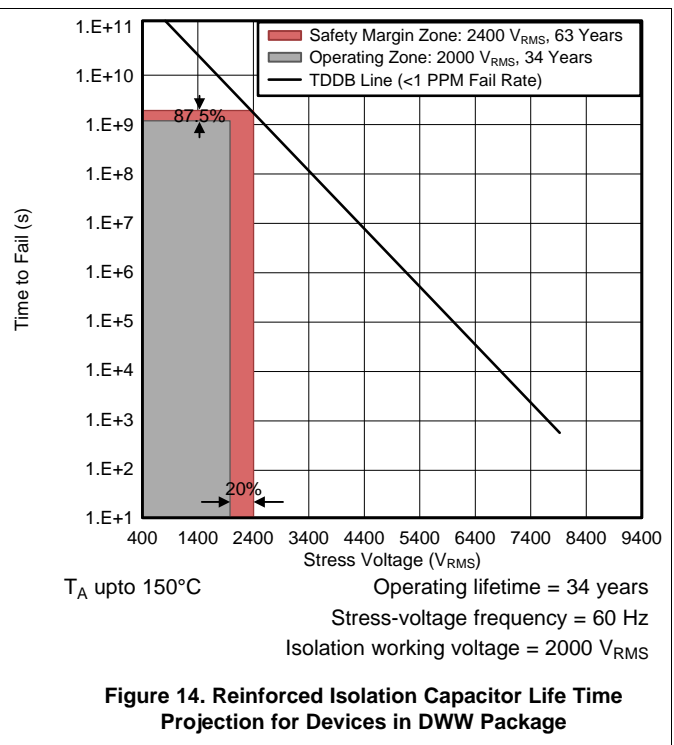
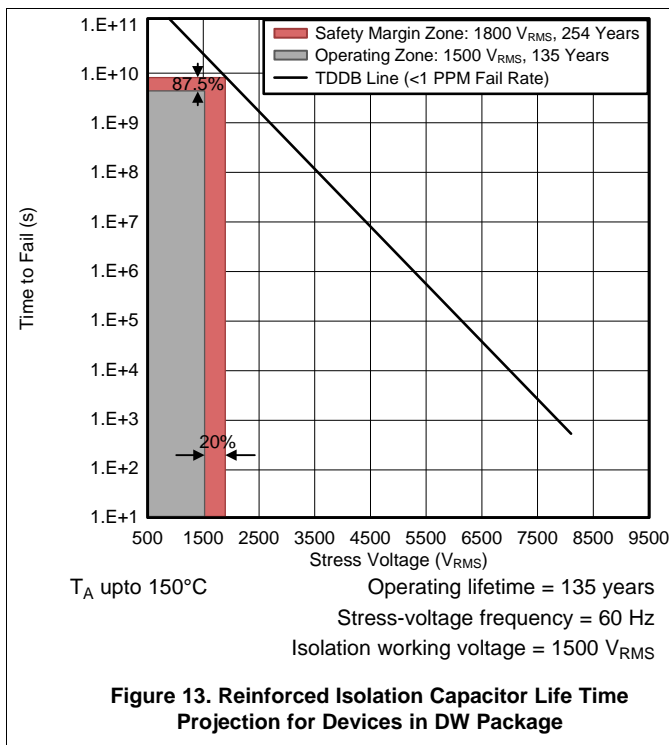
Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

**Table 3. Insulation Characteristics**

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	μm
V <sub>IOWM</sub>	Maximum rated working isolation voltage	Time dependent dielectric breakdown (TDDB) Test, see Figure 13 and Figure 14	1500	2000	V <sub>RMS</sub>
			2121	2828	V <sub>DC</sub>
<b>DIN V VDE V 0884-10 (VDE V 0884-10):2006-12</b>					
V <sub>IOTM</sub>	Maximum rated transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> t = 60 sec (qualification) t = 1 sec (100% production)	8000	8000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage for reinforced insulation	Test method per IEC 60065, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 12800 V <sub>PK</sub> <sup>(1)</sup> (qualification)	8000	8000	V <sub>PK</sub>
V <sub>IORM</sub>	Maximum rated repetitive peak isolation voltage		2121	2828	V <sub>PK</sub>
V <sub>PR</sub>	Input-to-output test voltage	Method a, After Input/Output safety test subgroup 2/3, V <sub>PR</sub> = V <sub>IORM</sub> × 1.2, t = 10 s, Partial discharge < 5 pC	2545	3394	V <sub>PK</sub>
		Method a, After environmental tests subgroup 1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.6, t = 10 s, Partial Discharge < 5 pC	3394	4525	
		Method b1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	3977	5303	
R <sub>S</sub>	Isolation resistance	V <sub>IO</sub> = 500 V at T <sub>S</sub>	>10 <sup>9</sup>	>10 <sup>9</sup>	Ω
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
<b>UL 1577</b>					
V <sub>ISO</sub>	Maximum withstanding isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5700 V <sub>RMS</sub> , t = 60 sec (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6840 V <sub>RMS</sub> , t = 1 sec (100% production)	5700	5700	V <sub>RMS</sub>

(1) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.



**Table 4. IEC 60664-1 Ratings Table**

PARAMETER		TEST CONDITIONS	SPECIFICATION
Material group			I
Overvoltage category / Installation classification	DW package	Rated mains voltage $\leq 600 V_{RMS}$	I–IV
		Rated mains voltage $\leq 1000 V_{RMS}$	I–III
	DWW package	Rated mains voltage $\leq 1000 V_{RMS}$	I–IV

### 8.3.1.1 Regulatory Information

Certifications for the DW package are complete. DWW package certifications are complete for UL, VDE and TUV and planned for CSA and CQC.

**Table 5. Regulatory Information**

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, $8000 V_{PK}$ ; Maximum repetitive peak isolation voltage, $2121 V_{PK}$ (DW), $2828 V_{PK}$ (DWW); Maximum surge isolation voltage, $8000 V_{PK}$	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., $800 V_{RMS}$ (DW package) and $1450 V_{RMS}$ (DWW package) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, $250 V_{RMS}$ ( $354 V_{PK}$ ) max working voltage (DW package)	Single protection, $5700 V_{RMS}$	Reinforced Insulation, Altitude $\leq 5000$ m, Tropical Climate, $250 V_{RMS}$ maximum working voltage	$5700 V_{RMS}$ Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of $600 V_{RMS}$ (DW package) and $1000 V_{RMS}$ (DWW package)  $5700 V_{RMS}$ Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of $800 V_{RMS}$ (DW package) and $1450 V_{RMS}$ (DWW package)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

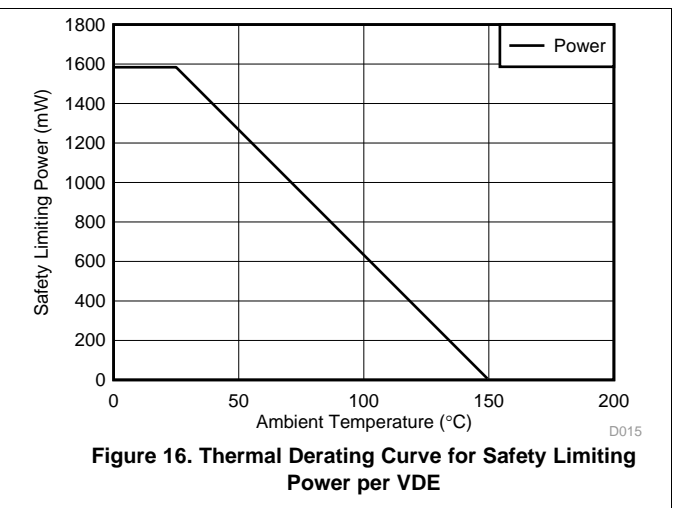
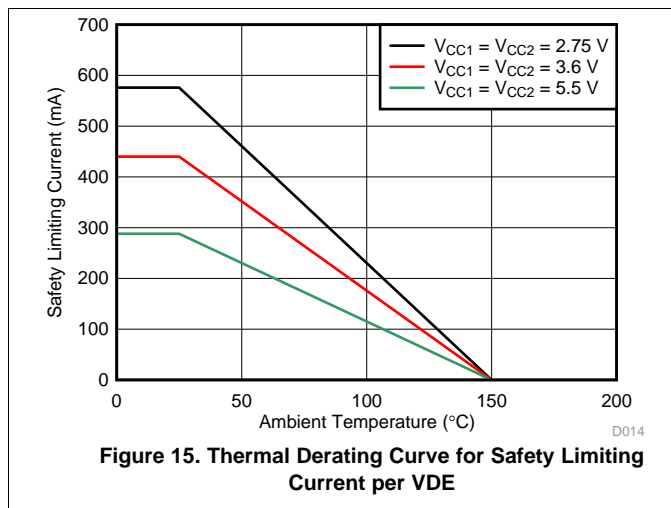
### 8.3.1.2 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

**Table 6. Safety Limiting Values**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub> Safety input, output, or supply current	R <sub>θJA</sub> = 78.9°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			288	mA
	R <sub>θJA</sub> = 78.9°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			440	
	R <sub>θJA</sub> = 78.9°C/W, V <sub>I</sub> = 2.75 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			576	
P <sub>S</sub> Safety input, output, or total power	R <sub>θJA</sub> = 78.9°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1584	mW
T <sub>S</sub> Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a High-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.



### 8.4 Device Functional Modes

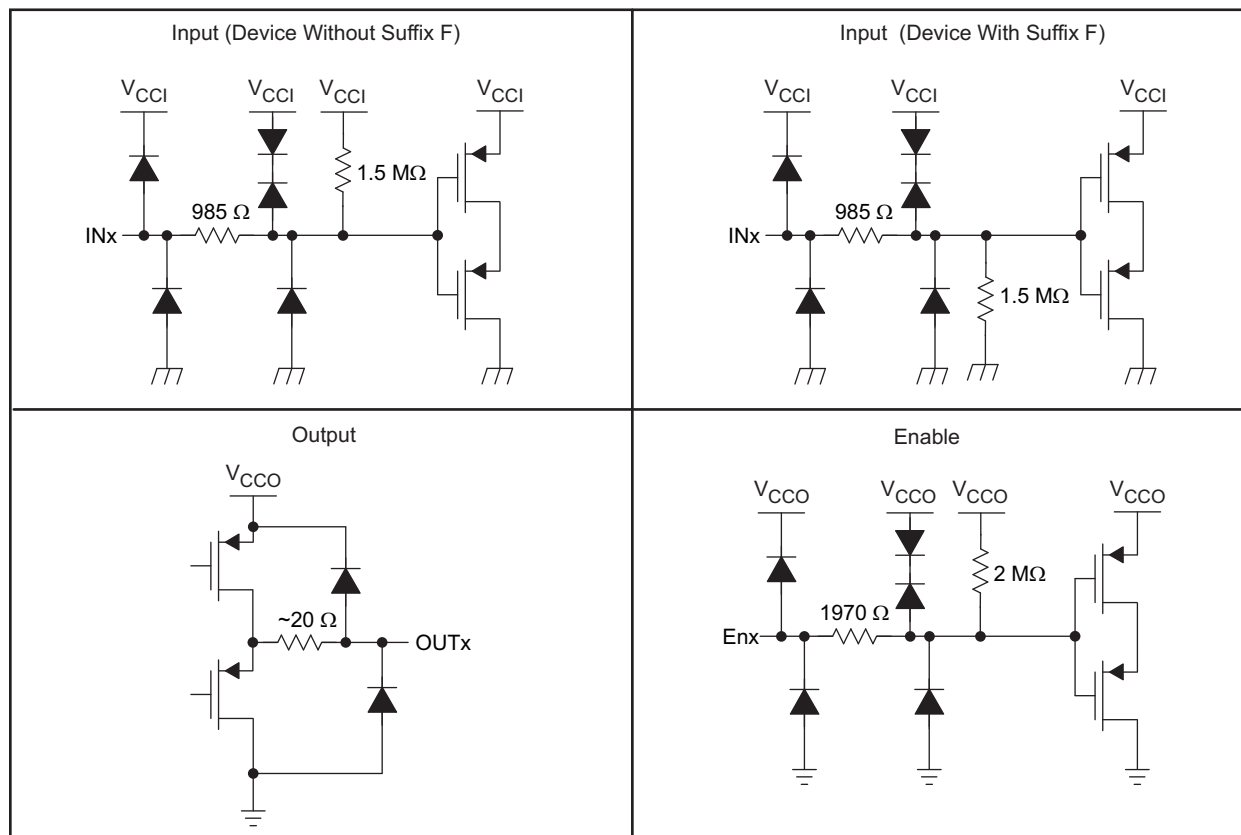
Table 7 lists the ISO7842 functional modes.

Table 7. Function Table<sup>(1)</sup>

V <sub>CCI</sub>	V <sub>CCO</sub>	INPUT (IN <sub>x</sub> ) <sup>(2)</sup>	OUTPUT ENABLE (EN <sub>x</sub> )	OUTPUT (OUT <sub>x</sub> )	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When IN <sub>x</sub> is open, the corresponding channel output goes to its default logic state. Default= High for ISO7842 and Low for ISO7842F.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V <sub>CCI</sub> is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for ISO7842 and Low for ISO7842F. When V <sub>CCI</sub> transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V <sub>CCI</sub> transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V <sub>CCO</sub> is unpowered, a channel output is undetermined <sup>(3)</sup> . When V <sub>CCO</sub> transitions from unpowered to powered-up, a channel output assumes the logic state of its input

- (1) V<sub>CCI</sub> = Input-side V<sub>CC</sub>; V<sub>CCO</sub> = Output-side V<sub>CC</sub>; PU = Powered up (V<sub>CC</sub> ≥ 2.25 V); PD = Powered down (V<sub>CC</sub> ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
- (2) A strongly driven input signal can weakly power the floating V<sub>CC</sub> through an internal protection diode and cause undetermined output.
- (3) The outputs are in undetermined state when 1.7 V < V<sub>CCI</sub>, V<sub>CCO</sub> < 2.25 V.

#### 8.4.1 Device I/O Schematics



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Figure 17. Device I/O Schematics

## 9 Application and Implementation

### NOTE

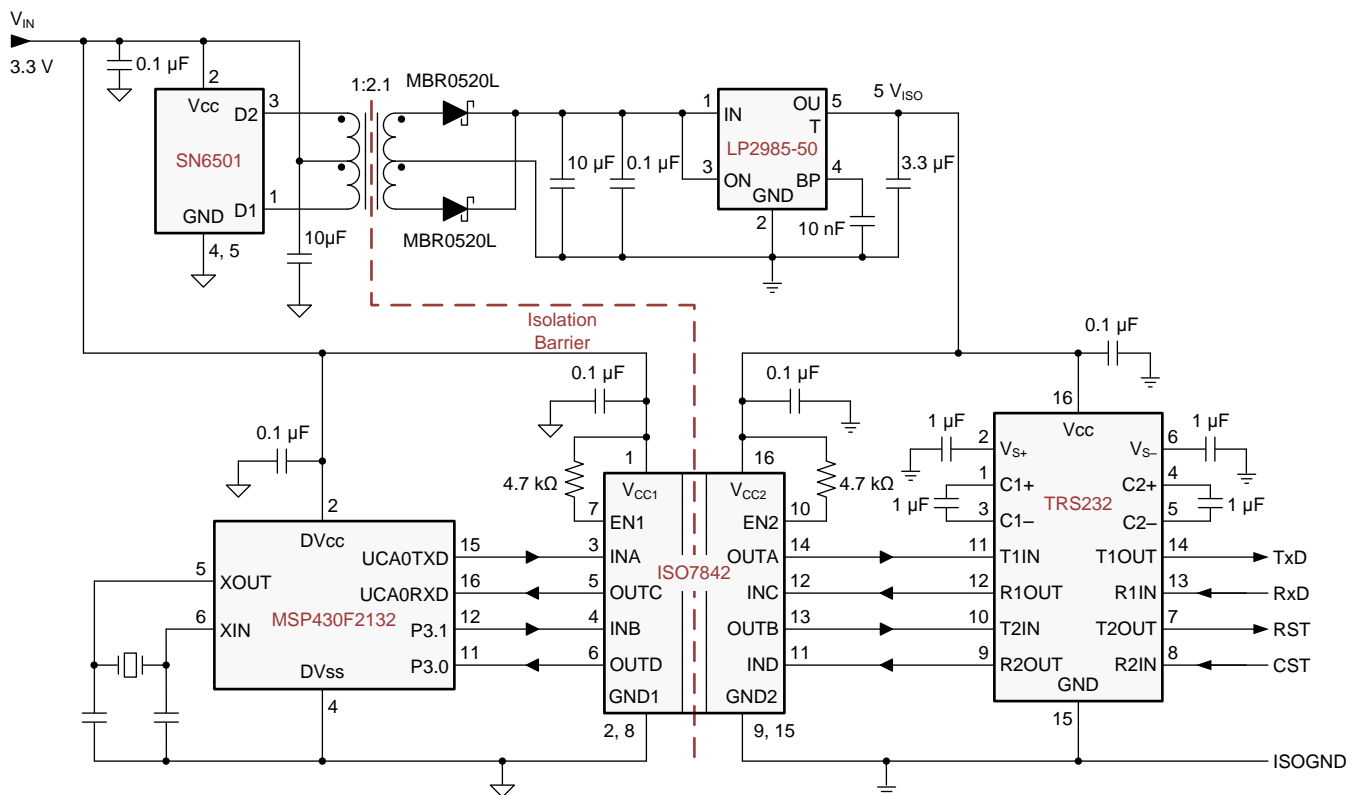
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The ISO7842 device is a high-performance, quad-channel digital isolator with a 5.7-kV<sub>RMS</sub> isolation voltage per UL 1577. The device comes with enable pins on each side that can be used to put the respective outputs in high impedance for multi-master driving applications and reduce power consumption. The ISO7842 device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V<sub>CC1</sub> and V<sub>CC2</sub>. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu$ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

### 9.2 Typical Application

Figure 18 shows the typical isolated RS-232 interface implementation.



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**Figure 18. Isolated RS-232 Interface**

## Typical Application (continued)

### 9.2.1 Design Requirements

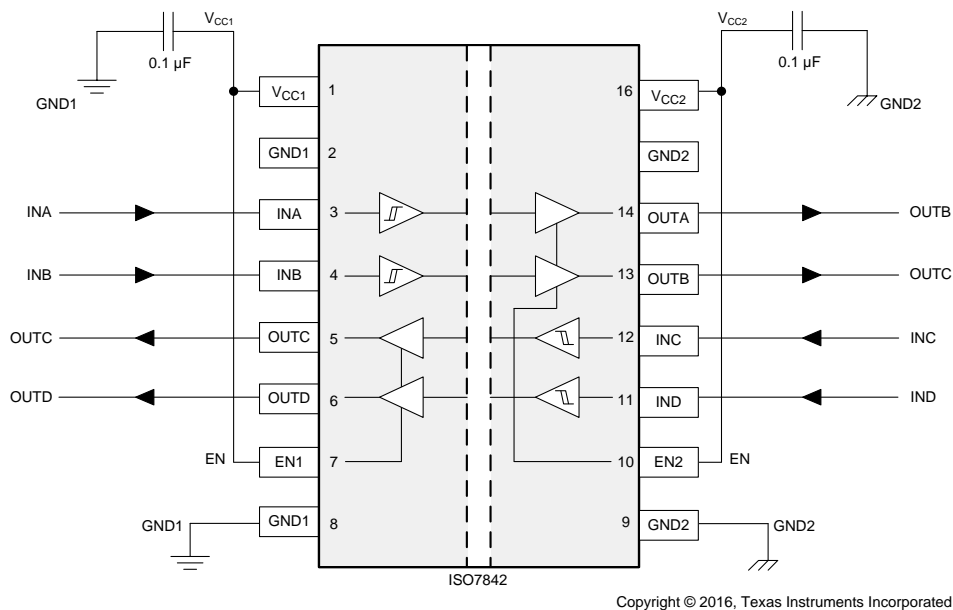
For this design example, use the parameters shown in [Table 8](#).

**Table 8. Design Parameters**

PARAMETER	VALUE
Supply voltage	2.25 to 5.5 V
Decoupling capacitor between $V_{CC1}$ and GND1	0.1 $\mu$ F
Decoupling capacitor from $V_{CC2}$ and GND2	0.1 $\mu$ F

### 9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7842 device only requires two external bypass capacitors to operate.



**Figure 19. Typical ISO7842 Circuit Hook-Up**

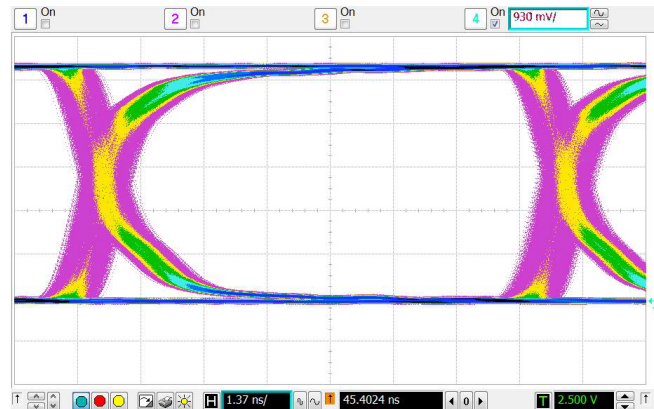
#### 9.2.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge, and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7842 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

### 9.2.3 Application Curve

The typical eye diagram of the ISO7842 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.



**Figure 20. Eye Diagram at 100 Mbps PRBS, 5 V and 25°C**

## 10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments [SN6501](#). For such applications, detailed power supply design and transformer selection recommendations are available in the [SN6501](#) data sheet ([SLLSEAO](#)).

## 11 Layout

### 11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 21](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the application note, *Digital Isolator Design Guide* ([SLLA284](#)).

#### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

### 11.2 Layout Example

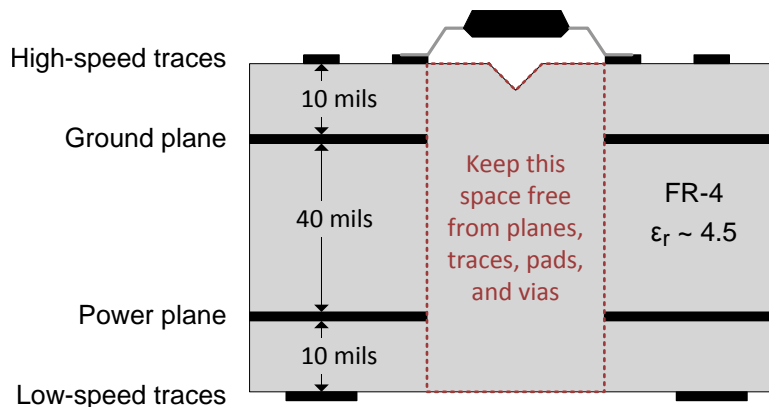


Figure 21. Layout Example Schematic

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

相关文档如下：

- 《数字隔离器设计指南》， [SLLA284](#)
- 《隔离相关术语》， [SLLA353](#)
- 《LP2985 具有关断模式的 150mA 低噪声低压降滤波器》， [SLVS522](#)
- 《MSP430G2x32、MSP430G2x02 混合信号微控制器》， [SLAS723](#)
- 《SN6501 用于隔离电源的变压器驱动器》， [SLLSEA0](#)
- 《TRS232 具有 IEC61000-4-2 保护的双路 RS-232 驱动器/接收器》， [SLLS861](#)

### 12.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 9. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ISO7842	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
ISO7842F	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 12.3 社区资源

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

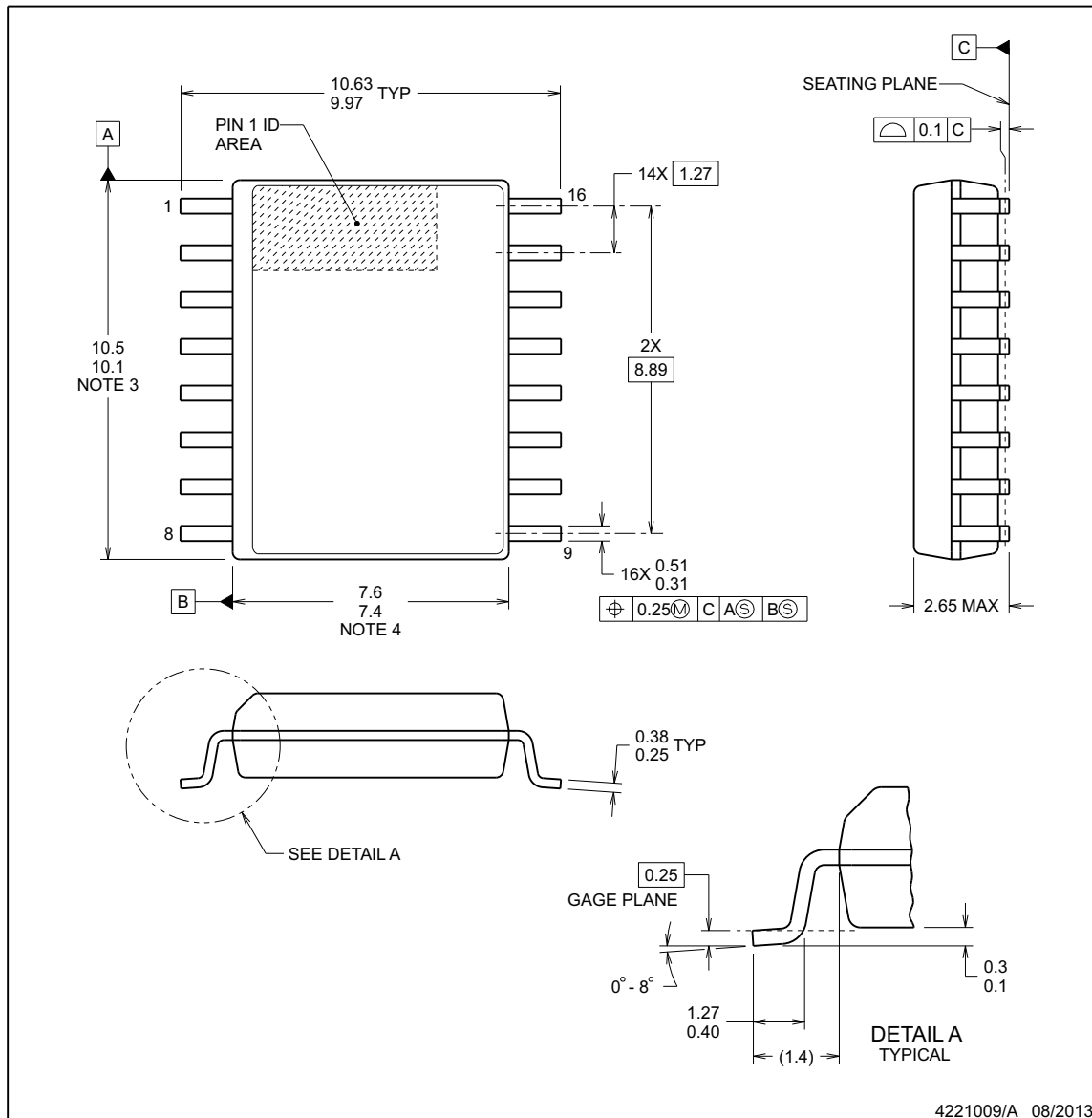
## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGE OUTLINE**

**DW0016B**
**SOIC - 2.65 mm max height**

SOIC


**NOTES:**

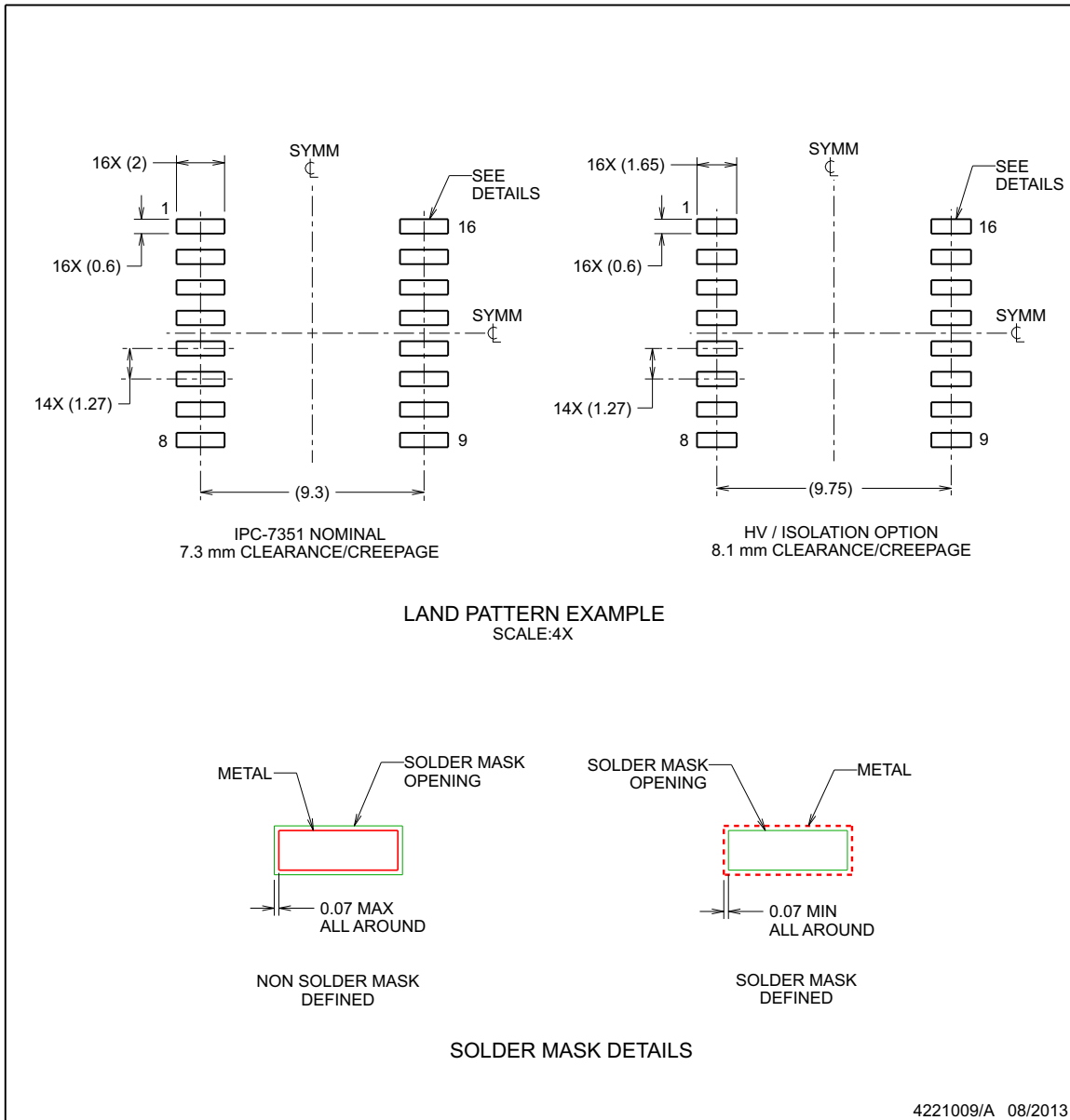
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.

## EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

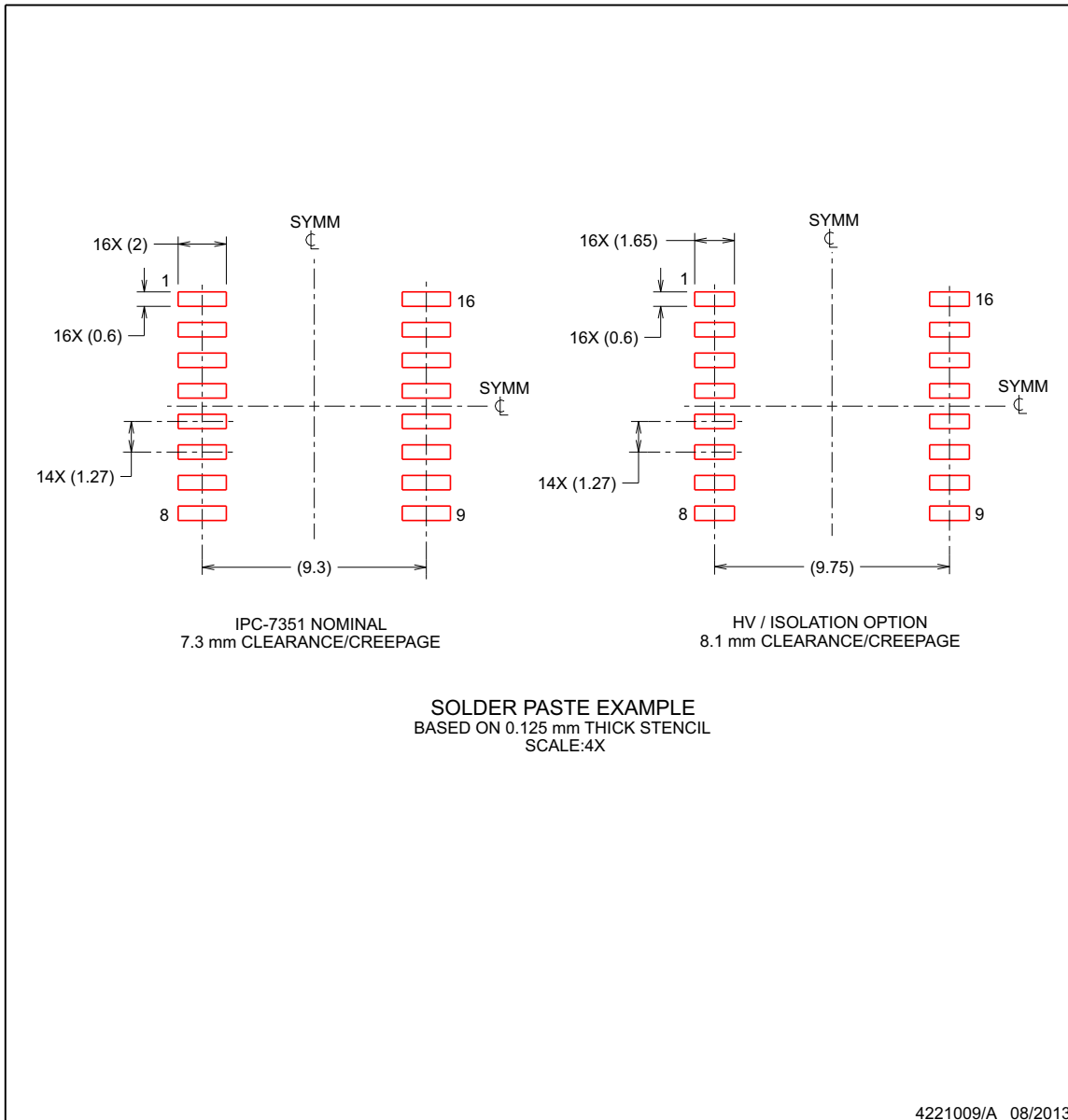
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN**

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

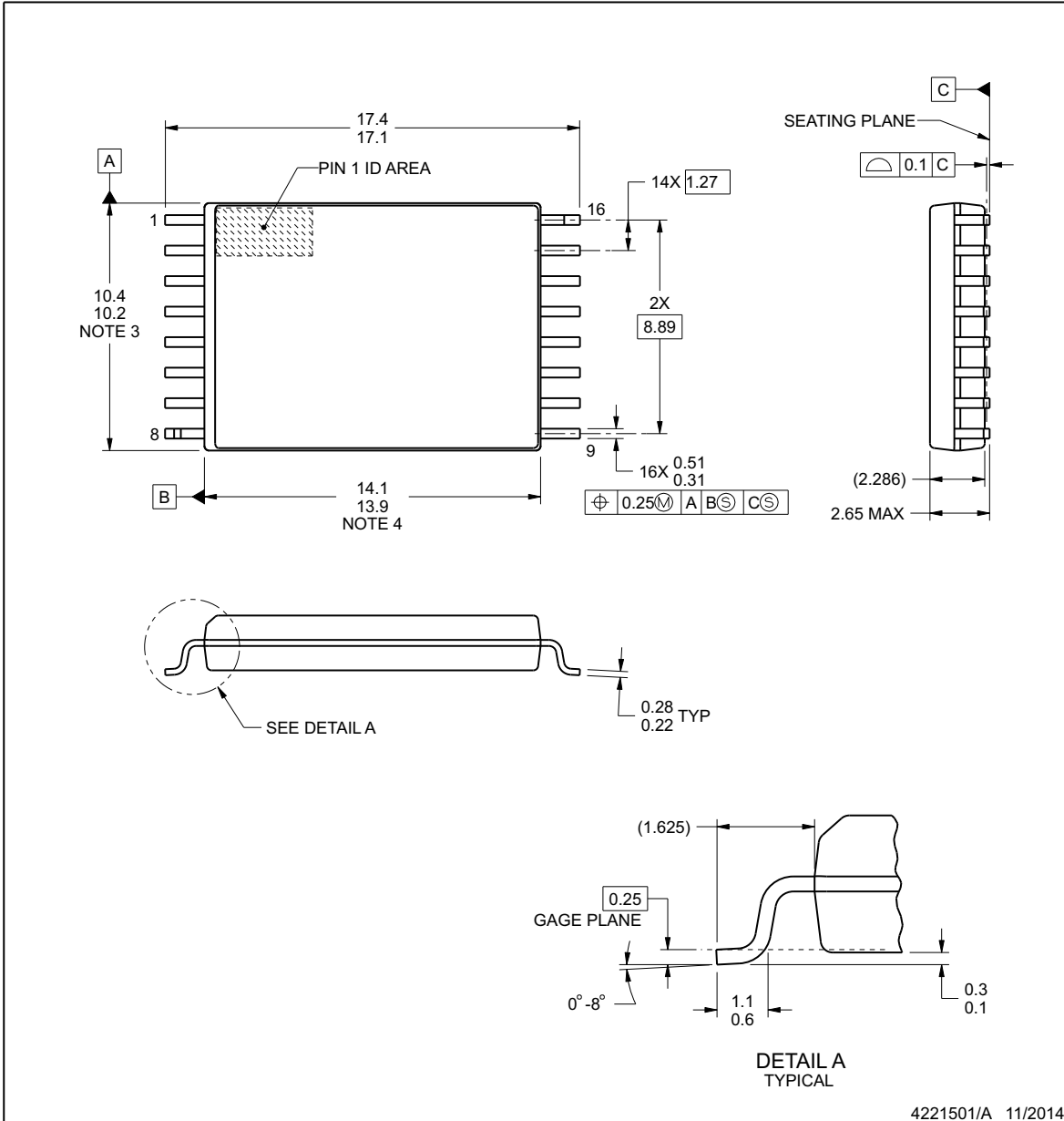


**DWW0016A**

**PACKAGE OUTLINE**

**SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



**NOTES:**

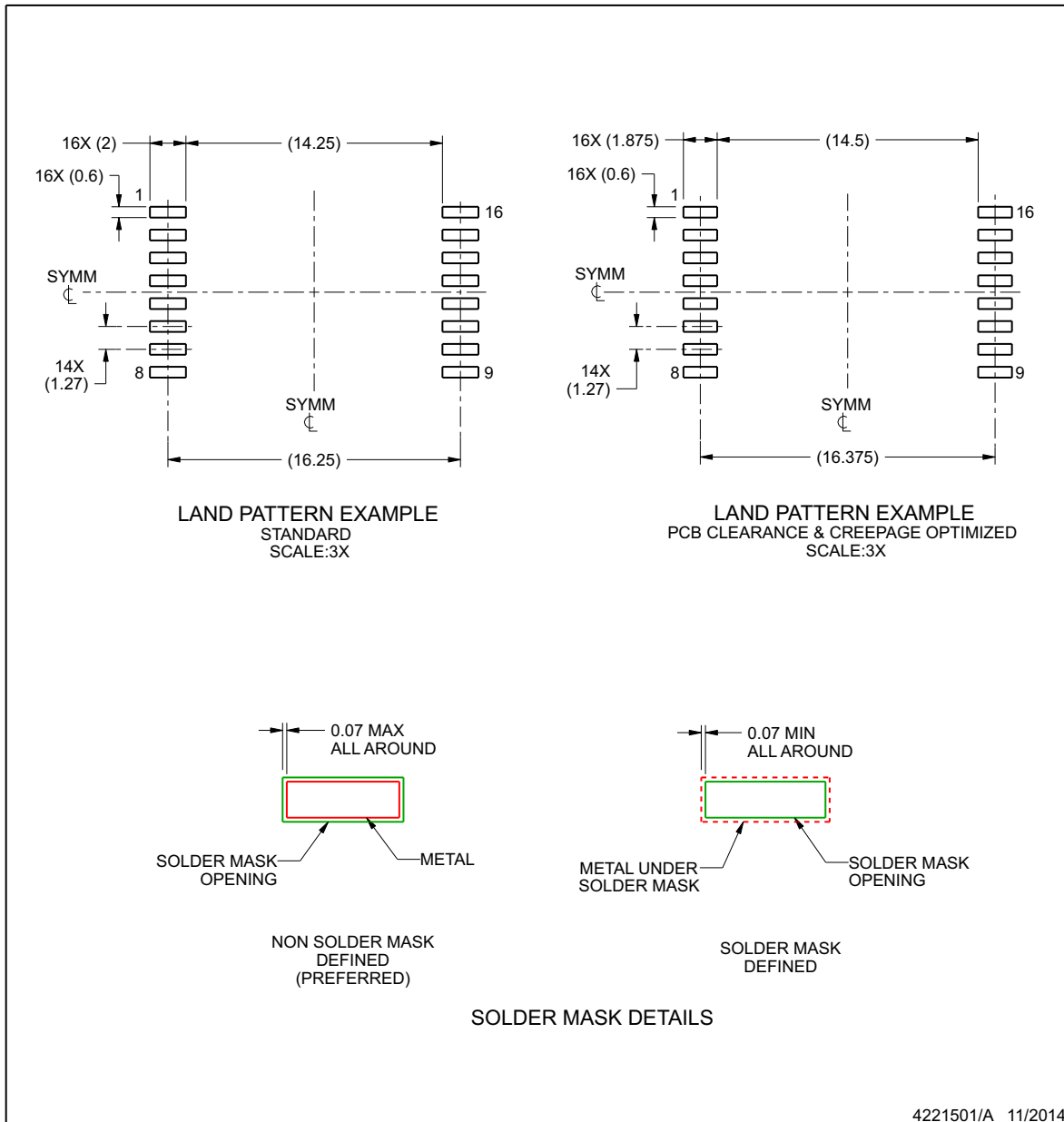
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash.

**EXAMPLE BOARD LAYOUT**

**DWW0016A**

**SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

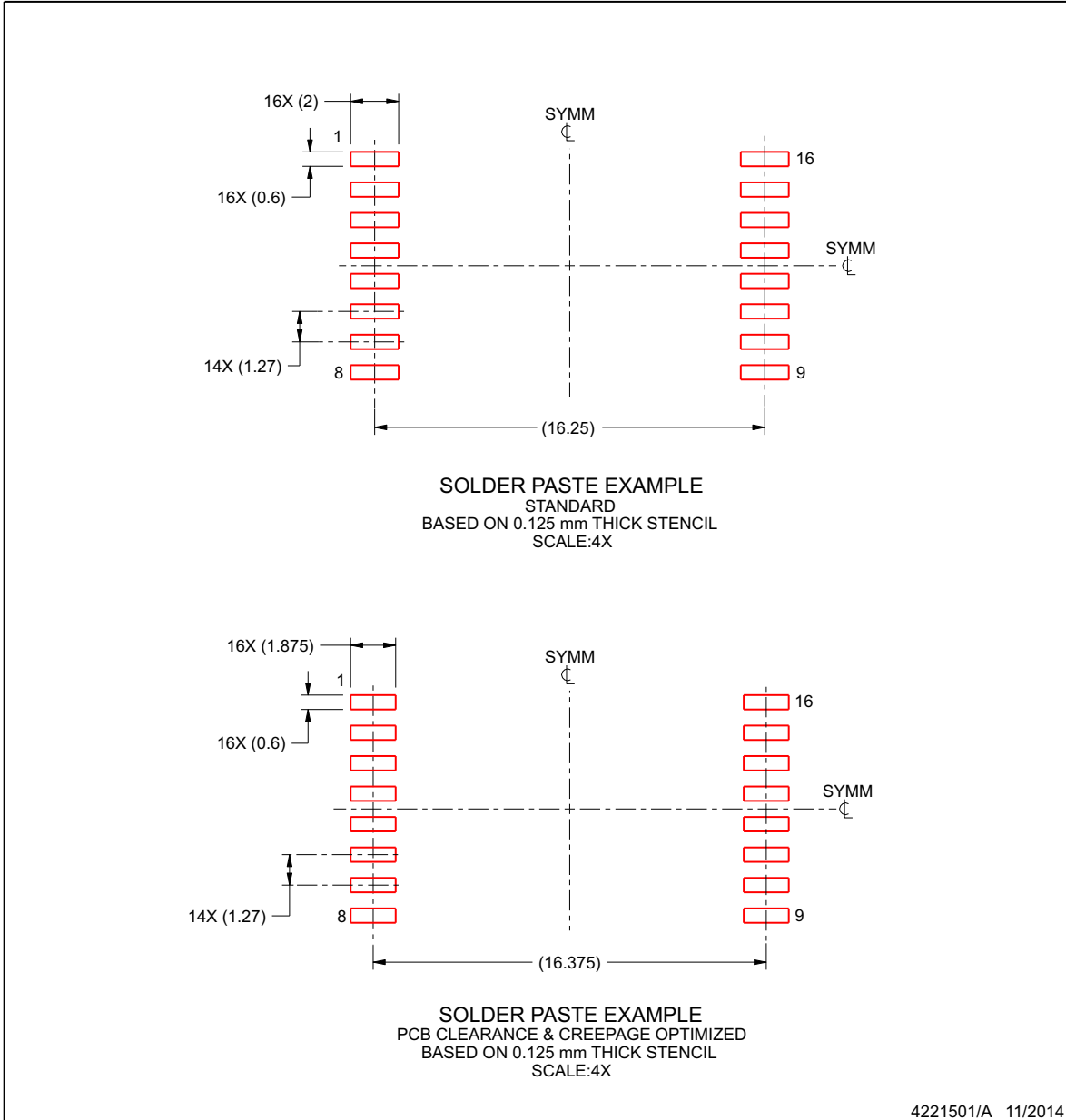
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN**

**DWW0016A**

**SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

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放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
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DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
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逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
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OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7842DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842	<a href="#">Samples</a>
ISO7842DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842	<a href="#">Samples</a>
ISO7842DWW	ACTIVE	SOIC	DWW	16	45	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842	<a href="#">Samples</a>
ISO7842DWWR	ACTIVE	SOIC	DWW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842	<a href="#">Samples</a>
ISO7842FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842F	<a href="#">Samples</a>
ISO7842FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842F	<a href="#">Samples</a>
ISO7842FDWW	ACTIVE	SOIC	DWW	16	45	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842F	<a href="#">Samples</a>
ISO7842FDWWR	ACTIVE	SOIC	DWW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7842F	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7842DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7842DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7842FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7842FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7842DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7842DWWR	SOIC	DWW	16	1000	367.0	367.0	45.0
ISO7842FDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7842FDWWR	SOIC	DWW	16	1000	367.0	367.0	45.0

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