

ISO774x High Speed, Robust EMC Reinforced Quad-Channel Digital Isolators

1 Features

- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level Translation
- Default Output *High* and *Low* Options
- Wide Temperature Range: –55°C to 125°C
- Low Power Consumption, Typical 1.5 mA per Channel at 1 Mbps
- Low Propagation Delay: 10.7 ns Typical (5-V Supplies)
- High CMTI: ± 75 kV/ μ s Typical
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: >40 Years
- Wide-SOIC (DW-16) and QSOP (DBQ-16) Package Options
- Safety-Related Certifications:
 - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
 - UL 1577 Component Recognition Program
 - CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 60601-1 and IEC 61010-1 End Equipment Standards
 - CQC Approval per GB4943.1-2011
 - TUV Certification according to EN 60950-1 and EN 61010-1
 - All Certifications are Planned

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

3 Description

The ISO774x devices are high-performance, quad-channel digital isolators with 5000 V_{RMS} (DW package) and 2500 V_{RMS} (DBQ package) isolation ratings per UL 1577. This family of devices has reinforced insulation ratings according to VDE, CSA, TUV and CQC.

The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO_2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7740 device has all four channels in the same direction, the ISO7741 device has three forward and one reverse-direction channels, and the ISO7742 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is *high* for devices without suffix F and *low* for devices with suffix F. See the [Device Functional Modes](#) section for further details.

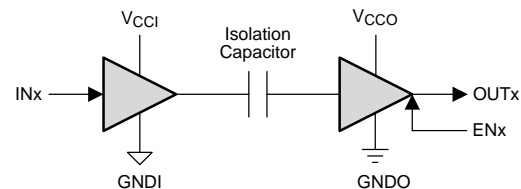
Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO774x family of devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO774x family of devices is available in 16-pin SOIC and QSOP packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7740	SOIC (DW)	10.30 mm × 7.50 mm
ISO7741	SSOP (DBQ)	4.90 mm × 3.90 mm
ISO7742		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Copyright © 2016, Texas Instruments Incorporated

V_{CCI} and $GNDI$ are supply and ground connections respectively for the input channels.

V_{CCO} and $GNDO$ are supply and ground connections respectively for the output channels.



Table of Contents

1 Features	1	6.19 Typical Characteristics	18
2 Applications	1	7 Parameter Measurement Information	20
3 Description	1	8 Detailed Description	22
4 Revision History	2	8.1 Overview	22
5 Pin Configuration and Functions	3	8.2 Functional Block Diagram	22
6 Specifications	5	8.3 Feature Description	23
6.1 Absolute Maximum Ratings	5	8.4 Device Functional Modes	24
6.2 ESD Ratings	5	9 Application and Implementation	25
6.3 Recommended Operating Conditions	5	9.1 Application Information	25
6.4 Thermal Information	6	9.2 Typical Application	25
6.5 Power Rating	6	10 Power Supply Recommendations	27
6.6 Insulation Specifications	7	11 Layout	28
6.7 Regulatory Information	8	11.1 Layout Guidelines	28
6.8 Safety Limiting Values	8	11.2 Layout Example	28
6.9 Electrical Characteristics—5-V Supply	9	12 Device and Documentation Support	29
6.10 Supply Current Characteristics—5-V Supply	10	12.1 Documentation Support	29
6.11 Electrical Characteristics—3.3-V Supply	11	12.2 Related Links	29
6.12 Supply Current Characteristics—3.3-V Supply	12	12.3 Receiving Notification of Documentation Updates	29
6.13 Electrical Characteristics—2.5-V Supply	13	12.4 Community Resources	29
6.14 Supply Current Characteristics—2.5-V Supply	14	12.5 Trademarks	29
6.15 Switching Characteristics—5-V Supply	15	12.6 Electrostatic Discharge Caution	29
6.16 Switching Characteristics—3.3-V Supply	16	12.7 Glossary	29
6.17 Switching Characteristics—2.5-V Supply	16	13 Mechanical, Packaging, and Orderable Information	30
6.18 Safety and Insulation Characteristics Curves	17		

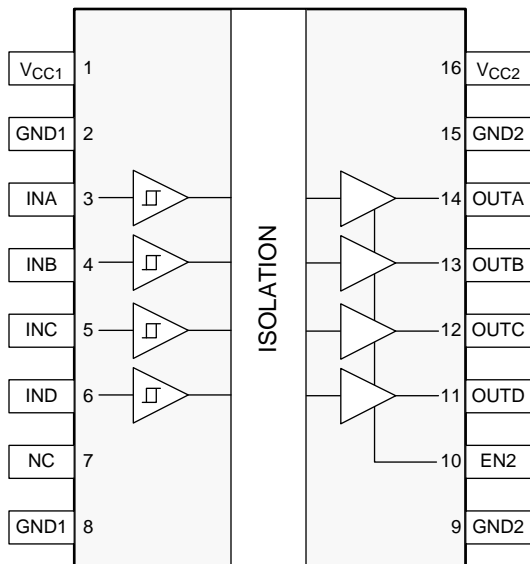
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

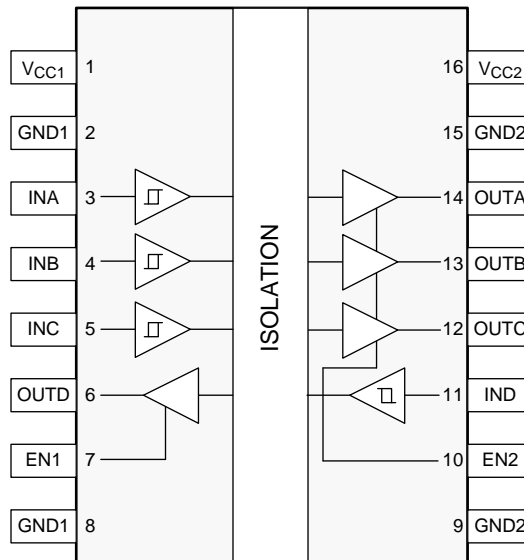
Changes from Original (March 2016) to Revision A	Page
• Changed the device status From: Preview To: Production	1

5 Pin Configuration and Functions

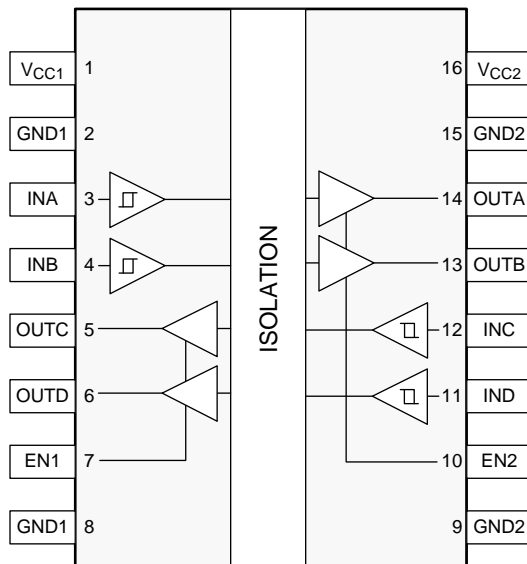
**ISO7740 DW and DBQ Packages
16-Pin SOIC-WB and QSOP
Top View**



**ISO7741 DW and DBQ Packages
16-Pin SOIC-WB and QSOP
Top View**



**ISO7742 DW and DBQ Packages
16-Pin SOIC-WB and QSOP
Top View**



Pin Functions

NAME	PIN			I/O	DESCRIPTION
	ISO7740	ISO7741	ISO7742		
V _{CC1}	1	1	1	—	Power supply, side 1
V _{CC2}	16	16	16	—	Power supply, side 2
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
EN1	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
NC	7	—	—	—	Not connected
GND1	2	2	2	—	Ground connection for V _{CC1}
	8	8	8		
GND2	9	9	9	—	Ground connection for V _{CC2}
	15	15	15		

6 Specifications

6.1 Absolute Maximum Ratings

 See ⁽¹⁾

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage ⁽²⁾	-0.5	6	V
V	Voltage at INx, OUTx, ENx	-0.5	$V_{CCX} + 0.5^{(3)}$	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±6000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500
			V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising		2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling	1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis	100	200		mV
I_{OH}	High-level output current	$V_{CCO}^{(1)} = 5\text{ V}$		-4	mA
		$V_{CCO} = 3.3\text{ V}$		-2	
		$V_{CCO} = 2.5\text{ V}$		-1	
I_{OL}	Low-level output current	$V_{CCO} = 5\text{ V}$		4	mA
		$V_{CCO} = 3.3\text{ V}$		2	
		$V_{CCO} = 2.5\text{ V}$		1	
V_{IH}	High-level input voltage	$0.7 \times V_{CCI}^{(1)}$		V_{CCI}	V
V_{IL}	Low-level input voltage	0		$0.3 \times V_{CCI}$	V
DR	Data rate	0		100	Mbps
T_A	Ambient temperature	-55	25	125	°C

- (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO774x		UNIT
		DW (SOIC)	DBQ (QSOP)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	109.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.0	54.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.0	51.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.1	14.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.5	51.4	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Rating

PARAMETER	TEST CONDITIONS	VALUE	UNIT
ISO7740			
P_D	Maximum power dissipation	200	mW
P_{D1}	Maximum power dissipation by side-1	40	mW
P_{D2}	Maximum power dissipation by side-2	160	mW
ISO7741			
P_D	Maximum power dissipation	200	mW
P_{D1}	Maximum power dissipation by side-1	50	mW
P_{D2}	Maximum power dissipation by side-2	150	mW
ISO7742			
P_D	Maximum power dissipation	200	mW
P_{D1}	Maximum power dissipation by side-1	100	mW
P_{D2}	Maximum power dissipation by side-2	100	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	DBQ-16	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	>3.7	μm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	>3.7	μm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	I-III	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	n/a	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	n/a	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12⁽²⁾					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	566	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	1000	400	V _{RMS}
		DC voltage	1414	566	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} t = 60 s (qualification) t = 1 s (100% production)	8000	3600	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	8000	4000	V _{PK}
Q _{pd}	Apparent charge ⁽⁴⁾	Method a, After Input/Output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~1	~1	pF
R _{IO}	Isolation resistance ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	>10 ⁹	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5000	2500	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Regulatory Information

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Maximum transient isolation voltage, 8000 V _{PK} (DW-16) and 3600 V _{PK} (DBQ-16); Maximum repetitive peak isolation voltage, 1414 V _{PK} (DW-16) and 566 V _{PK} (DBQ-16); Maximum surge isolation voltage, 8000 V _{PK} (DW-16) and 4000 V _{PK} (DBQ-16)	Reinforced insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed., 600 V _{RMS} (DW-16) maximum working voltage; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V _{RMS} (DW-16) and 370 V _{RMS} (DBQ-16) max working voltage (pollution degree 2, material group I); DW-16: 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V _{RMS} (DW-16) max working voltage	DW-16: Single protection, 5000 V _{RMS} ; DBQ-16: Single protection, 2500 V _{RMS}	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V _{RMS} maximum working voltage; DBQ-16: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V _{RMS} maximum working voltage	5000 V _{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V _{RMS} (DW package) 5000 V _{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V _{RMS} (DW package)
Certification Planned	Certification Planned	Certification Planned	Certification Planned	Certification Planned

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE					
I _S Safety input, output, or supply current	R _{θJA} = 83.4 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 1			273	mA
	R _{θJA} = 83.4 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 1			416	
	R _{θJA} = 83.4 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 1			545	
P _S Safety input, output, or total power	R _{θJA} = 83.4 °C/W, T _J = 150°C, T _A = 25°C, see Figure 3			1499	mW
T _S Maximum safety temperature				150	°C
DBQ-16 PACKAGE					
I _S Safety input, output, or supply current	R _{θJA} = 109 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 2			209	mA
	R _{θJA} = 109 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 2			319	
	R _{θJA} = 109 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 2			417	
P _S Safety input, output, or total power	R _{θJA} = 109 °C/W, T _J = 150°C, T _A = 25°C, see Figure 4			1147	mW
T _S Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) is that of a device installed on a High-K test board for leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance

6.9 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4\text{ mA}$; see Figure 15	$V_{CCO}^{(1)} - 0.4$	4.8		V
V_{OL}	Low-level output voltage	$I_{OL} = 4\text{ mA}$; see Figure 15		0.2	0.4	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx or ENx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 18	40	75		$\text{kV}/\mu\text{s}$
C_I	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$		2		pF

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7740							
Supply current - Disable	EN2 = 0 V; $V_I = V_{CC1}$ (ISO7740); $V_I = 0\text{ V}$ (ISO7740 with F suffix)	I_{CC1}		1.2	1.6	mA	
		I_{CC2}		0.3	0.5		
	EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7740); $V_I = V_{CC1}$ (ISO7740 with F suffix)	I_{CC1}		5.5	7.8		
		I_{CC2}		0.3	0.5		
Supply current - DC signal	EN2 = V_{CC2} ; $V_I = V_{CC1}$ (ISO7740); $V_I = 0\text{ V}$ (ISO7740 with F suffix)	I_{CC1}		1.2	1.6		
		I_{CC2}		2	3.2		
	EN2 = V_{CC2} ; $V_I = 0\text{ V}$ (ISO7740); $V_I = V_{CC1}$ (ISO7740 with F suffix)	I_{CC1}		5.5	7.8		
		I_{CC2}		2.2	3.6		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.3	4.7	
			I_{CC2}		2.3	3.6	
		10 Mbps	I_{CC1}		3.4	4.8	
			I_{CC2}		4.2	5.8	
		100 Mbps	I_{CC1}		3.8	5.7	
			I_{CC2}		22.7	28	
ISO7741							
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CC1}^{(1)}$ (ISO7741); $V_I = 0\text{ V}$ (ISO7741 with F suffix)	I_{CC1}		1	1.5	mA	
		I_{CC2}		0.8	1.1		
	EN1 = EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7741); $V_I = V_{CC1}$ (ISO7741 with F suffix)	I_{CC1}		4.3	6.3		
		I_{CC2}		1.8	2.7		
Supply current - DC signal	EN1 = EN2 = V_{CC1} ; $V_I = V_{CC1}$ (ISO7741); $V_I = 0\text{ V}$ (ISO7741 with F suffix)	I_{CC1}		1.5	2.3		
		I_{CC2}		2	3		
	EN1 = EN2 = V_{CC1} ; $V_I = 0\text{ V}$ (ISO7741); $V_I = V_{CC1}$ (ISO7741 with F suffix)	I_{CC1}		4.8	6.8		
		I_{CC2}		3.2	4.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.2	4.6	
			I_{CC2}		2.8	4.1	
		10 Mbps	I_{CC1}		3.7	5.2	
			I_{CC2}		4.2	5.7	
		100 Mbps	I_{CC1}		8.6	11.3	
			I_{CC2}		18	22	
ISO7742							
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CC1}$ (ISO7742); $V_I = 0\text{ V}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		0.9	1.3	mA	
	EN1 = EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7742); $V_I = V_{CC1}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		3	4.6		
Supply current - DC signal	EN1 = EN2 = V_{CC1} ; $V_I = V_{CC1}$ (ISO7742); $V_I = 0\text{ V}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		1.7	2.7		
	EN1 = EN2 = V_{CC1} ; $V_I = 0\text{ V}$ (ISO7742); $V_I = V_{CC1}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		4	5.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		3		4.4
		10 Mbps	I_{CC1}, I_{CC2}		4		5.5
		100 Mbps	I_{CC1}, I_{CC2}		13.4	17	

 (1) V_{CC1} = Input-side V_{CC}

6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2 \text{ mA}$; see Figure 15	$V_{CCO}^{(1)} - 0.3$	3.2		V
V_{OL}	Low-level output voltage	$I_{OL} = 2 \text{ mA}$; see Figure 15		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx or ENx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$; see Figure 18	40	75		$\text{kV}/\mu\text{s}$

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.12 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7740							
Supply current - Disable	EN2 = 0 V; $V_I = V_{CC1}$ (ISO7740); $V_I = 0\text{ V}$ (ISO7740 with F suffix)	I_{CC1}		1.2	1.6	mA	
		I_{CC2}		0.3	0.5		
	EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7740); $V_I = V_{CC1}$ (ISO7740 with F suffix)	I_{CC1}		5.5	7.8		
		I_{CC2}		0.3	0.5		
Supply current - DC signal	EN2 = V_{CC2} ; $V_I = V_{CC1}$ (ISO7740); $V_I = 0\text{ V}$ (ISO7740 with F suffix)	I_{CC1}		1.2	1.6		
		I_{CC2}		1.9	3.2		
	EN2 = V_{CC2} ; $V_I = 0\text{ V}$ (ISO7740); $V_I = V_{CC1}$ (ISO7740 with F suffix)	I_{CC1}		5.5	7.8		
		I_{CC2}		2.2	3.6		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.3		4.7
			I_{CC2}		2.2		3.6
		10 Mbps	I_{CC1}		3.4		4.8
			I_{CC2}		3.6		5
		100 Mbps	I_{CC1}		3.3	5.5	
			I_{CC2}		17	20	
ISO7741							
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CCI}^{(1)}$ (ISO7741); $V_I = 0\text{ V}$ (ISO7741 with F suffix)	I_{CC1}		1	1.5	mA	
		I_{CC2}		0.8	1.1		
	EN1 = EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7741); $V_I = V_{CCI}$ (ISO7741 with F suffix)	I_{CC1}		4.3	6.3		
		I_{CC2}		1.9	2.7		
Supply current - DC signal	EN1 = EN2 = V_{CCI} ; $V_I = V_{CCI}$ (ISO7741); $V_I = 0\text{ V}$ (ISO7741 with F suffix)	I_{CC1}		1.5	2.3		
		I_{CC2}		2	3		
	EN1 = EN2 = V_{CCI} ; $V_I = 0\text{ V}$ (ISO7741); $V_I = V_{CCI}$ (ISO7741 with F suffix)	I_{CC1}		4.8	6.8		
		I_{CC2}		3.2	4.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.2		4.6
			I_{CC2}		2.7		4.1
		10 Mbps	I_{CC1}		3.5		5
			I_{CC2}		3.7		5.2
		100 Mbps	I_{CC1}		6.8	9.3	
			I_{CC2}		13.7	16.4	
ISO7742							
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CCI}$ (ISO7742); $V_I = 0\text{ V}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		0.9	1.3	mA	
	EN1 = EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7742); $V_I = V_{CCI}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		3	4.6		
Supply current - DC signal	EN1 = EN2 = V_{CCI} ; $V_I = V_{CCI}$ (ISO7742); $V_I = 0\text{ V}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		1.7	2.7		
	EN1 = EN2 = V_{CCI} ; $V_I = 0\text{ V}$ (ISO7742); $V_I = V_{CCI}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		4	5.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		2.9		4.3
		10 Mbps	I_{CC1}, I_{CC2}		3.6		5.1
		100 Mbps	I_{CC1}, I_{CC2}		10.3		13

 (1) V_{CCI} = Input-side V_{CC}

6.13 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$; see Figure 15	$V_{CCO}^{(1)} - 0.2$	2.45		V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$; see Figure 15		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx or ENx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx or ENx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 18	40	75		$\text{kV}/\mu\text{s}$

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7740							
Supply current - Disable	EN2 = 0 V; $V_I = V_{CC1}$ (ISO7740); $V_I = 0\text{ V}$ (ISO7740 with F suffix)	I_{CC1}		1.2	1.6	mA	
		I_{CC2}		0.3	0.5		
	EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7740); $V_I = V_{CC1}$ (ISO7740 with F suffix)	I_{CC1}		5.5	7.8		
		I_{CC2}		0.3	0.5		
Supply current - DC signal	EN2 = V_{CC2} ; $V_I = V_{CC1}$ (ISO7740); $V_I = 0\text{ V}$ (ISO7740 with F suffix)	I_{CC1}		1.2	1.6		
		I_{CC2}		1.9	3.2		
	EN2 = V_{CC2} ; $V_I = 0\text{ V}$ (ISO7740); $V_I = V_{CC1}$ (ISO7740 with F suffix)	I_{CC1}		5.4	7.8		
		I_{CC2}		2.2	3.6		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.3	4.7	
			I_{CC2}		2.2	3.5	
		10 Mbps	I_{CC1}		3.4	4.8	
			I_{CC2}		3.2	4.7	
		100 Mbps	I_{CC1}		3.2	5.4	
			I_{CC2}		13	17	
ISO7741							
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CCI}^{(1)}$ (ISO7741); $V_I = 0\text{ V}$ (ISO7741 with F suffix)	I_{CC1}		1	1.5	mA	
		I_{CC2}		0.8	1.1		
	EN1 = EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7741); $V_I = V_{CCI}$ (ISO7741 with F suffix)	I_{CC1}		4.3	6.3		
		I_{CC2}		1.8	2.7		
Supply current - DC signal	EN1 = EN2 = V_{CCI} ; $V_I = V_{CCI}$ (ISO7741); $V_I = 0\text{ V}$ (ISO7741 with F suffix)	I_{CC1}		1.4	2.3		
		I_{CC2}		2	3		
	EN1 = EN2 = V_{CCI} ; $V_I = 0\text{ V}$ (ISO7741); $V_I = V_{CCI}$ (ISO7741 with F suffix)	I_{CC1}		4.7	6.8		
		I_{CC2}		3.2	4.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		3.1	4.6	
			I_{CC2}		2.7	4	
		10 Mbps	I_{CC1}		3.4	4.9	
			I_{CC2}		3.5	4.9	
		100 Mbps	I_{CC1}		5.6	8.3	
			I_{CC2}		10.8	13.8	
ISO7742							
Supply current - Disable	EN1 = EN2 = 0 V; $V_I = V_{CCI}$ (ISO7742); $V_I = 0\text{ V}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		0.9	1.3	mA	
	EN1 = EN2 = 0 V; $V_I = 0\text{ V}$ (ISO7742); $V_I = V_{CCI}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		3	4.6		
Supply current - DC signal	EN1 = EN2 = V_{CCI} ; $V_I = V_{CCI}$ (ISO7742); $V_I = 0\text{ V}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		1.7	2.7		
	EN1 = EN2 = V_{CCI} ; $V_I = 0\text{ V}$ (ISO7742); $V_I = V_{CCI}$ (ISO7742 with F suffix)	I_{CC1}, I_{CC2}		4	5.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		2.9		4.3
		10 Mbps	I_{CC1}, I_{CC2}		3.4		4.9
		100 Mbps	I_{CC1}, I_{CC2}		8.3	11.5	

 (1) V_{CCI} = Input-side V_{CC}

6.15 Switching Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 15	6	10.7	16	ns	
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $		0		4.9	ns	
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4	ns	
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.4	ns	
t_r	Output signal rise time	See Figure 15		2.4	3.9	ns	
t_f	Output signal fall time			2.4	3.9	ns	
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 16		9	20	ns	
t_{PLZ}	Disable propagation delay, low-to-high impedance output			9	20	ns	
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO774x				7	20	ns
	Enable propagation delay, high impedance-to-high output for ISO774x with F suffix				3	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO774x				3	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO774x with F suffix				7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 17		6	9	μs	
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.80		ns	

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 15	6	11	16	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $		0.1		5	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.5	ns
t_r	Output signal rise time	See Figure 15		1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 16		17	30	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO774x			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO774x with F suffix			3.2	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO774x			3.2	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO774x with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 17		6	9	μs
t_e	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.90		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 15	7.5	12	18.5	ns
PWD	Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $		0.2		5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time ⁽²⁾	Same-direction Channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time ⁽³⁾				4.6	ns
t_r	Output signal rise time	See Figure 15		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 16		22	40	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO774x			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO774x with F suffix			3.3	8.5	μs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO774x			3.3	8.5	μs
	Enable propagation delay, high impedance-to-low output for ISO774x with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 17		6	9	μs
t_e	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		0.7		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Safety and Insulation Characteristics Curves

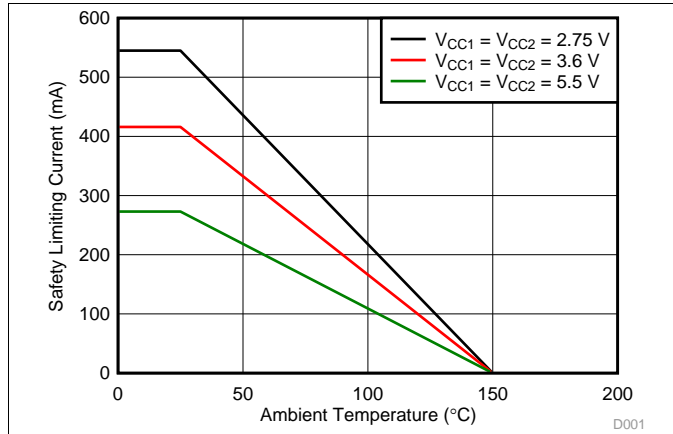


Figure 1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

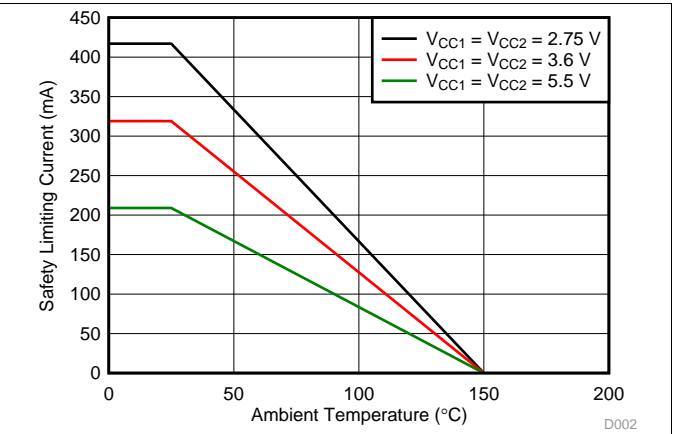


Figure 2. Thermal Derating Curve for Safety Limiting Current for DBQ-16 Package

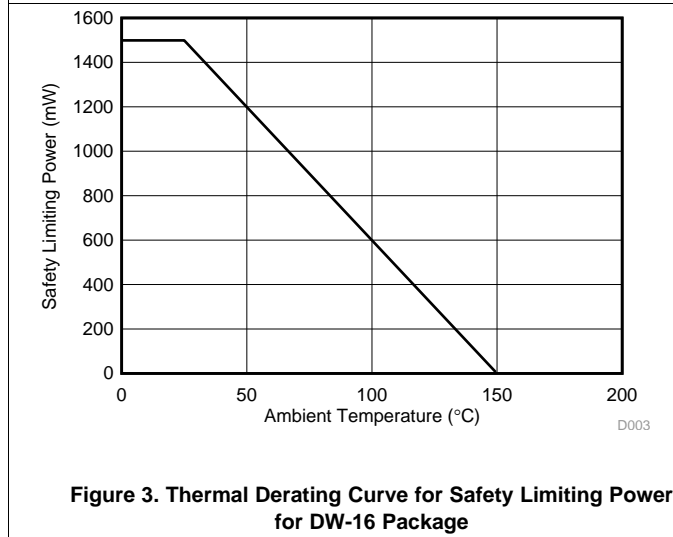


Figure 3. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

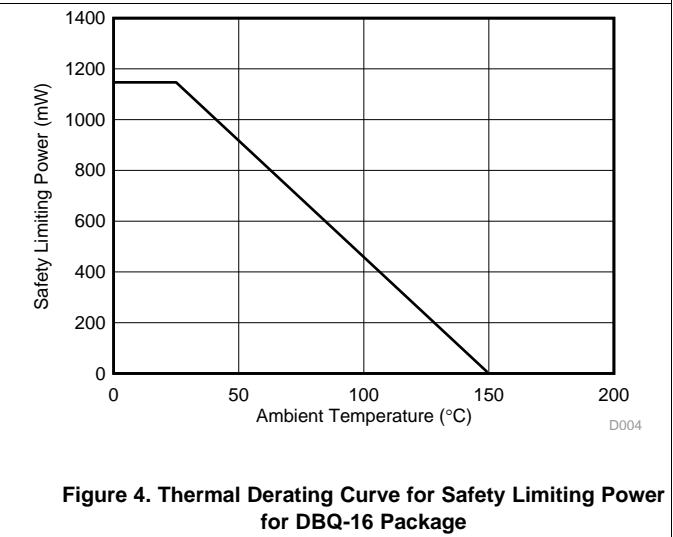
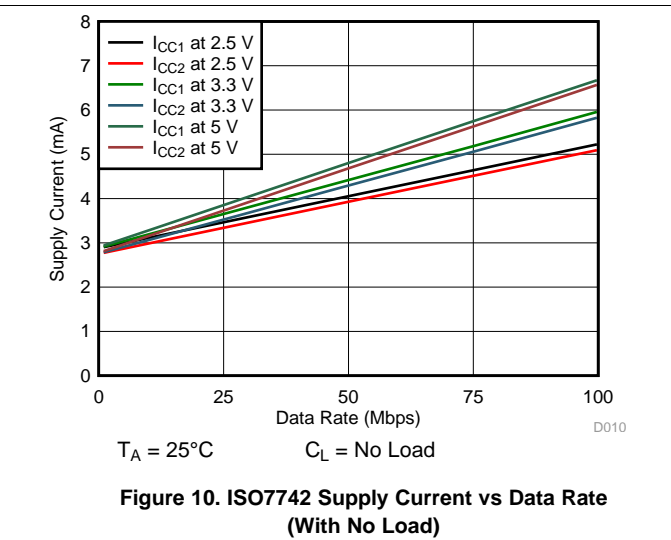
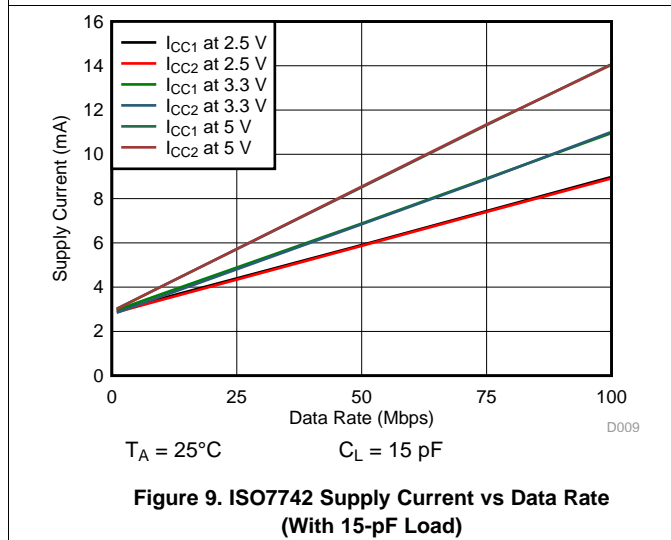
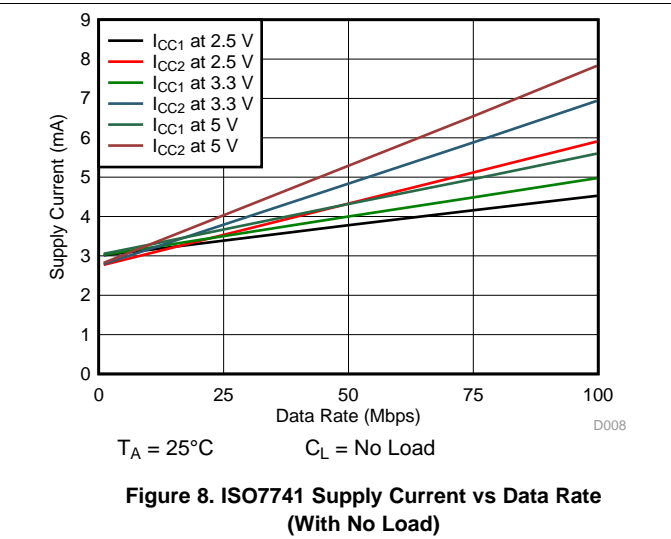
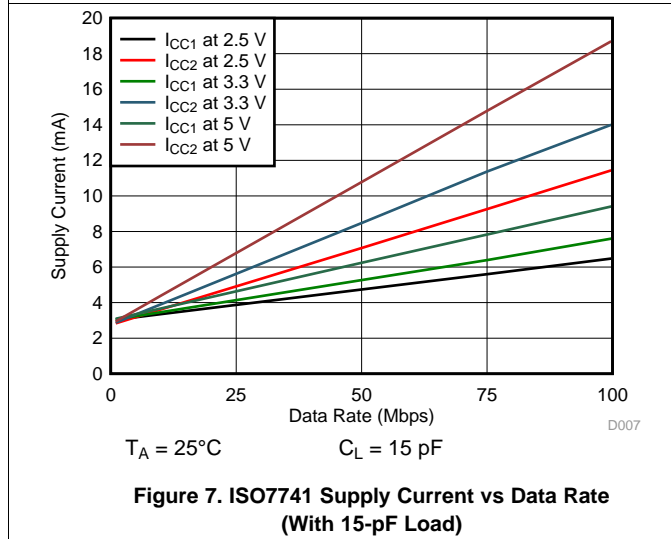
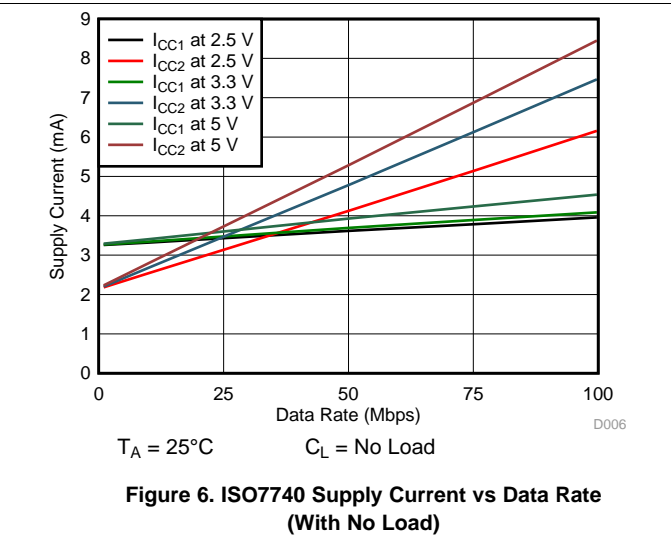
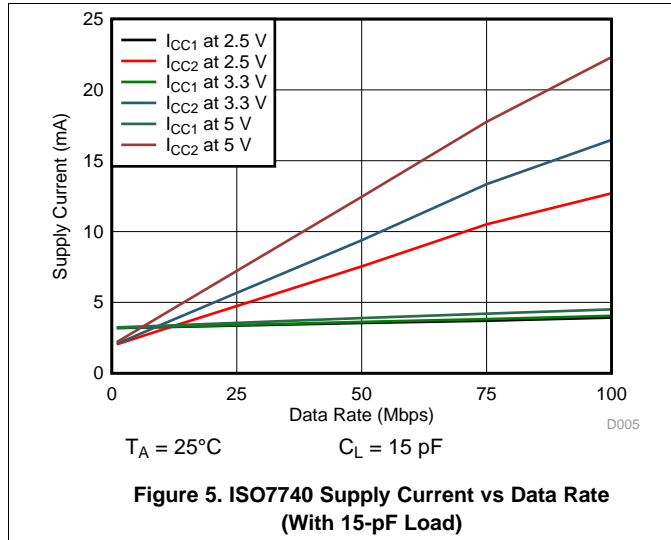


Figure 4. Thermal Derating Curve for Safety Limiting Power for DBQ-16 Package

6.19 Typical Characteristics



Typical Characteristics (continued)

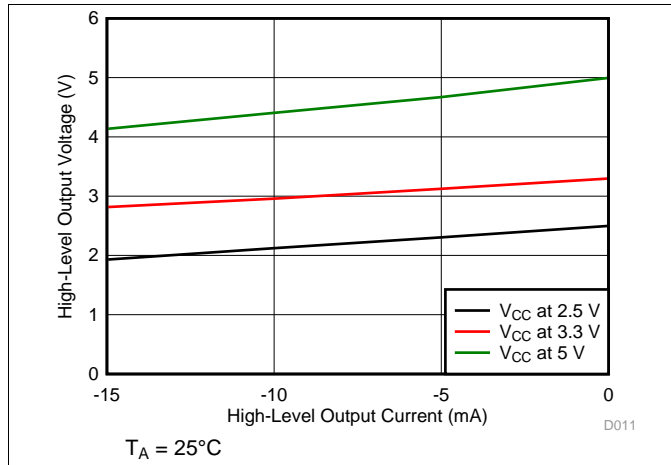


Figure 11. High-Level Output Voltage vs High-level Output Current

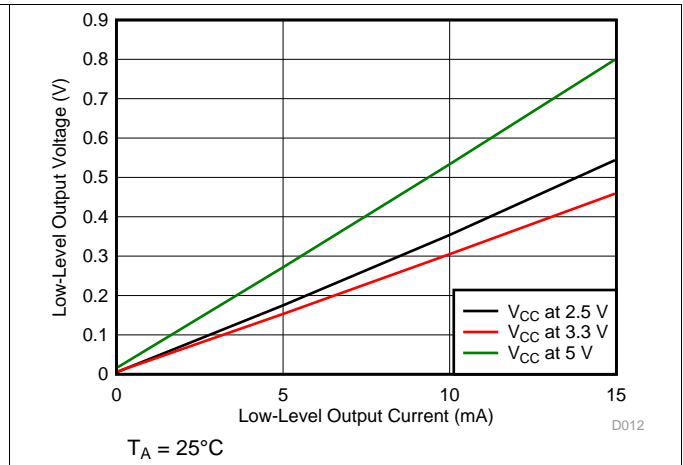


Figure 12. Low-Level Output Voltage vs Low-Level Output Current

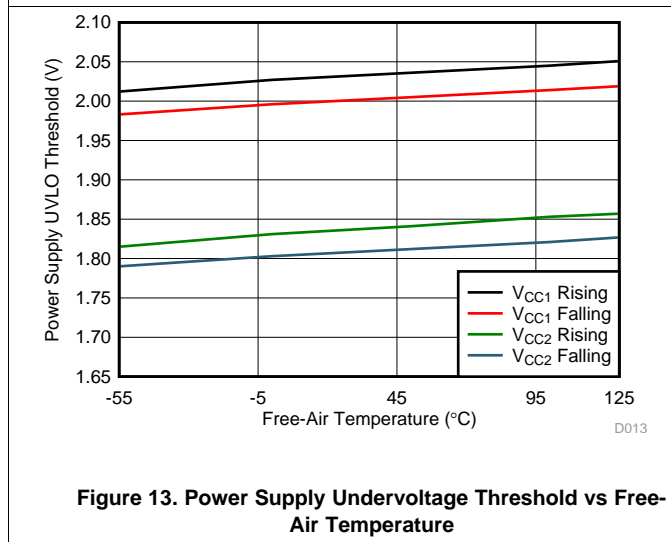


Figure 13. Power Supply Undervoltage Threshold vs Free-Air Temperature

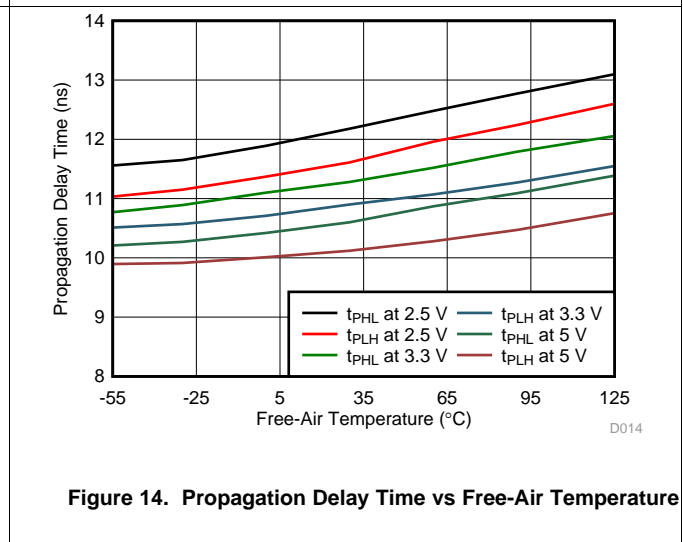
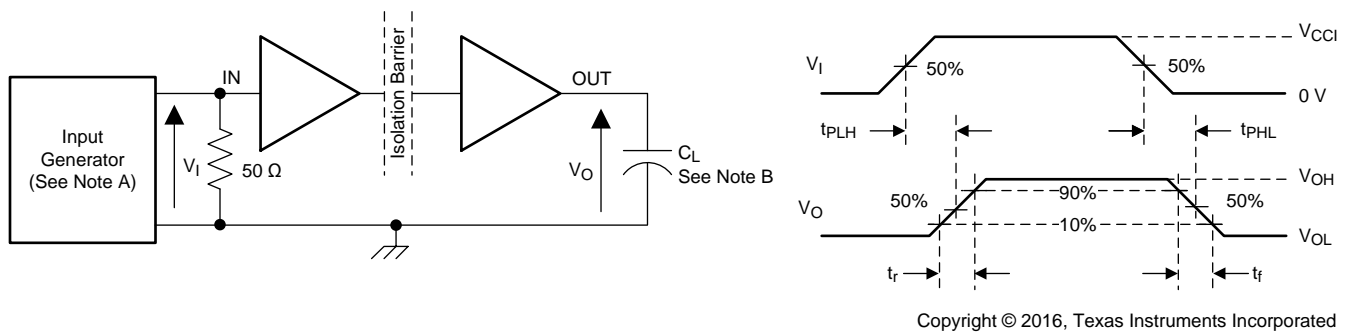


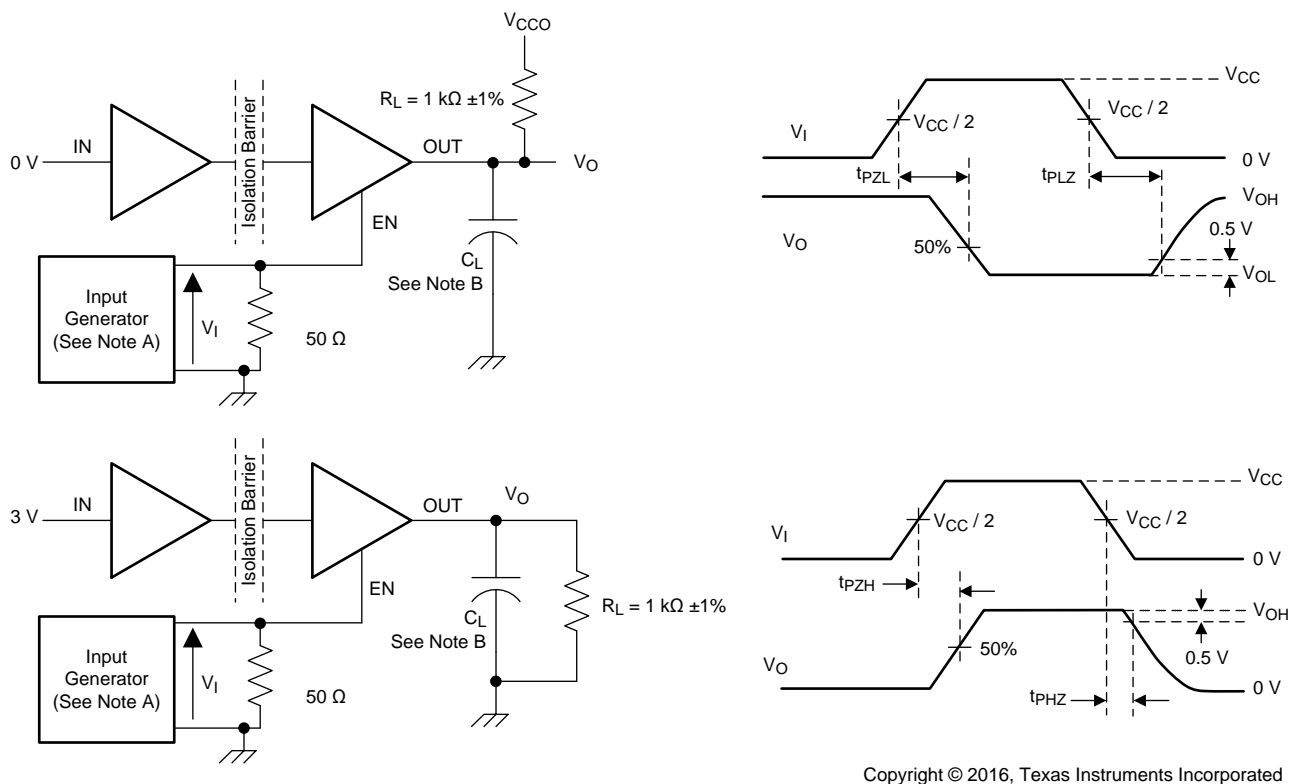
Figure 14. Propagation Delay Time vs Free-Air Temperature

7 Parameter Measurement Information



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50 \Omega$. At the input, 50Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

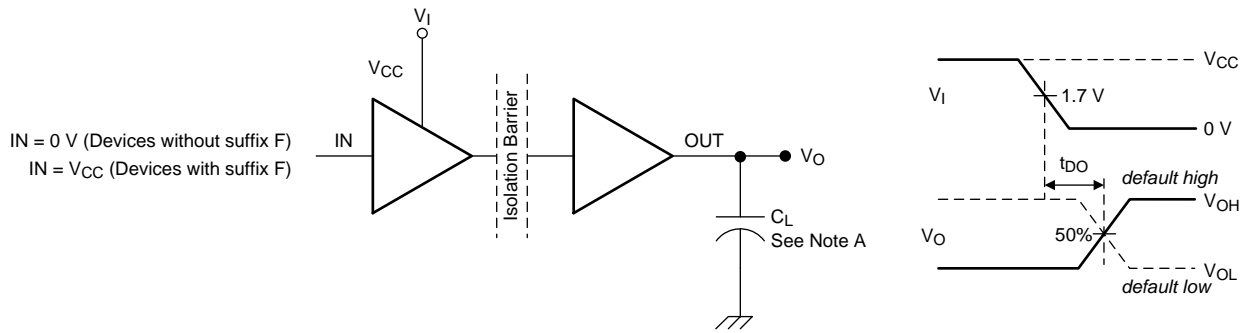
Figure 15. Switching Characteristics Test Circuit and Voltage Waveforms



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 10 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50 \Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 16. Enable/Disable Propagation Delay Time Test Circuit and Waveform

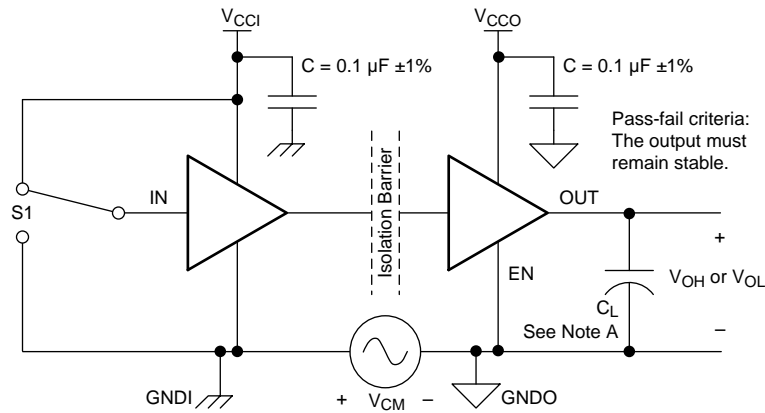
Parameter Measurement Information (continued)



Copyright © 2016, Texas Instruments Incorporated

- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 17. Default Output Delay Time Test Circuit and Voltage Waveforms



Copyright © 2016, Texas Instruments Incorporated

- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.

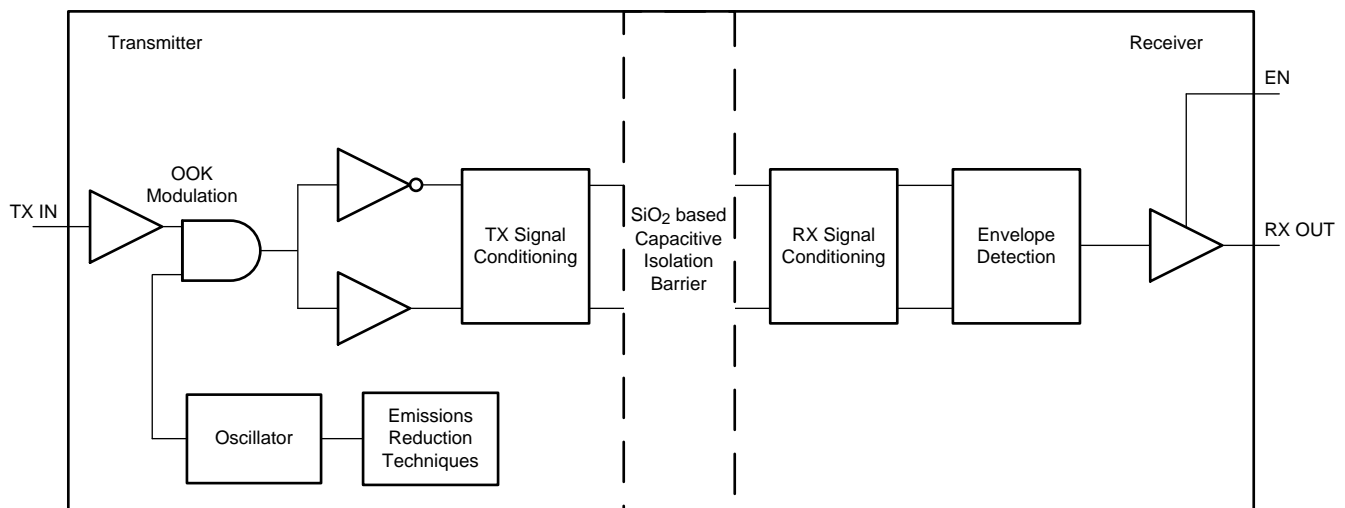
Figure 18. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO774x family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO774x devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 19](#), shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

Figure 19. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 20](#) shows a conceptual detail of how the ON/OFF keying scheme works.

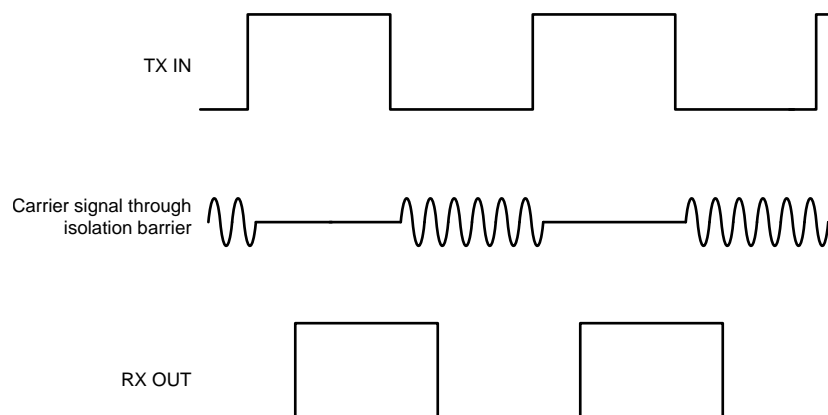


Figure 20. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 1 provides an overview of the device features.

Table 1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION ⁽¹⁾
ISO7740	4 Forward, 0 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DBQ-16	2500 V _{RMS} / 3600 V _{PK}
ISO7740 with F suffix	4 Forward, 0 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DBQ-16	2500 V _{RMS} / 3600 V _{PK}
ISO7741	3 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DBQ-16	2500 V _{RMS} / 3600 V _{PK}
ISO7741 with F suffix	3 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DBQ-16	2500 V _{RMS} / 3600 V _{PK}
ISO7742	2 Forward, 2 Reverse	100 Mbps	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DBQ-16	2500 V _{RMS} / 3600 V _{PK}
ISO7742 with F suffix	2 Forward, 2 Reverse	100 Mbps	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DBQ-16	2500 V _{RMS} / 3600 V _{PK}

(1) See [Regulatory Information](#) for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO774x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

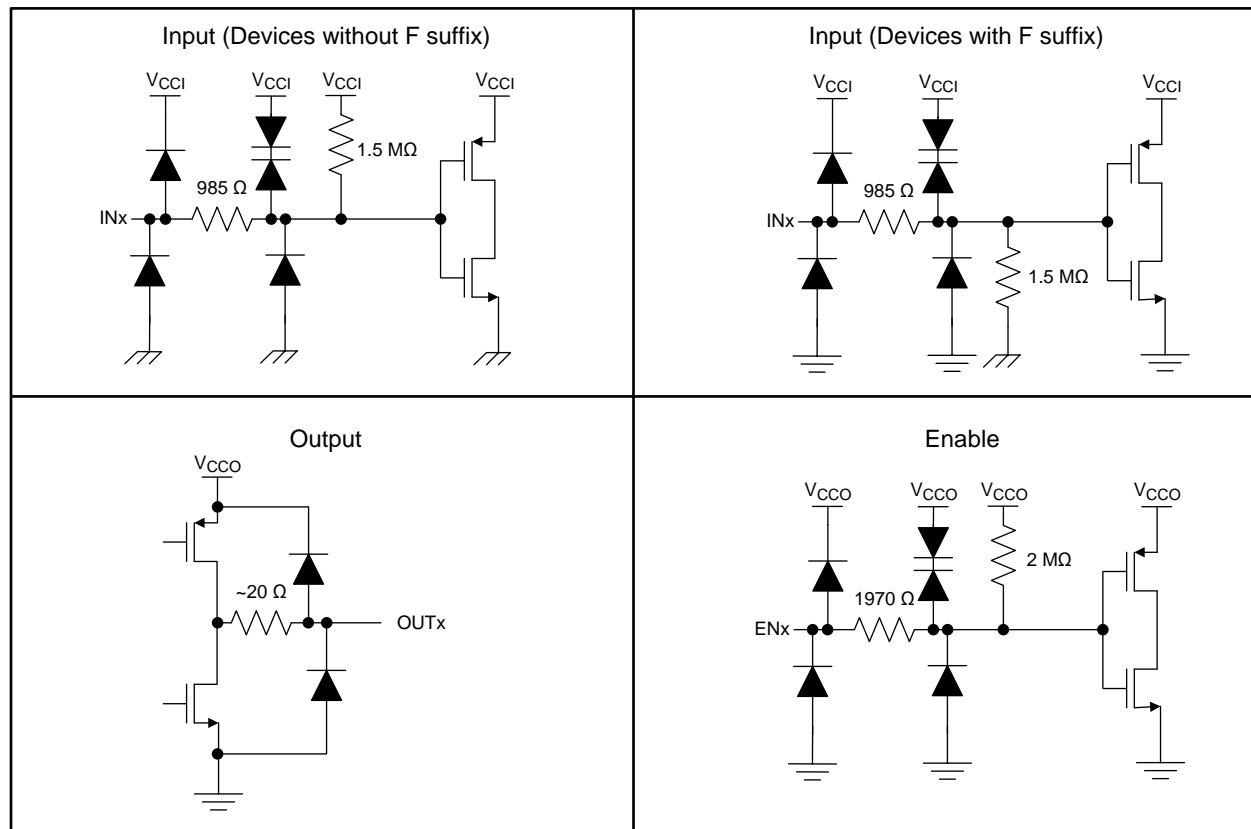
Table 2 lists the functional modes for the ISO774x devices.

Table 2. Function Table⁽¹⁾

V _{CCI}	V _{CCO}	INPUT (IN _x) ⁽²⁾	OUTPUT ENABLE (EN _x)	OUTPUT (OUT _x)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When IN _x is open, the corresponding channel output goes to its default logic state. Default= High for ISO774x and Low for ISO774x with F suffix.
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V _{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for ISO774x and Low for ISO774x with F suffix. When V _{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V _{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V _{CCO} is unpowered, a channel output is undetermined ⁽³⁾ . When V _{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

- (1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
- (2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.
- (3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics



Copyright © 2016, Texas Instruments Incorporated

Figure 21. Device I/O Schematics

9 Application and Implementation

NOTE

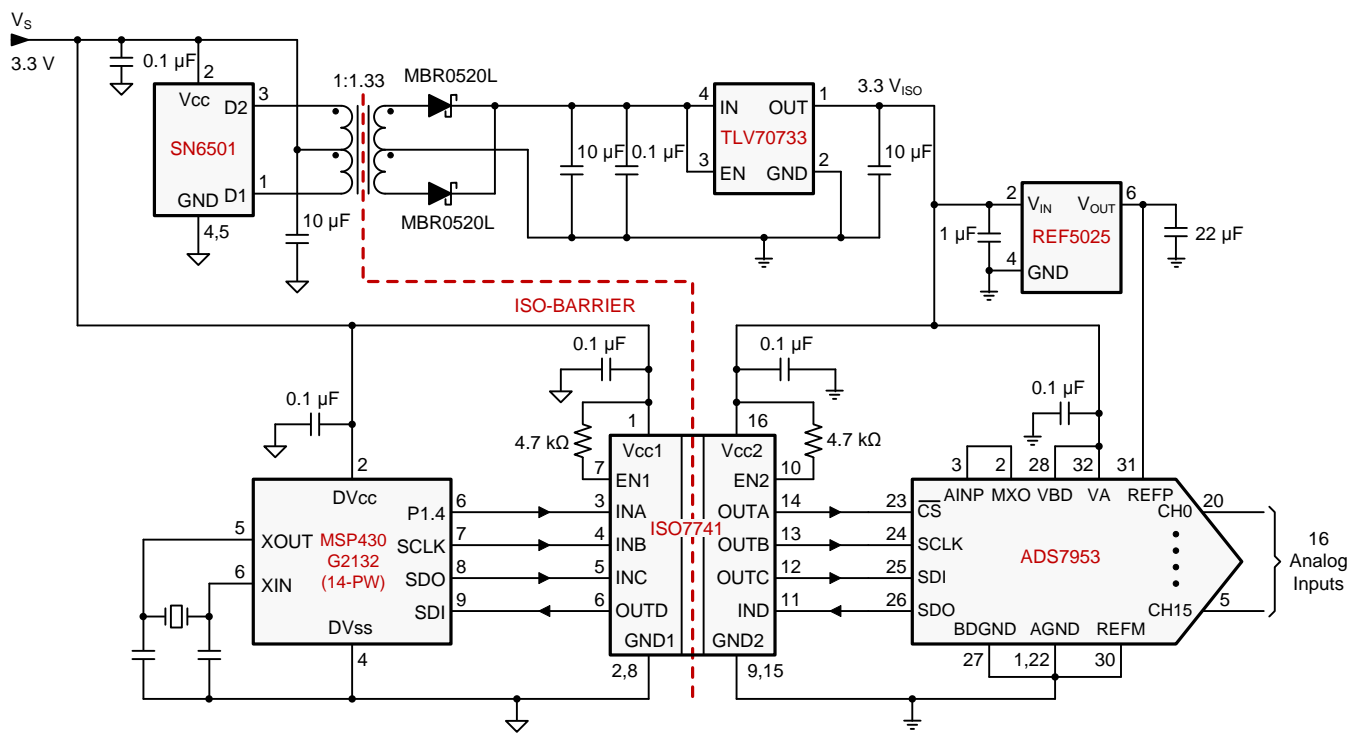
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO774x devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications and reduce power consumption. The ISO774x devices use single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Figure 22 shows the isolated serial peripheral interface (SPI).



Copyright © 2016, Texas Instruments Incorporated

Figure 22. Isolated SPI for an Analog Input Module With 16 Input

Typical Application (continued)

9.2.1 Design Requirements

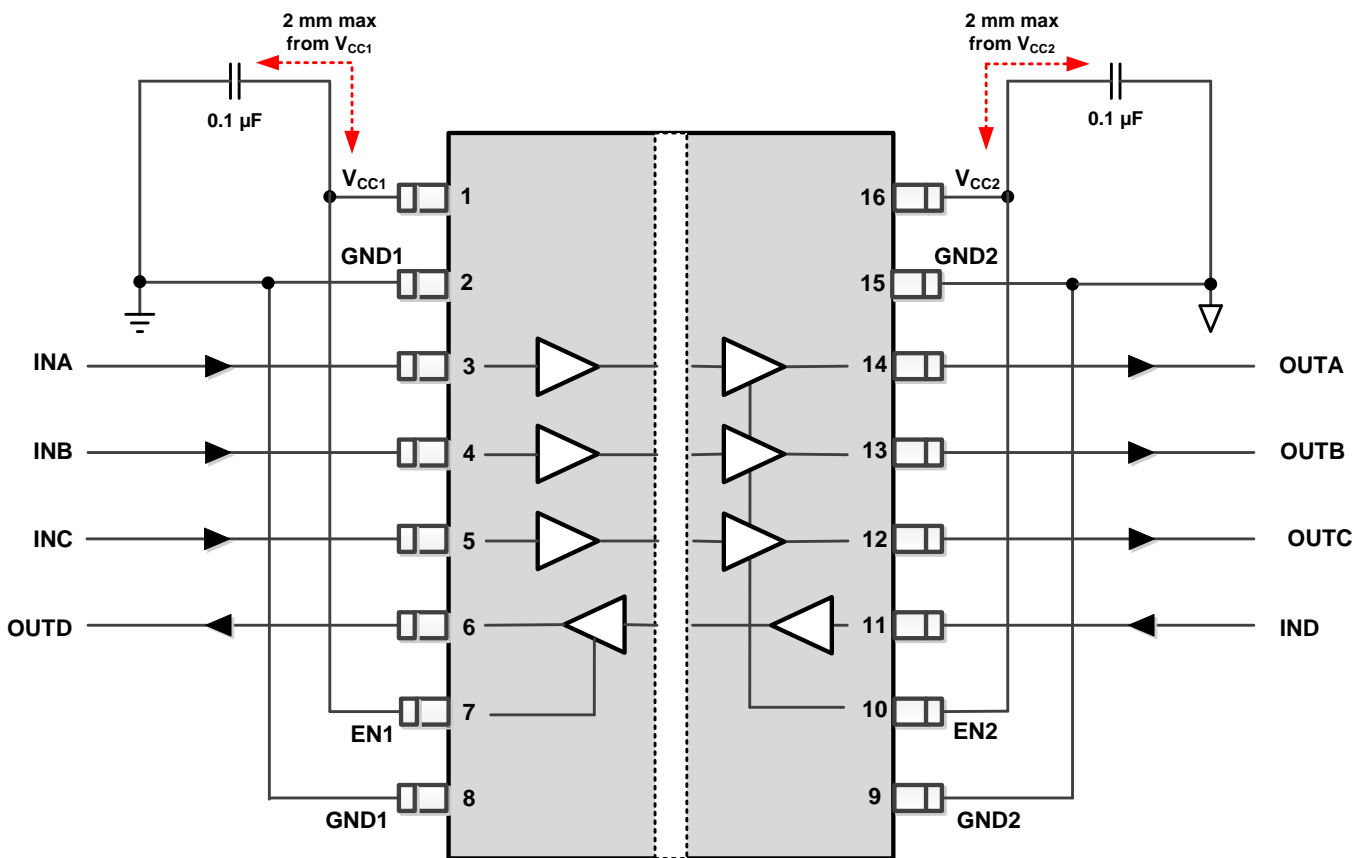
For this design example, use the parameters listed [Table 3](#).

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO774x family of devices only require two external bypass capacitors to operate.

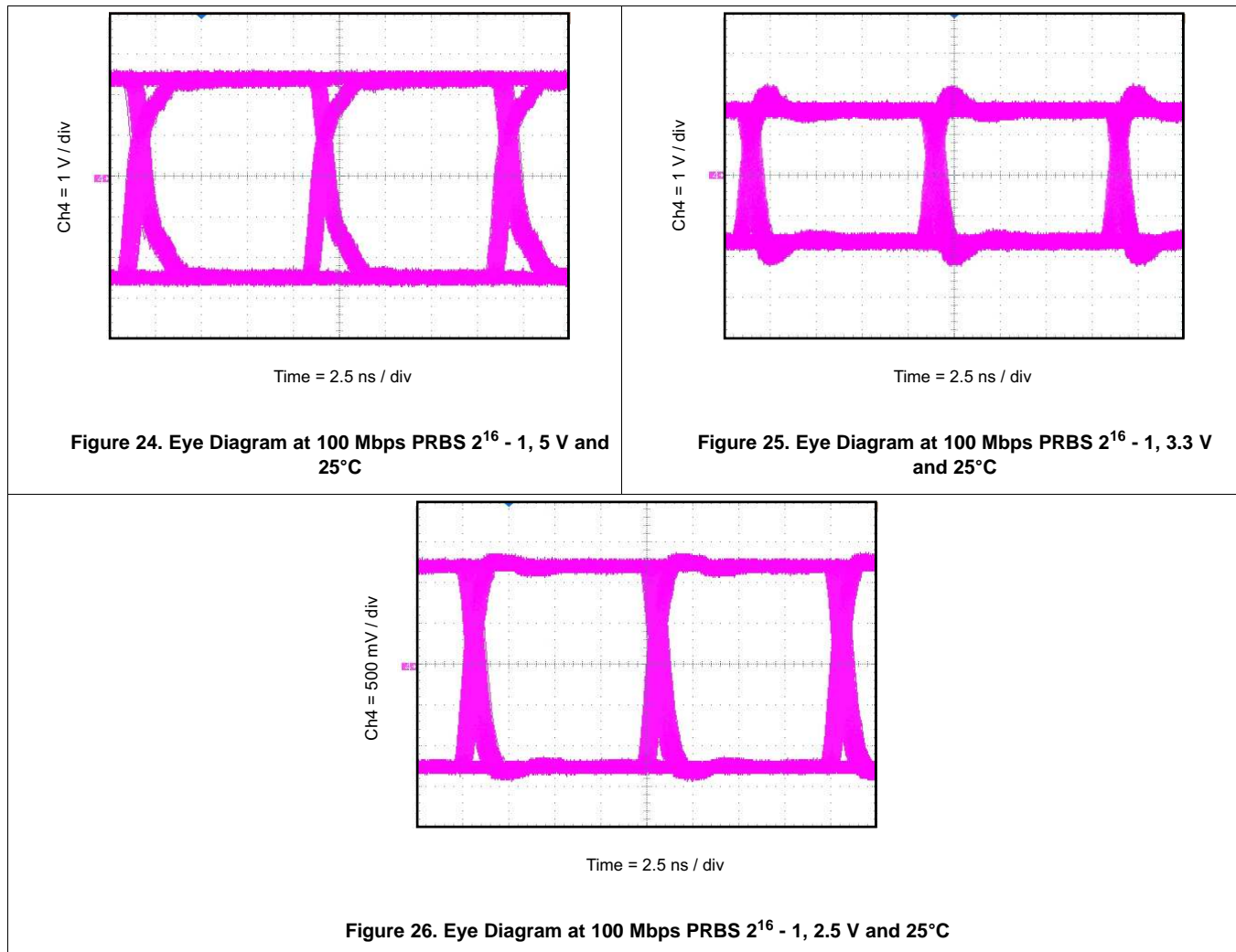


Copyright © 2016, Texas Instruments Incorporated

Figure 23. Typical ISO7741 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO774x family of devices indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.



10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501](#) data sheet ([SLLSEA0](#)).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 27](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see application note, *Digital Isolator Design Guide* ([SLLA284](#)).

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

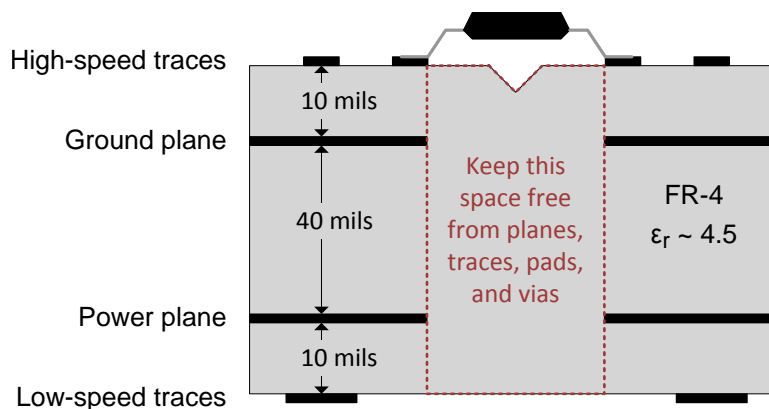


Figure 27. Layout Example Schematic

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs*, [SLAS605](#)
- *Isolation Glossary*, [SLLA353](#)
- *MSP430G2132 Mixed Signal Microcontroller*, [SLAS723](#)
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*, [SBOS410](#)
- *SN6501 Transformer Driver for Isolated Power Supplies*, [SLLSEA0](#)
- *TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices*, [SBVS153](#)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7740	Click here	Click here	Click here	Click here	Click here
ISO7741	Click here	Click here	Click here	Click here	Click here
ISO7742	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

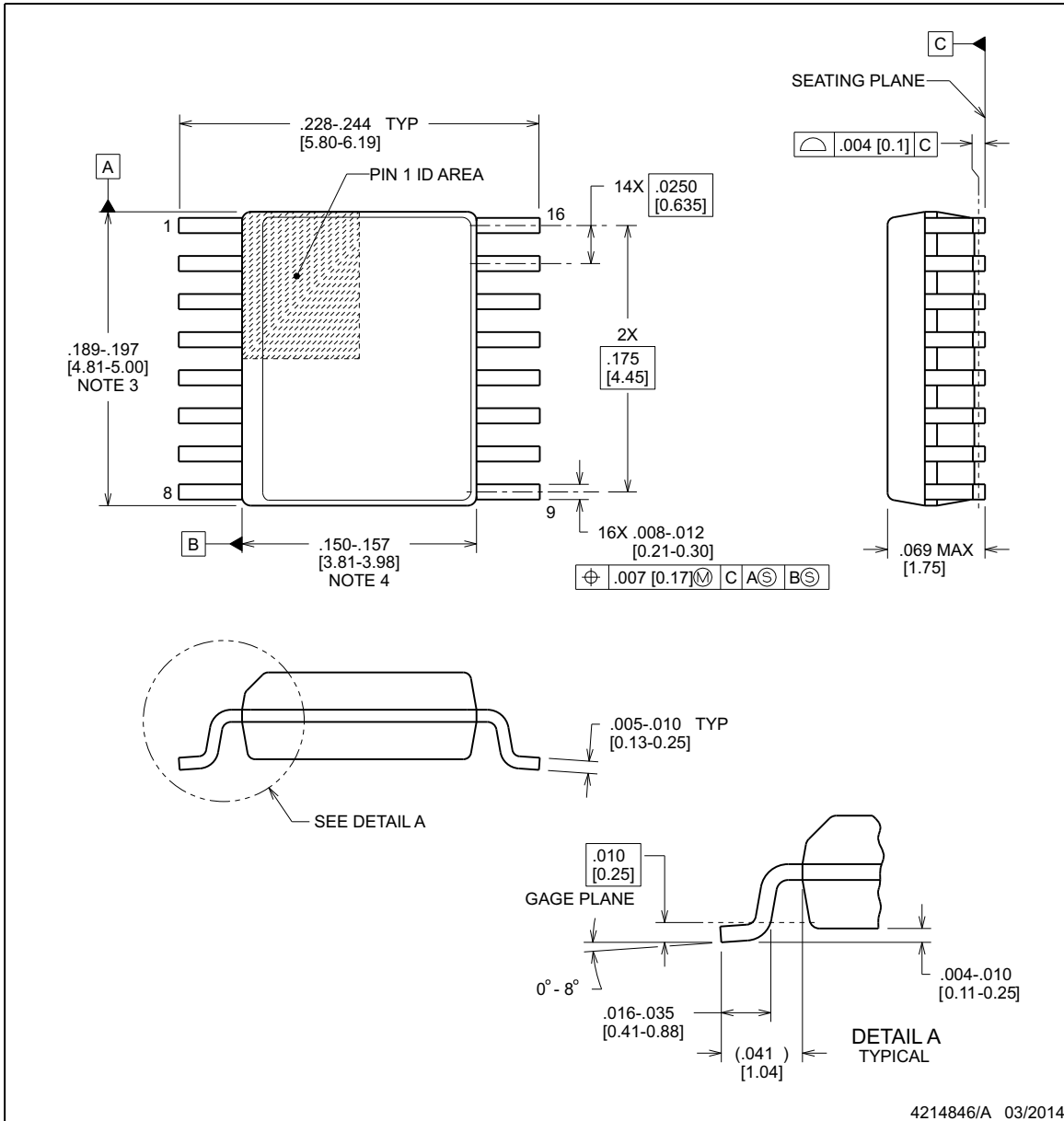
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DBQ0016A

PACKAGE OUTLINE
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

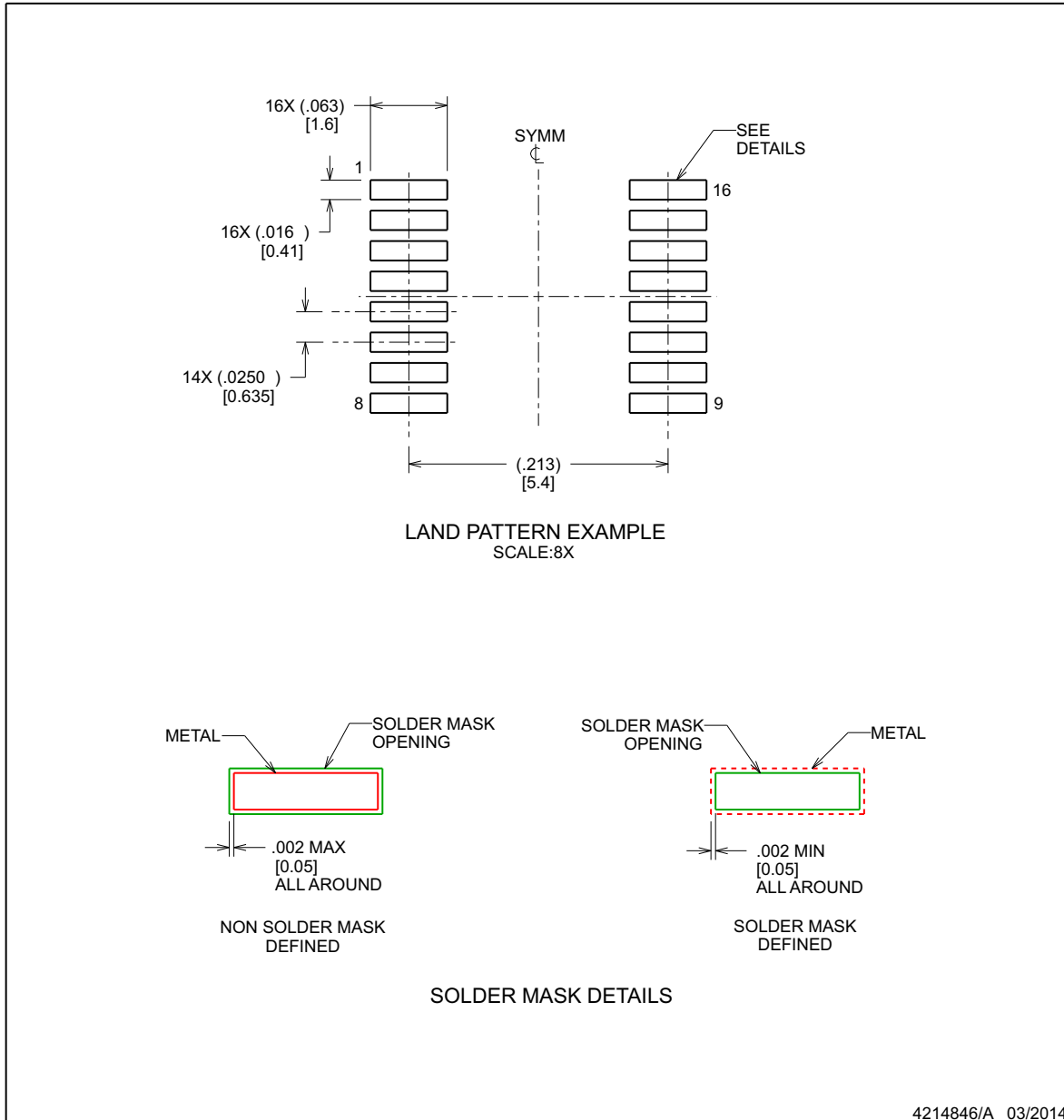
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

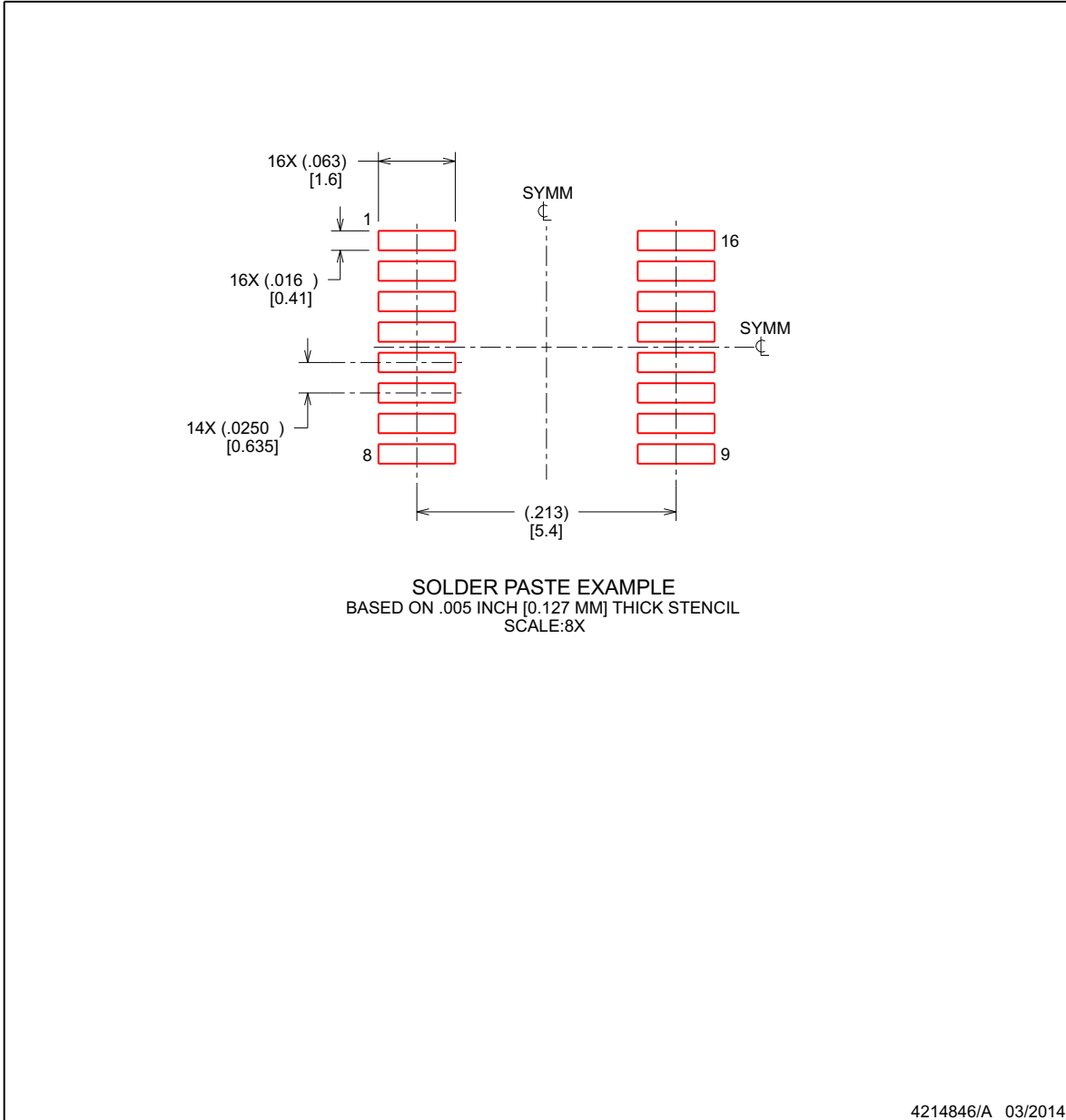
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

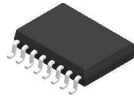
SHRINK SMALL-OUTLINE PACKAGE



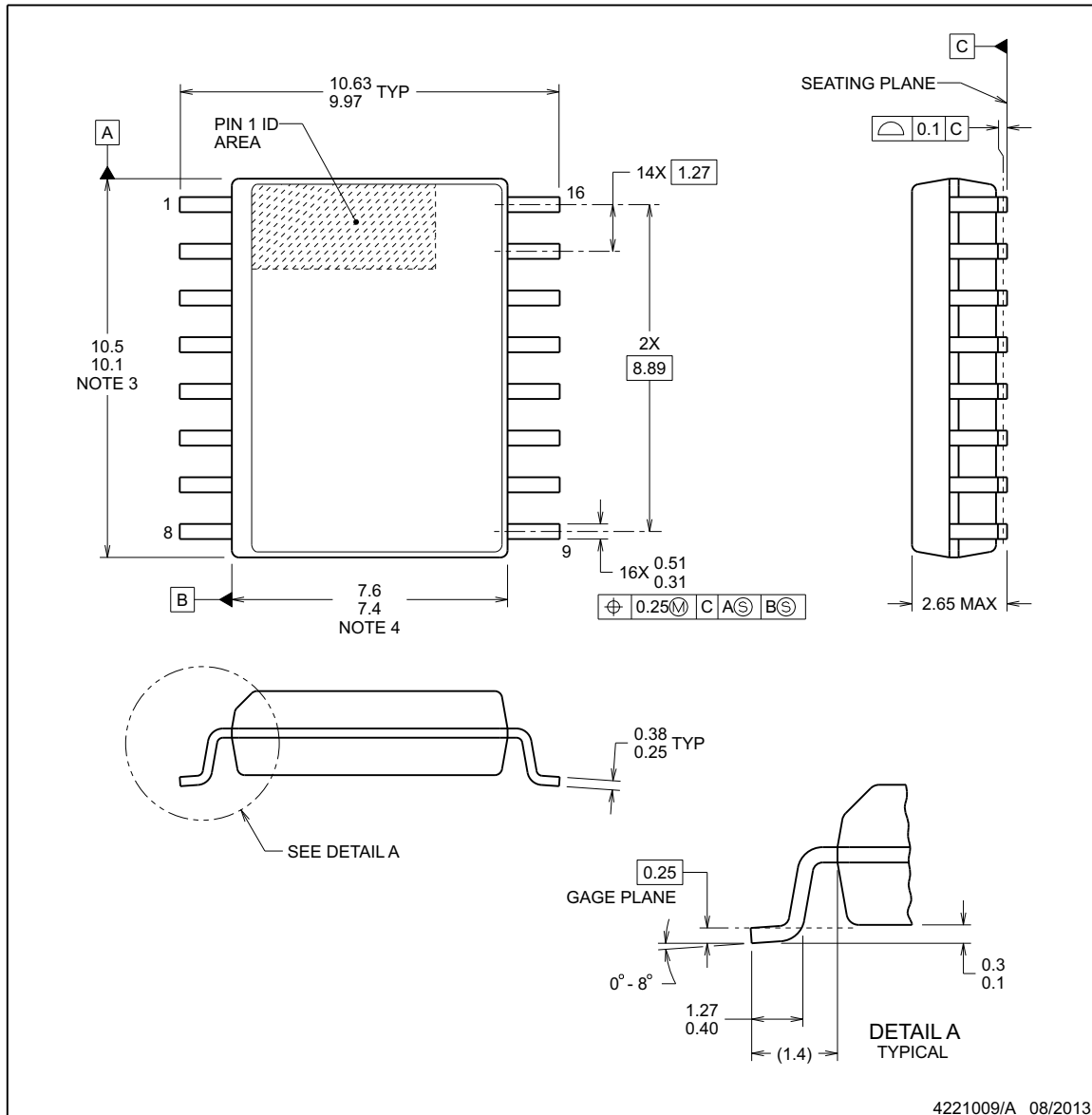
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE


DW0016B
SOIC - 2.65 mm max height

SOIC


NOTES:

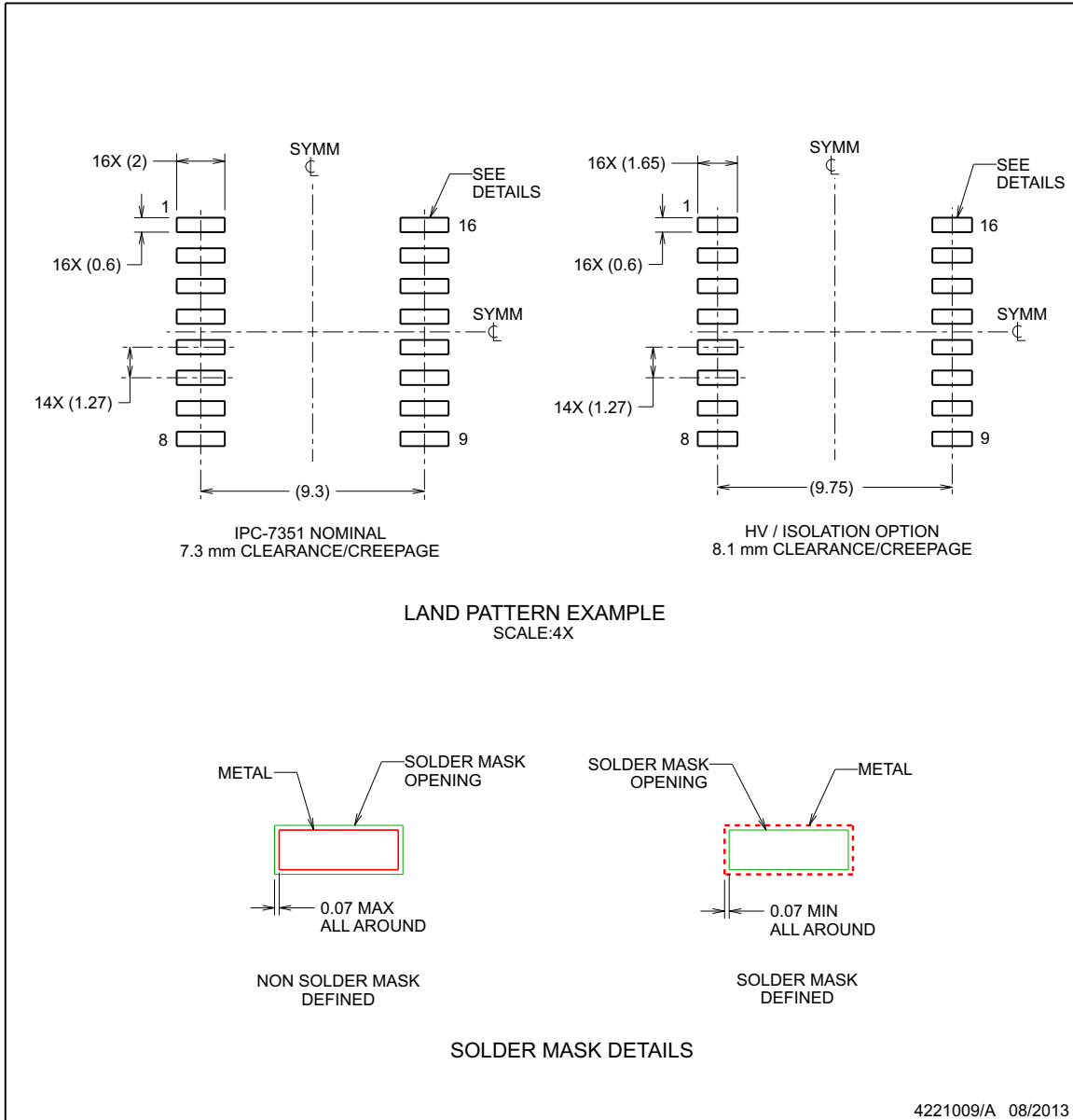
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



4221009/A 08/2013

NOTES: (continued)

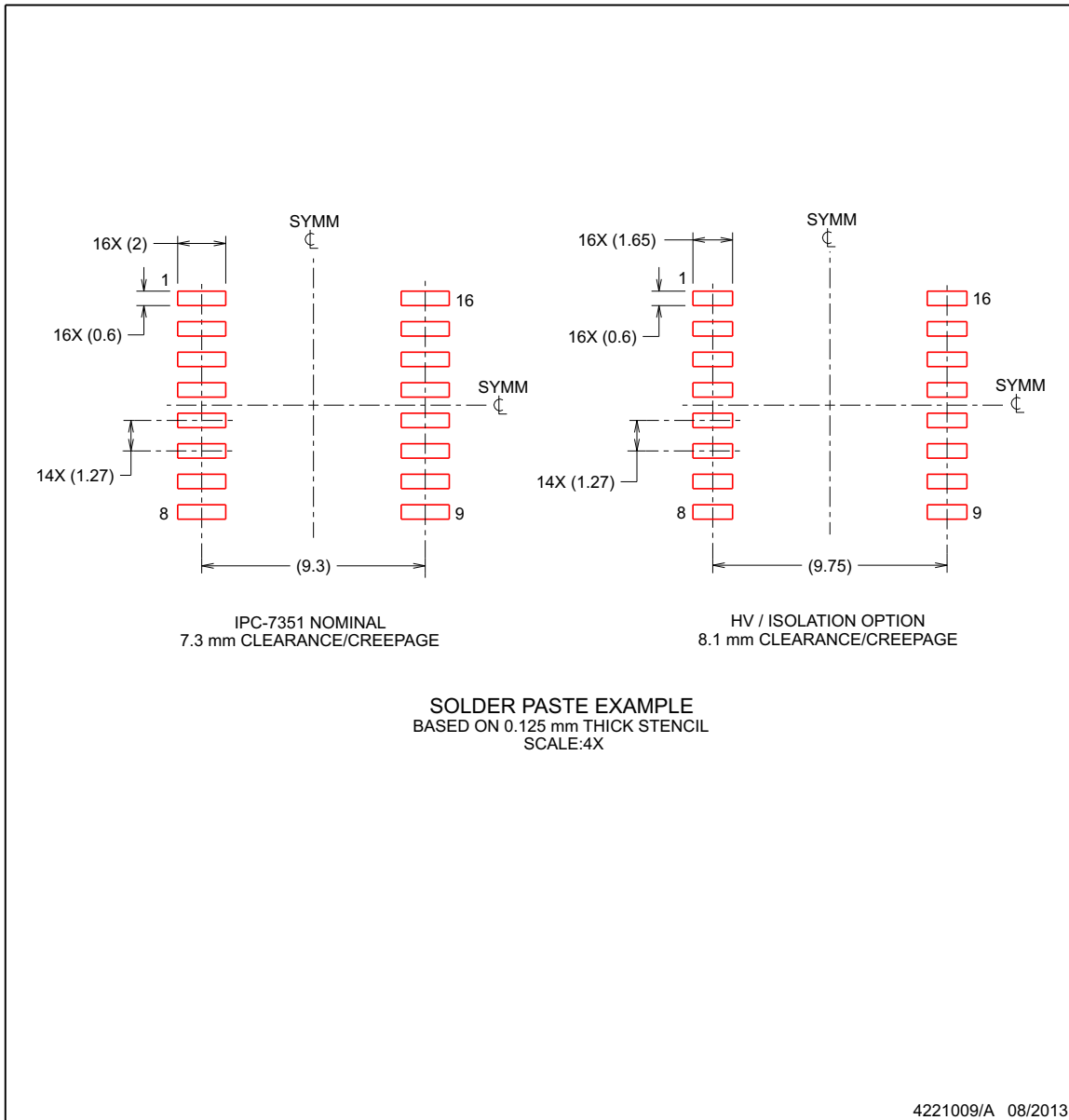
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7740DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740	Samples
ISO7740DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740	Samples
ISO7740FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740F	Samples
ISO7740FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7740F	Samples
ISO7741DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741	Samples
ISO7741DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741	Samples
ISO7741FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741F	Samples
ISO7741FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7741F	Samples
ISO7742DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742	Samples
ISO7742DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742	Samples
ISO7742FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742F	Samples
ISO7742FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7742F	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7740DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7740FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7741FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7742FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7740DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7740FDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7741DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7741FDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7742DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7742FDWR	SOIC	DW	16	2000	367.0	367.0	38.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com