

ISO5452 具有分离输出和有源保护功能的高 CMTI 2.5A 和 5A 增强型隔离式 IGBT、MOSFET 栅极驱动器

1 特性

- 共模瞬态抗扰度 (CMTI) 的最小值和典型值分别为 50kV/ μ s 和 100kV/ μ s (对应的 $V_{CM} = 1500V$)
- 分离输出, 可提供 2.5A 峰值拉电流和 5A 峰值灌电流
- 短暂传播延迟: 76ns (典型值), 110ns (最大值)
- 2A 有源米勒钳位
- 输出短路钳位
- 短路期间的软关断 (STO)
- 在检测到去饱和和故障时通过 \overline{FLT} 发出故障报警并通过 \overline{RST} 复位
- 具有就绪 (RDY) 引脚指示的输入和输出欠压锁定 (UVLO)
- 有源输出下拉特性, 在低电源或输入悬空的情况下默认输出低电平
- 2.25V 至 5.5V 输入电源电压
- 15V 至 30V 输出驱动器电源电压
- 互补金属氧化物半导体 (CMOS) 兼容输入
- 抑制短于 20ns 的输入脉冲和瞬态噪声
- 工作环境温度范围: $-40^{\circ}C$ 至 $+125^{\circ}C$
- 可承受的浪涌隔离电压达 10000V_{PK}
- 安全相关认证:
 - 符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准的 8000 V_{PK} V_{IOTM} 和 1420 V_{PK} V_{IORM} 增强型隔离
 - 符合 UL 1577 标准且长达 1 分钟的 5700 V_{RMS} 隔离
 - 符合 CSA 组件验收通知 5A, IEC 60950-1 和 IEC 60601-1 终端设备标准
 - 符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证
 - 符合 GB4943.1-2011 CQC 认证

2 应用

- 隔离式绝缘栅双极型晶体管 (IGBT) 和金属氧化物半导体场效应晶体管 (MOSFET) 驱动器:
 - 工业电机控制驱动
 - 工业电源
 - 太阳能逆变器
 - HEV 和 EV 电源模块
 - 感应加热

3 说明

ISO5452 是一款用于 IGBT 和 MOSFET 的 5.7 kV_{RMS} 增强型隔离栅极驱动器, 具有分离输出 (OUTH 和 OUTL) 以及 2.5A 的拉电流能力和 5A 的灌电流能力。输入端由 2.25V 至 5.5V 的单电源供电运行。输出侧支持的电源电压范围为 15V 至 30V。两路互补 CMOS 输入控制栅极驱动器输出状态。76ns 的短暂传播时间保证了对于输出级的精确控制。

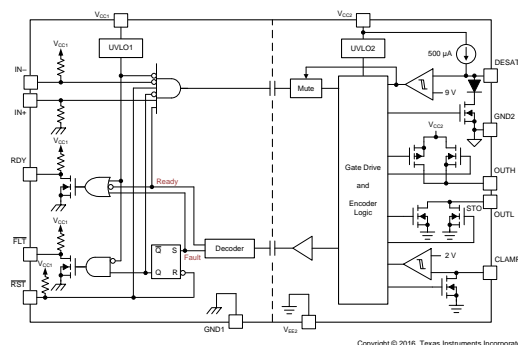
内置的去饱和 (DESAT) 故障检测功能可识别 IGBT 何时处于过流状态。检测到 DESAT 时, “静音”逻辑会立即阻断隔离器输出, 并启动软关断过程以禁止 OUTH 并将 OUTL 拉至低电平持续 2 μ s。当 OUTL 达到 2V 时 (相对于最大负电源电势 V_{EE2}), 栅极驱动器输出会被“硬”拉至 V_{EE2} 电势, 从而立即将 IGBT 关断。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
ISO5452	SOIC (16)	10.30mm x 7.50mm

(1) 如需了解所有可用封装, 请参见数据表末尾的可订购产品附录。

功能框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (September 2015) to Revision B	Page
• 已将标题由“有源安全 特性”更改至“有源保护 功能”	1
• 已将特性“浪涌抗扰度高达 10000V _{PK} (根据 IEC 61000-4-5)”更改为“可承受的浪涌隔离电压达 10000V _{PK} ”	1
• Moved <i>Insulation Specifications</i> to the <i>Specifications</i> section	6
• Changed R _{IO} Test conditions From: T _S To: T _S = 150°C in <i>Insulation Specifications</i>	6
• Moved <i>Safety-Related Certifications</i> to the <i>Specifications</i> section	7
• Moved <i>Safety Limiting Values</i> to the <i>Specifications</i> section	7
• Moved <i>Insulation Characteristics Curves</i> to the <i>Specifications</i>	11
• Added text ", but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue." to <i>Supply and Active Miller Clamp</i>	22
• Deleted ground symbol on pin 11 of the <i>Global Shutdown With Inverting Input Configuration</i> figure	29
• Deleted ground symbol on pin 11 on the inverting input of the <i>Auto Reset for Noninverting and Inverting Input Configuration</i> figure	29
• 已更改 静电放电注意事项	35

Changes from Original (August 2015) to Revision A	Page
• 已由单页产品预览变为完整数据表	1
• 已将特性“共模瞬态抗扰度的最小值和典型值分别为 50kV/μs 和 100kV/μs.”移至列表顶部	1
• 已更改 所有待通过认证的状态	1
• 更改了功能框图，在引脚 OUTL 上添加了 STO	1
• Changed R _{IO} Test conditions From: 100°C ≤ T _A ≤ max To: 100°C ≤ T _A ≤ 125°C in <i>Insulation Specifications</i>	6
• Changed the <i>Safety-Related Certifications</i> table	7
• 已添加 接收文档更新通知部分	35

5 说明（续）

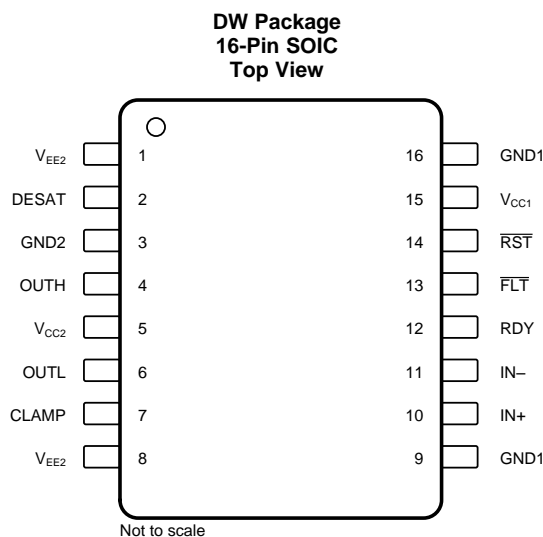
当发生去饱和故障时，器件会通过隔离栅发送故障信号，以将输入端的 $\overline{\text{FLT}}$ 输出拉为低电平并阻断隔离器的输入。“静音”逻辑在软关断期间激活。 $\overline{\text{FLT}}$ 的输出状态将被锁存，并只能在 RDY 变为高电平后通过 $\overline{\text{RST}}$ 输入上的低电平有效脉冲复位。

如果在由双极输出电源供电的正常运行期间关断 IGBT，输出电压会被硬钳位为 $V_{\text{EE}2}$ 。如果输出电源为单极，那么可采用有源米勒钳位，这种钳位会在一条低阻抗路径上灌入米勒电流，从而防止 IGBT 在高电压瞬态条件下发生动态导通。

栅极驱动器是否准备就绪待运行由两个欠压锁定电路控制，这两个电路会监视输入端和输出端的电源。如果任意一端电源不足， RDY 输出会变为低电平，否则该输出为高电平。

ISO5452 采用 16 引脚小外形尺寸集成电路 (SOIC) 封装。此器件的额定工作环境温度范围为 -40°C 至 $+125^{\circ}\text{C}$ 。

6 Pin Configuration and Function



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$V_{\text{EE}2}$	—	Output negative supply. Connect to GND2 for Unipolar supply application.
2	DESAT	I	Desaturation voltage input
3	GND2	—	Gate drive common. Connect to IGBT emitter.
4	OUTH	O	Positive gate drive voltage output
5	$V_{\text{CC}2}$	—	Most positive output supply potential.
6	OUTL	O	Negative gate drive voltage output
7	CLAMP	O	Miller clamp output
8	$V_{\text{EE}2}$	—	Output negative supply. Connect to GND2 for Unipolar supply application.
9	GND1	—	Input ground
10	IN+	I	Non-inverting gate drive voltage control input
11	IN-	I	Inverting gate drive voltage control input
12	RDY	O	Power-good output, active high when both supplies are good.
13	$\overline{\text{FLT}}$	O	Fault output, low-active during DESAT condition
14	$\overline{\text{RST}}$	I	Reset input, apply a low pulse to reset fault latch.
15	$V_{\text{CC}1}$	—	Positive input supply (2.25 V to 5.5 V)

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
16	GND1	—	Input ground

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC1}	Supply voltage input side		GND1 - 0.3	6	V
V_{CC2}	Positive supply voltage output side	$(V_{CC2} - GND2)$	-0.3	35	V
V_{EE2}	Negative supply voltage output side	$(V_{EE2} - GND2)$	-17.5	0.3	V
$V_{(SUP2)}$	Total supply output voltage	$(V_{CC2} - V_{EE2})$	-0.3	35	V
$V_{(OUTH)}$	Positive gate driver output voltage		$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
$V_{(OUTL)}$	Negative gate driver output voltage		$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
$I_{(OUTH)}$	Gate driver high output current	Gate driver high output current (maximum pulse width = 10 μ s, maximum duty cycle = 0.2%)		2.7	A
$I_{(OUTL)}$	Gate driver low output current	Gate driver high output current (maximum pulse width = 10 μ s, maximum duty cycle = 0.2%)		5.5	A
$V_{(LIP)}$	Voltage at IN+, IN-, \overline{FLT} , RDY, \overline{RST}		GND1 - 0.3	$V_{CC1} + 0.3$	V
$I_{(LOP)}$	Output current of \overline{FLT} , RDY			10	mA
$V_{(DESAT)}$	Voltage at DESAT		GND2 - 0.3	$V_{CC2} + 0.3$	V
$V_{(CLAMP)}$	Clamp voltage		$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
T_J	Junction temperature		-40	150	°C
T_{STG}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage input side		2.25		5.5	V
V_{CC2}	Positive supply voltage output side	$(V_{CC2} - GND2)$	15		30	V
V_{EE2}	Negative supply voltage output side	$(V_{EE2} - GND2)$	-15		0	V
$V_{(SUP2)}$	Total supply voltage output side	$(V_{CC2} - V_{EE2})$	15		30	V
V_{IH}	High-level input voltage (IN+, IN-, \overline{RST})		$0.7 \times V_{CC1}$		V_{CC1}	V
V_{IL}	Low-level input voltage (IN+, IN-, \overline{RST})		0		$0.3 \times V_{CC1}$	V
t_{UI}	Pulse width at IN+, IN- for full output ($C_{LOAD} = 1$ nF)		40			ns
t_{RST}	Pulse width at \overline{RST} for resetting fault latch		800			ns
T_A	Ambient temperature		-40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO5452	
		DW (SOIC)	
		16 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

7.5 Power Ratings

 $V_{CC1} = 5.5\text{ V}$, $V_{CC2} = 30\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation ⁽¹⁾				1255	mW
P_{ID}	Maximum input power dissipation				175	mW
P_{OD}	Maximum output power dissipation				1080	mW

(1) Full chip power dissipation is derated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that Junction temperature does not exceed 150°C.

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	μm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category (according to IEC 60664-1)	Rated Mains Voltage ≤ 300 V _{RMS}	I-IV	
		Rated Mains Voltage ≤ 600 V _{RMS}	I-III	
		Rated Mains Voltage ≤ 1000 V _{RMS}	I-II	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1420	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage. Time dependent dielectric breakdown (TDDb) Test, see Figure 1	1000	V _{RMS}
		DC voltage	1420	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification), t = 1 s (100% production)	8000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 10000 V _{PK} (qualification) ⁽³⁾	6250	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} = 1704 V _{PK} , t _m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} = 2272 V _{PK} , t _m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.875 × V _{IORM} = 2663 V _{PK} , t _m = 10 s	≤5	
R _{IO}	Isolation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	> 10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	Ω
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	Ω
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~1	pF
	Pollution degree		2	
	Climatic category		40/125/2 1	
UL 1577				
V _{ISO}	Withstanding Isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 6840 V _{RMS} , t = 1 s (100% production)	5700	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01	Certified according to CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced Insulation Maximum Transient isolation voltage, 8000 V _{PK} ; Maximum surge isolation voltage, 6250 V _{PK} ; Maximum repetitive peak isolation voltage, 1420 V _{PK}	Isolation Rating of 5700 V _{RMS} ; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 V _{RMS} max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V _{RMS} (354 V _{PK}) max working voltage	Single Protection, 5700 V _{RMS}	Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 V _{RMS} maximum working voltage	5700 V _{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V _{RMS} 5700 V _{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V _{RMS}
Certification completed Certificate number: 40040142	Certification completed Master contract number: 220991	Certification completed File number: E181974	Certification completed Certificate number: CQC16001141761	Certification completed Client ID number: 77311

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S Safety input, output or supply current	R _{θJA} = 99.6°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 2			456	mA
	R _{θJA} = 99.6°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 2			346	
	R _{θJA} = 99.6°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 2			228	
	R _{θJA} = 99.6°C/W, V _I = 15 V, T _J = 150°C, T _A = 25°C, see Figure 2			484	
	R _{θJA} = 99.6°C/W, V _I = 30 V, T _J = 150°C, T _A = 25°C, see Figure 2			42	
P _S Safety input, output, or total power	R _{θJA} = 99.6°C/W, T _J = 150°C, T _A = 25°C, see Figure 3			1255 ⁽¹⁾	mW
T _S Safety temperature				150	°C

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE SUPPLY						
$V_{IT+}(UVLO1)$	Positive-going UVLO1 threshold voltage input side ($V_{CC1} - GND1$)				2.25	V
$V_{IT-}(UVLO1)$	Negative-going UVLO1 threshold voltage input side ($V_{CC1} - GND1$)		1.7			V
$V_{HYS}(UVLO1)$	UVLO1 Hysteresis voltage ($V_{IT+} - V_{IT-}$) input side	$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		0.2		V
$V_{IT+}(UVLO2)$	Positive-going UVLO2 threshold voltage output side ($V_{CC2} - GND2$)	$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		12	13	V
$V_{IT-}(UVLO2)$	Negative-going UVLO2 threshold voltage output side ($V_{CC2} - GND2$)		9.5			V
		$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		11		
$V_{HYS}(UVLO2)$	UVLO2 Hysteresis voltage ($V_{IT+} - V_{IT-}$) output side	$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		1		V
I_{Q1}	Input supply quiescent current				4.5	mA
		$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		2.8		
I_{Q2}	Output supply quiescent current				6	mA
		$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		3.6		
LOGIC I/O						
$V_{IT+}(IN, \overline{RST})$	Positive-going input threshold voltage ($IN+$, $IN-$, \overline{RST})				$0.7 \times V_{CC1}$	V
$V_{IT-}(IN, \overline{RST})$	Negative-going input threshold voltage ($IN+$, $IN-$, \overline{RST})		$0.3 \times V_{CC1}$			V
$V_{HYS}(IN, \overline{RST})$	Input hysteresis voltage ($IN+$, $IN-$, \overline{RST})	$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		$0.15 \times V_{CC1}$		V
I_{IH}	High-level input leakage at ($IN+$) ⁽¹⁾	$IN+ = V_{CC1}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		100		μA
I_{IL}	Low-level input leakage at ($IN-$, \overline{RST}) ⁽²⁾	$IN- = GND1$, $\overline{RST} = GND1$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		-100		μA
I_{PU}	Pullup current of \overline{FLT} , RDY	$V_{(RDY)} = GND1$, $V_{(FLT)} = GND1$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		100		μA
V_{OL}	Low-level output voltage at \overline{FLT} , RDY	$I_{(FLT)} = 5\text{ mA}$			0.2	V
GATE DRIVER STAGE						
$V_{(OUTPD)}$	Active output pulldown voltage	$I_{(OUTH/L)} = 200\text{ mA}$, $V_{CC2} = \text{open}$			2	V
$V_{(OUTH)}$	High-level output voltage	$I_{(OUTH)} = -20\text{ mA}$		$V_{CC2} - 0.5$		V
		$I_{(OUTH)} = -20\text{ mA}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		$V_{CC2} - 0.24$		
$V_{(OUTL)}$	Low-level output voltage	$I_{(OUTL)} = 20\text{ mA}$			$V_{EE2} + 50$	mV
		$I_{(OUTL)} = 20\text{ mA}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		$V_{EE2} + 13$		
$I_{(OUTH)}$	High-level output peak current	$IN+ = \text{high}$, $IN- = \text{low}$, $V_{(OUTH)} = V_{CC2} - 15\text{ V}$	1.5			A
		$IN+ = \text{high}$, $IN- = \text{low}$, $V_{(OUTH)} = V_{CC2} - 15\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		2.5		
$I_{(OUTL)}$	Low-level output peak current	$IN+ = \text{low}$, $IN- = \text{high}$, $V_{(OUTL)} = V_{EE2} + 15\text{ V}$	3.4			A
		$IN+ = \text{low}$, $IN- = \text{high}$, $V_{(OUTL)} = V_{EE2} + 15\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		5		
$I_{(OLF)}$	Low level output current during fault condition	$T_A = 25^\circ\text{C}$, $V_{CC1} = 5\text{ V}$, $V_{CC2} - GND2 = 15\text{ V}$, $GND2 - V_{EE2} = 8\text{ V}$		130		mA

(1) I_{IH} for $IN-$, \overline{RST} pin is zero as they are pulled high internally.

(2) I_{IL} for $IN+$ is zero, as it is pulled low internally.

Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACTIVE MILLER CLAMP						
$V_{(CLP)}$	Low-level clamp voltage	$I_{(CLP)} = 20 \text{ mA}$			$V_{EE2} + 0.08$	V
		$I_{(CLP)} = 20 \text{ mA}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		$V_{EE2} + 0.015$		
$I_{(CLP)}$	Low-level clamp current	$V_{(CLAMP)} = V_{EE2} + 2.5 \text{ V}$	1.6		3.3	A
		$V_{(CLAMP)} = V_{EE2} + 2.5 \text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		2.5		
$V_{(CLTH)}$	Clamp threshold voltage		1.6		2.5	V
		$T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		2.1		
SHORT CIRCUIT CLAMPING						
$V_{(CLP_OUTH)}$	Clamping voltage ($V_{OUTH} - V_{CC2}$)	$\text{IN+} = \text{high}$, $\text{IN-} = \text{low}$, $t_{CLP} = 10 \mu\text{s}$, $I_{(OUTH)} = 500 \text{ mA}$		1.1	1.3	V
		$\text{IN+} = \text{high}$, $\text{IN-} = \text{low}$, $t_{CLP} = 10 \mu\text{s}$, $I_{(OUTH)} = 500$ mA , $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$				
$V_{(CLP_OUTL)}$	Clamping voltage ($V_{OUTL} - V_{CC2}$)	$\text{IN+} = \text{high}$, $\text{IN-} = \text{low}$, $t_{CLP} = 10 \mu\text{s}$, $I_{(OUTL)} = 500 \text{ mA}$		1.3	1.5	V
		$\text{IN+} = \text{high}$, $\text{IN-} = \text{low}$, $t_{CLP} = 10 \mu\text{s}$, $I_{(OUTL)} = 500$ mA , $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$				
$V_{(CLP_CLAMP)}$	Clamping voltage ($V_{CLP} - V_{CC2}$)	$\text{IN+} = \text{high}$, $\text{IN-} = \text{low}$, $t_{CLP} = 10 \mu\text{s}$, $I_{(CLP)} = 500$ mA , $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		1.3		V
	Clamping voltage at CLAMP	$\text{IN+} = \text{High}$, $\text{IN-} = \text{Low}$, $I_{(CLP)} = 20 \text{ mA}$			1.1	V
$V_{(CLP_OUTL)}$	Clamping voltage at OUTL ($V_{CLP} - V_{CC2}$)	$\text{IN+} = \text{High}$, $\text{IN-} = \text{Low}$, $I_{(OUTL)} = 20 \text{ mA}$			1.1	V
		$\text{IN+} = \text{High}$, $\text{IN-} = \text{Low}$, $I_{(OUTL)} = 20 \text{ mA}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		0.7		
DESAT PROTECTION						
$I_{(CHG)}$	Blanking capacitor charge current	$V_{(DESAT)} - \text{GND2} = 2 \text{ V}$	0.42		0.58	mA
		$V_{(DESAT)} - \text{GND2} = 2 \text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		0.5		
$I_{(DCHG)}$	Blanking capacitor discharge current	$V_{(DESAT)} - \text{GND2} = 6 \text{ V}$	9			mA
		$V_{(DESAT)} - \text{GND2} = 6 \text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		14		
$V_{(DSTH)}$	DESAT threshold voltage with respect to GND2		8.3		9.5	V
		$T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - \text{GND2} = 15 \text{ V}$, $\text{GND2} - V_{EE2} = 8 \text{ V}$		9		
$V_{(DSL)}$	DESAT voltage with respect to GND2, when OUTH/L is driven low		0.4		1	V

7.10 Switching Characteristics

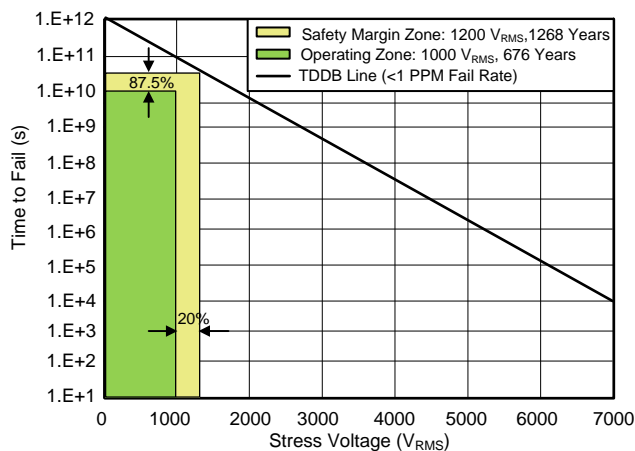
Over recommended operating conditions unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r Output signal rise time, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 1 \text{ nF}$	12		35	ns
	$C_{LOAD} = 1 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		18		
t_f Output signal fall time, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 1 \text{ nF}$	12		37	ns
	$C_{LOAD} = 1 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		20		
t_{PLH} , t_{PHL} Propagation delay, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 1 \text{ nF}$		76	110	ns
	$C_{LOAD} = 1 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$				
t_{sk-p} Pulse skew $ t_{PHL} - t_{PLH} $, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 1 \text{ nF}$			20	ns
t_{sk-pp} Part-to-part skew, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 1 \text{ nF}$			30 ⁽¹⁾	ns
t_{GF} Glitch filter on $IN+$, $IN-$, \overline{RST} , see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 1 \text{ nF}$	20		40	ns
	$C_{LOAD} = 1 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		30		
$t_{DS(90\%)}$ DESAT sense to 90% $V_{OUTH/L}$ delay, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 10 \text{ nF}$			760	ns
	$C_{LOAD} = 10 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		553		
$t_{DS(10\%)}$ DESAT sense to 10% $V_{OUTH/L}$ delay, see Figure 44, Figure 45 and Figure 46	$C_{LOAD} = 10 \text{ nF}$			3.5	μs
	$C_{LOAD} = 10 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		2		
$t_{DS(GF)}$ DESAT glitch filter delay	$C_{LOAD} = 1 \text{ nF}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		330		ns
$t_{DS(\overline{FLT})}$ DESAT sense to \overline{FLT} -low delay, see Figure 46				1.4	μs
t_{LEB} Leading edge blanking time, see Figure 44 and Figure 45		310		480	ns
	$T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		400		
$t_{GF(RSTFLT)}$ Glitch filter on \overline{RST} for resetting \overline{FLT}		300		800	ns
C_i Input capacitance ⁽²⁾	$V_i = V_{CC1} / 2 + 0.4 \times \sin(2\pi ft)$, $f = 1 \text{ MHz}$, $V_{CC1} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		2		pF
CMTI Common-mode transient immunity, see Figure 47	$V_{CM} = 1500 \text{ V}$	50			kV/ μs
	$V_{CM} = 1500 \text{ V}$, $T_A = 25^\circ\text{C}$, $V_{CC1} = 5 \text{ V}$, $V_{CC2} - GND2 = 15 \text{ V}$, $GND2 - V_{EE2} = 8 \text{ V}$		100		

(1) Measured at same supply voltage and temperature condition

(2) Measured from input pin to ground.

7.11 Insulation Characteristics Curves



T_A up to 150°C Stress-voltage frequency = 60 Hz
Figure 1. Reinforced Isolation Capacitor Lifetime Projection

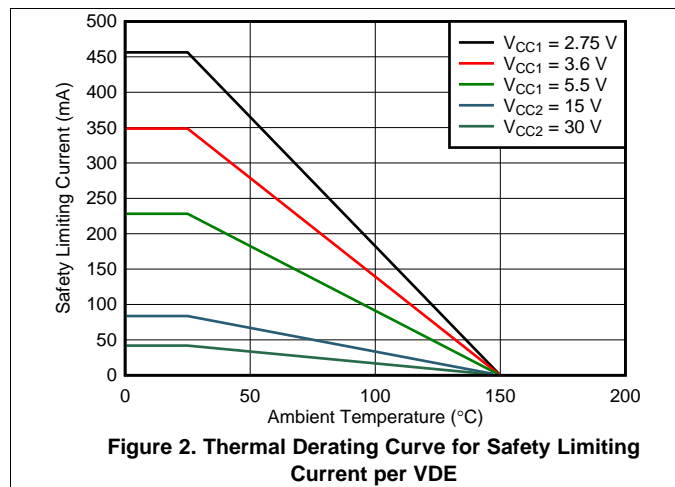


Figure 2. Thermal Derating Curve for Safety Limiting Current per VDE

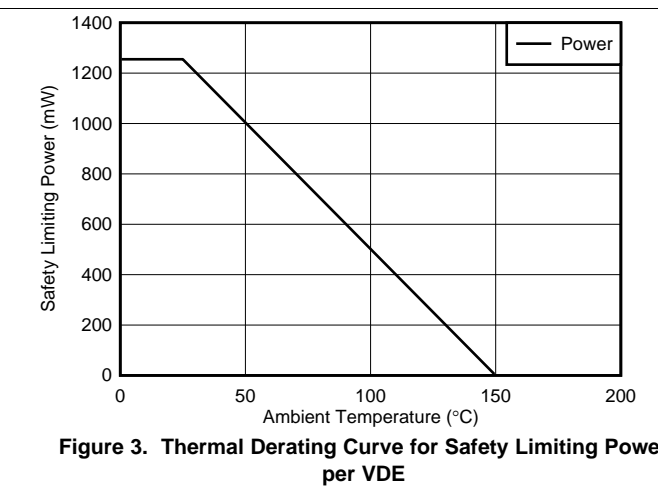


Figure 3. Thermal Derating Curve for Safety Limiting Power per VDE

7.12 Typical Characteristics

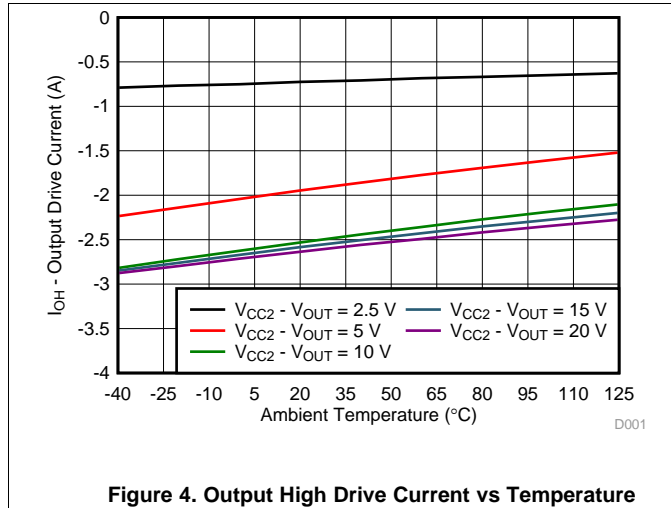


Figure 4. Output High Drive Current vs Temperature

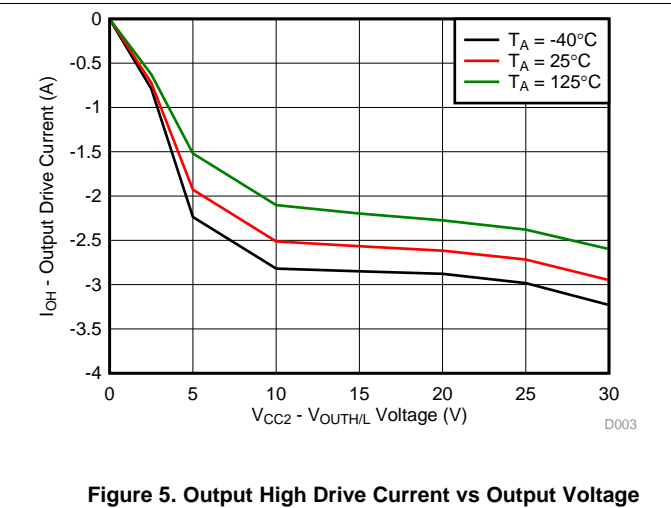


Figure 5. Output High Drive Current vs Output Voltage

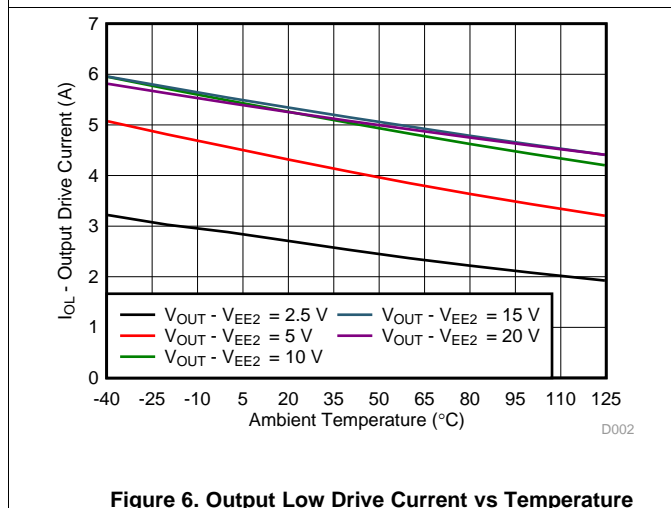


Figure 6. Output Low Drive Current vs Temperature

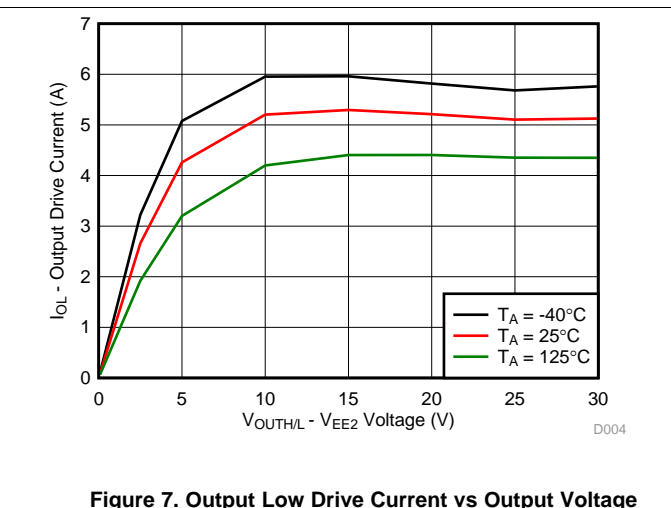


Figure 7. Output Low Drive Current vs Output Voltage

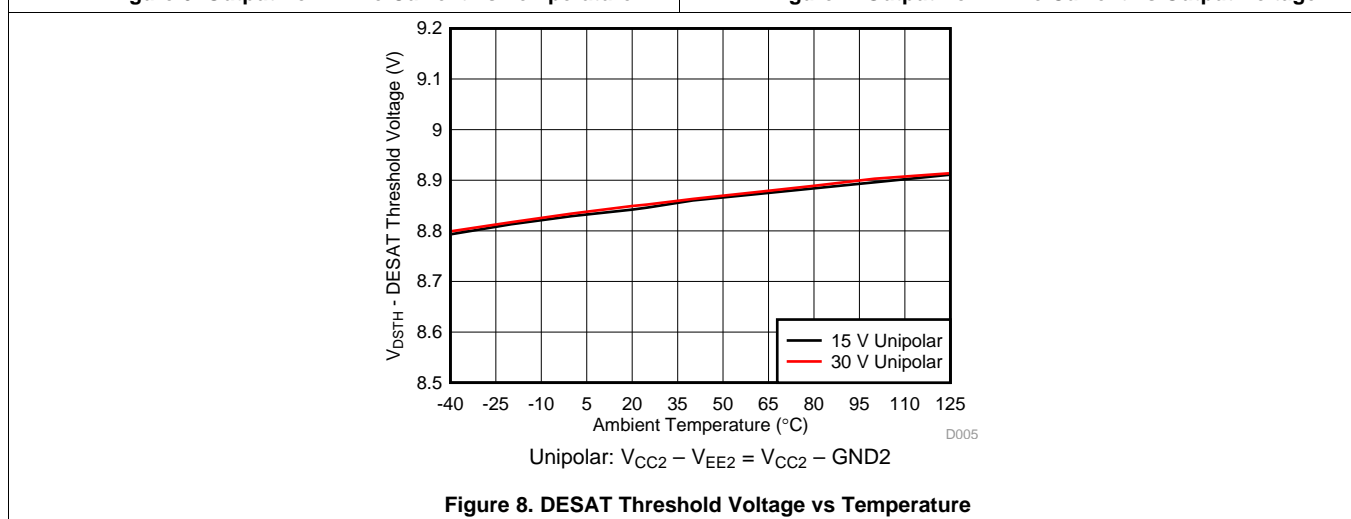
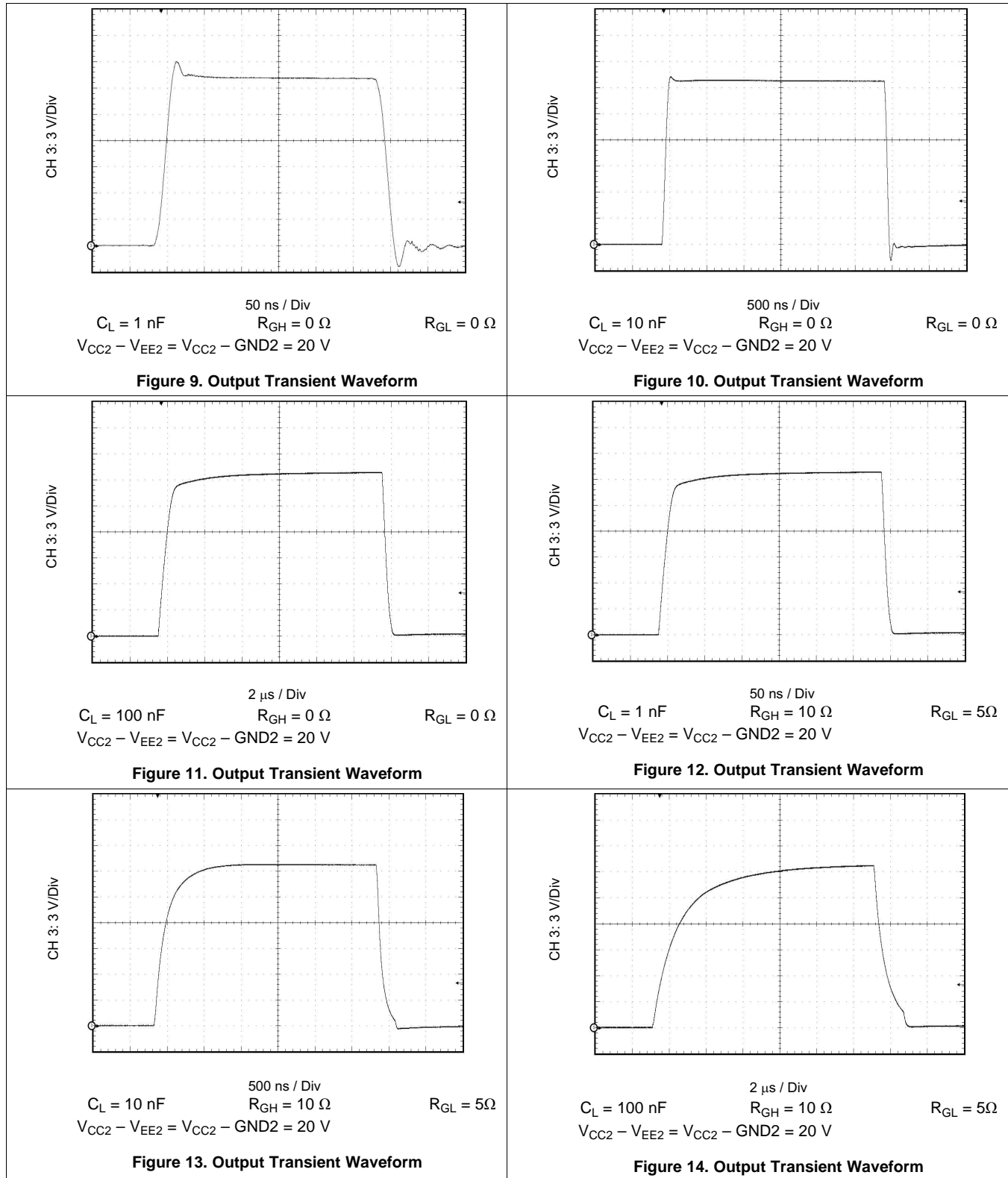


Figure 8. DESAT Threshold Voltage vs Temperature

Typical Characteristics (continued)



Typical Characteristics (continued)

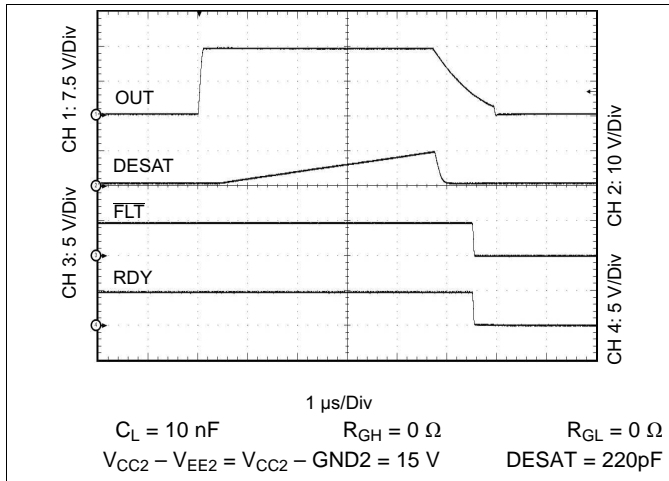


Figure 15. Output Transient Waveform DESAT, RDY and FLT

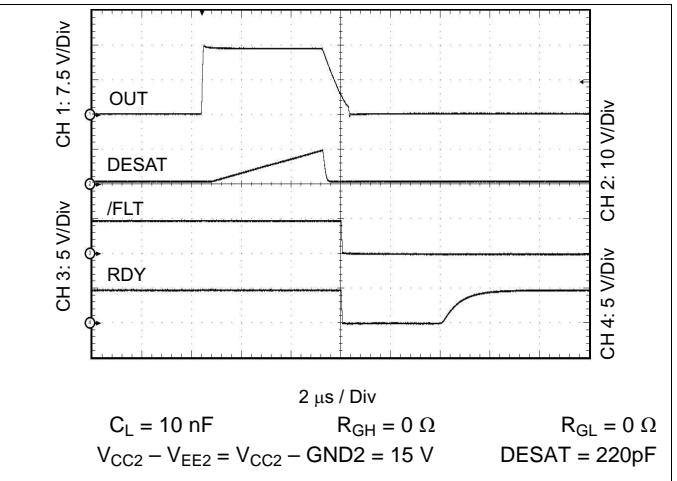


Figure 16. Output Transient Waveform DESAT, RDY and FLT

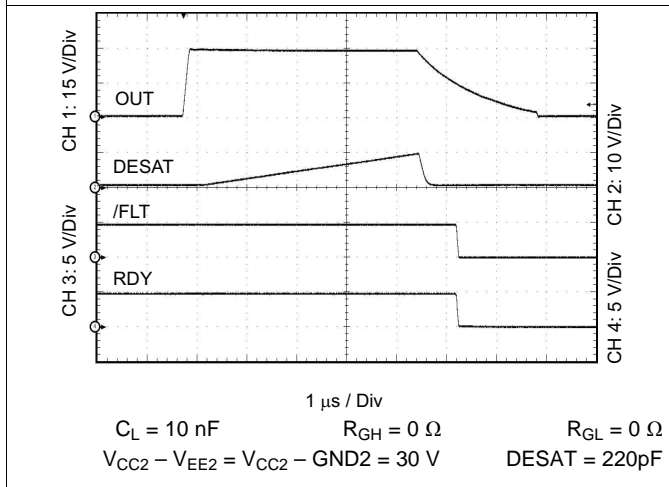


Figure 17. Output Transient Waveform DESAT, RDY and FLT

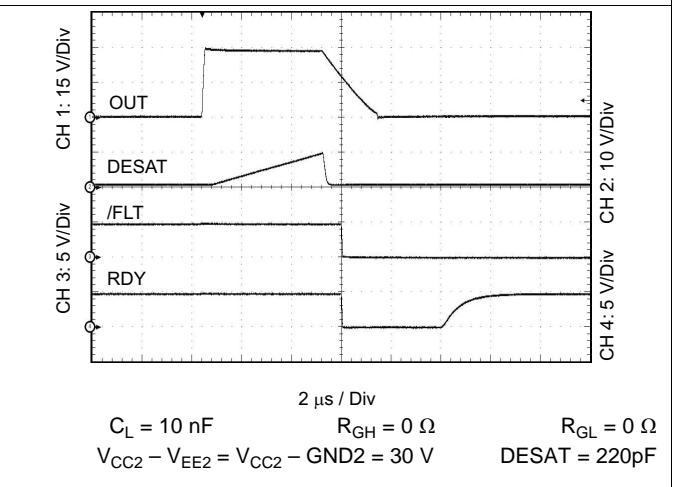


Figure 18. Output Transient Waveform DESAT, RDY and FLT

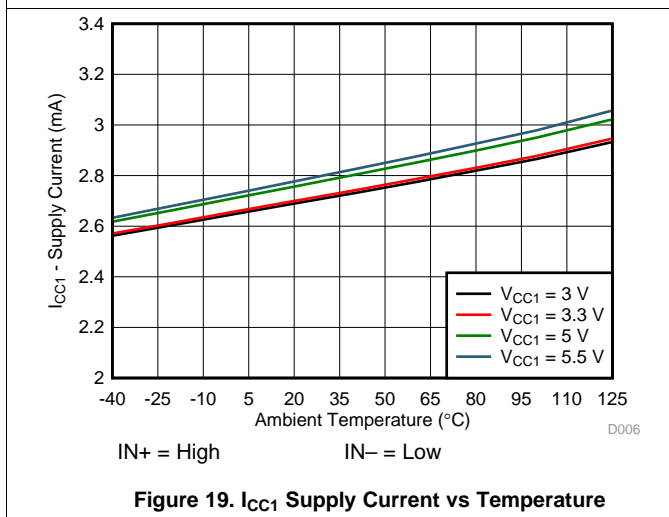


Figure 19. I_{CC1} Supply Current vs Temperature

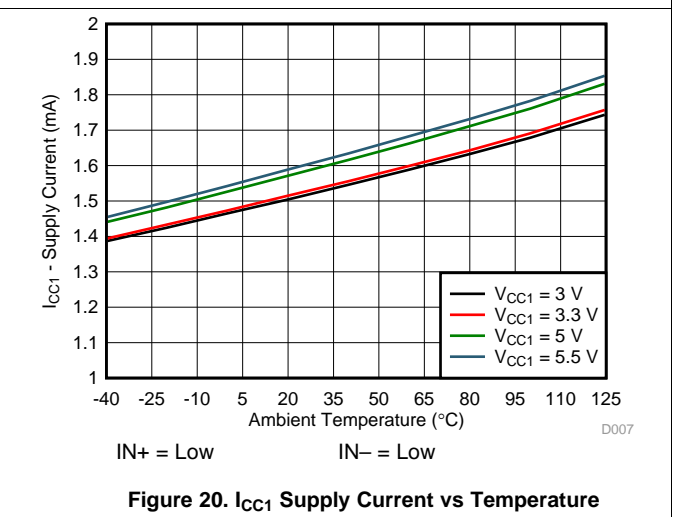


Figure 20. I_{CC1} Supply Current vs Temperature

Typical Characteristics (continued)

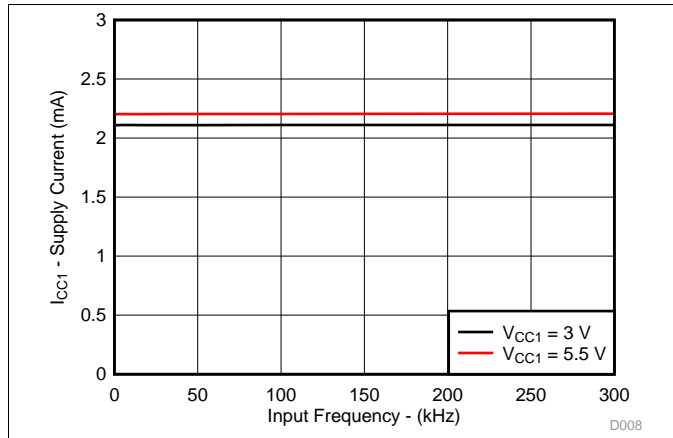


Figure 21. I_{CC1} Supply Current vs Input Frequency

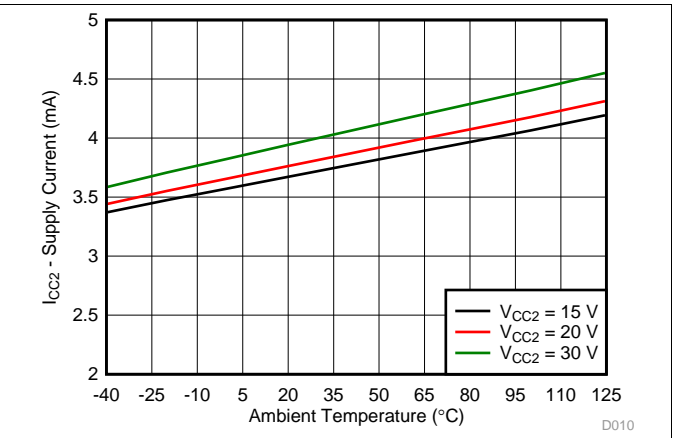


Figure 22. I_{CC2} Supply Current vs Temperature

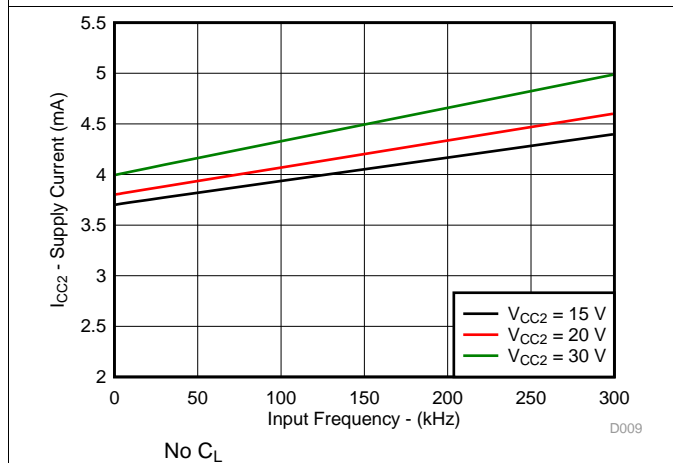


Figure 23. I_{CC2} Supply Current vs Input Frequency

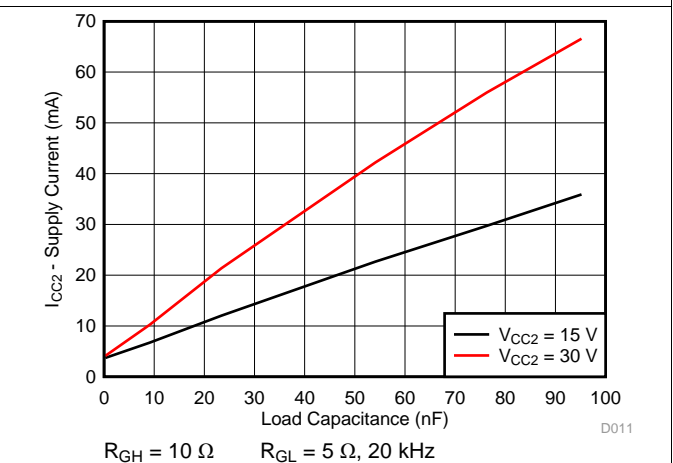


Figure 24. I_{CC2} Supply Current vs Load Capacitance

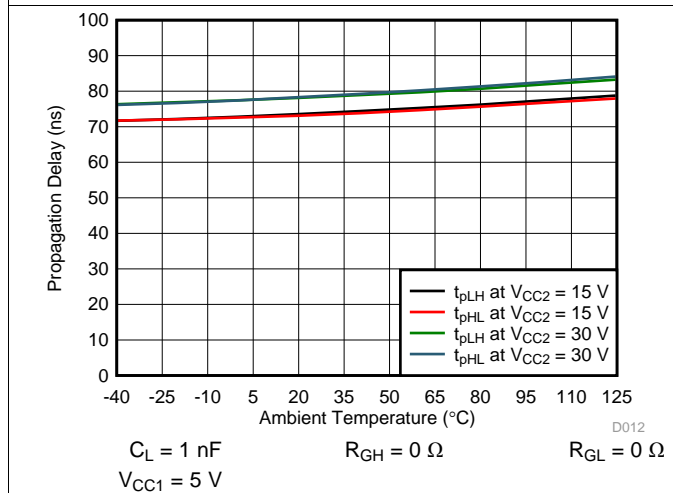


Figure 25. Propagation Delay vs Temperature

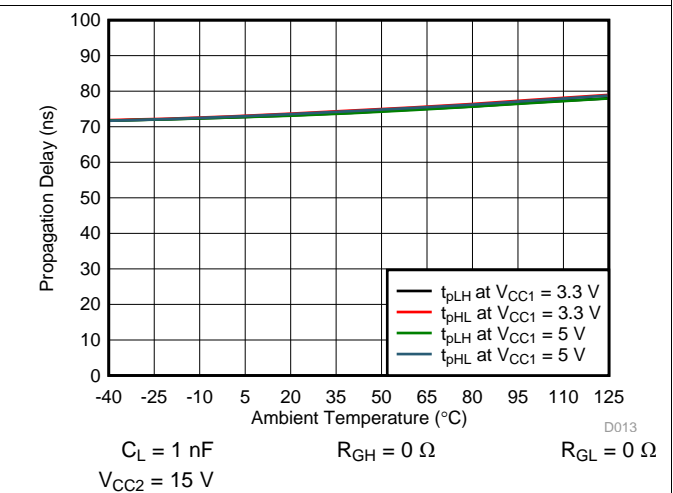


Figure 26. Propagation Delay vs Temperature

Typical Characteristics (continued)

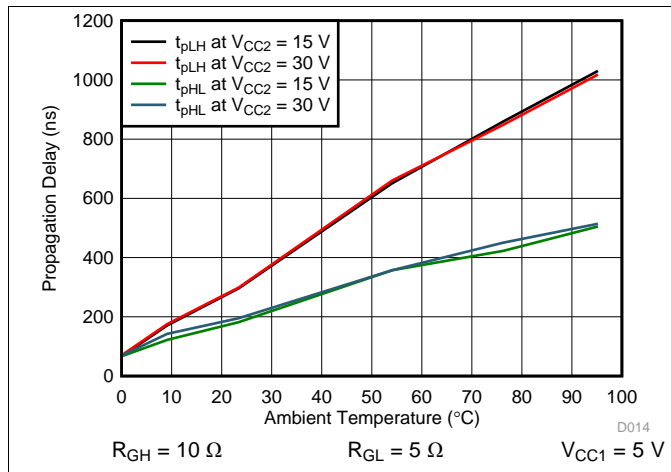


Figure 27. Propagation Delay vs Load Capacitance

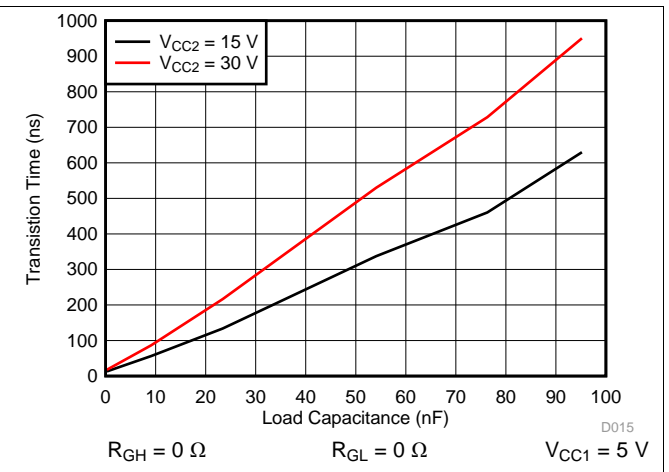


Figure 28. t_r Rise Time vs Load Capacitance

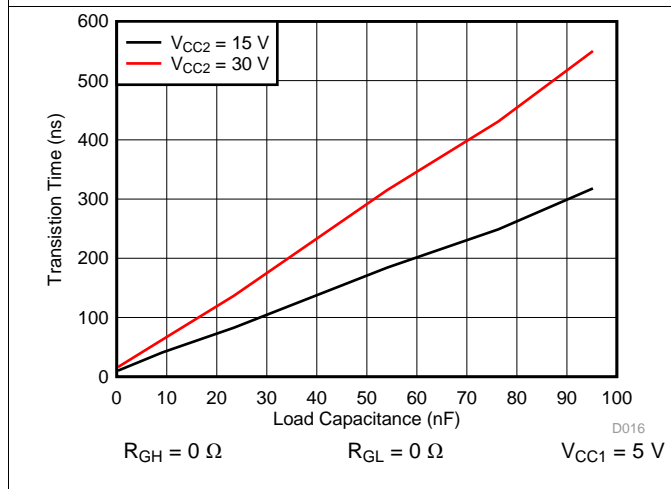


Figure 29. t_f Fall Time v. Load Capacitance

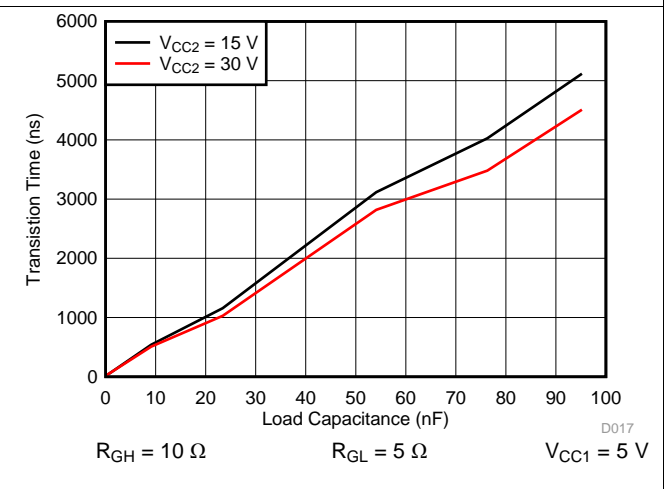


Figure 30. t_r Rise Time vs Load Capacitance

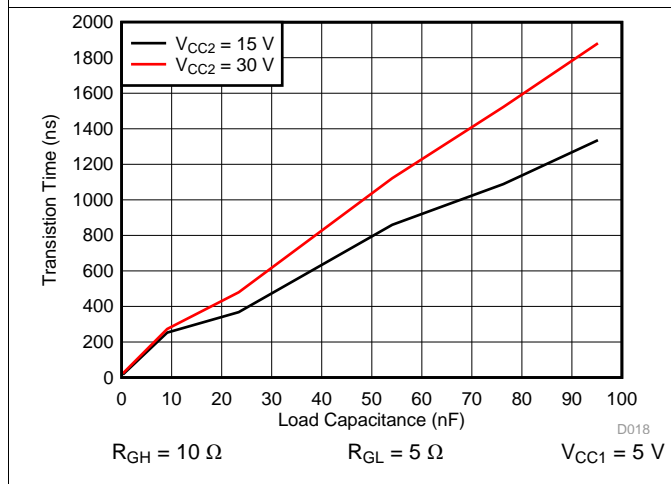


Figure 31. t_f Fall Time vs Load Capacitance

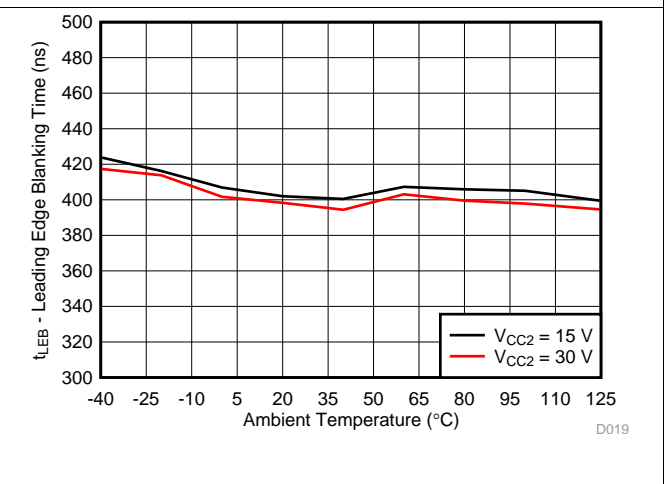


Figure 32. Leading Edge Blanking Time With Temperature

Typical Characteristics (continued)

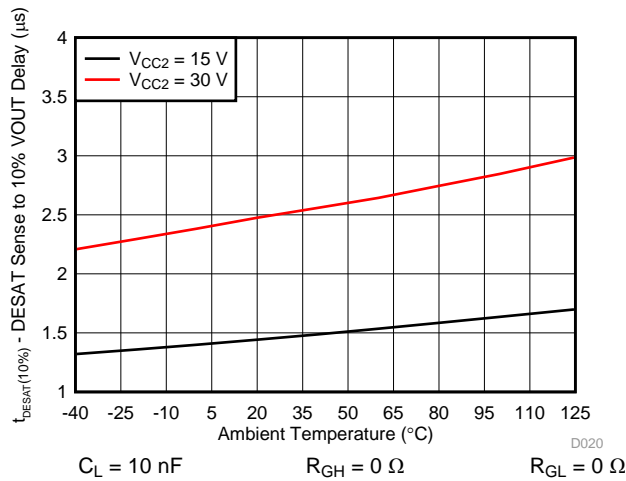


Figure 33. DESAT Sense to V_{OUTH/L} 10% Delay vs Temperature

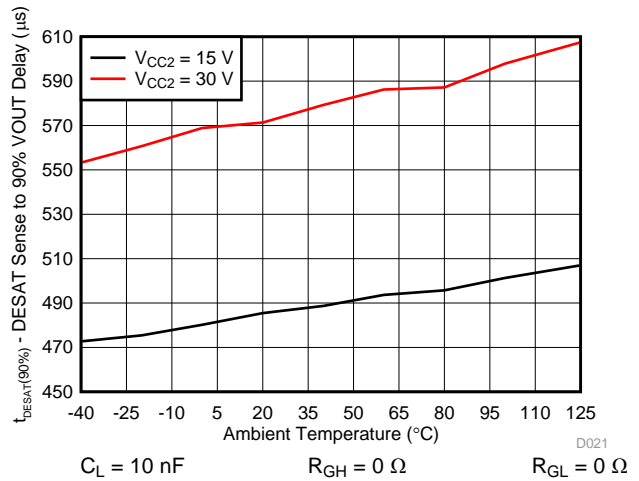


Figure 34. DESAT Sense to V_{OUTH/L} 90% Delay vs Temperature

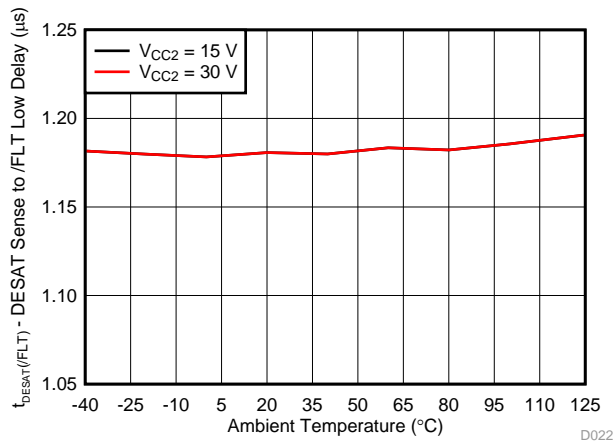


Figure 35. DESAT Sense to Fault Low Delay vs Temperature

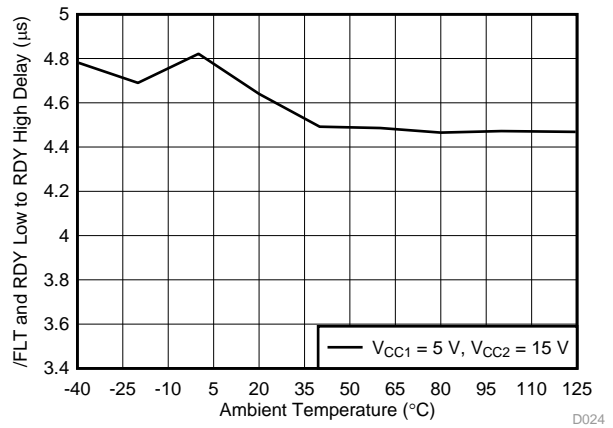


Figure 36. Fault and RDY Low to RDY High Delay vs Temperature

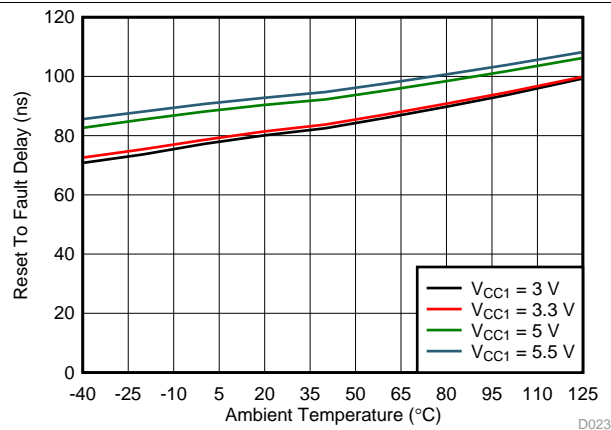


Figure 37. Reset to Fault Delay Across Temperature

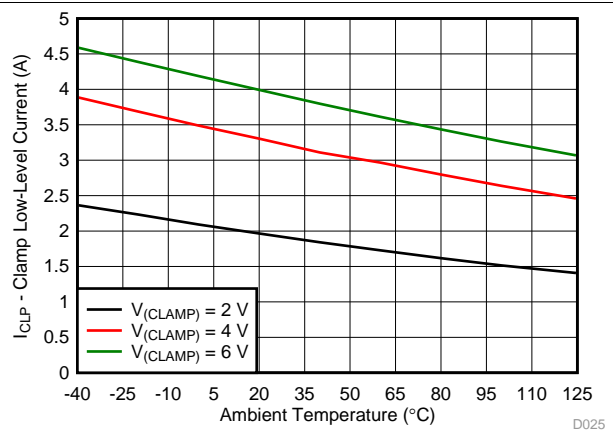


Figure 38. Miller Clamp Current vs Temperature

Typical Characteristics (continued)

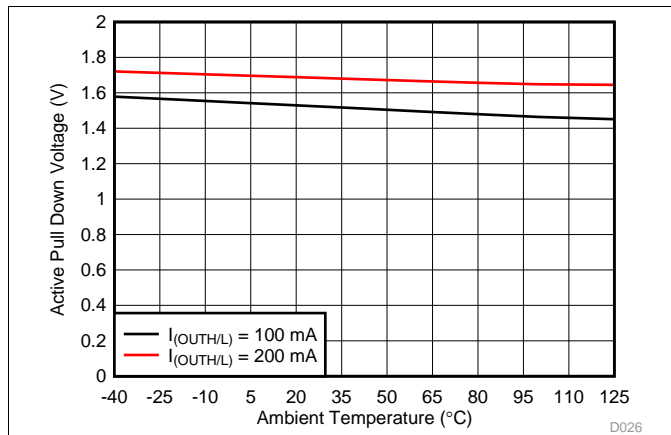


Figure 39. Active Pull Down Voltage vs Temperature

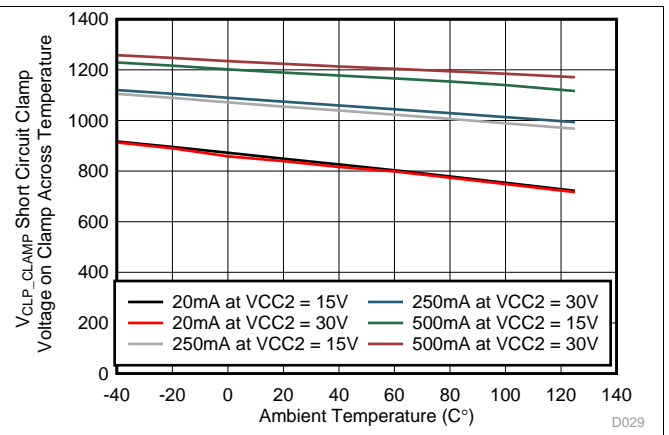


Figure 40. V_{CLP_CLAMP} - Short Circuit Clamp Voltage on Clamp Across Temperature

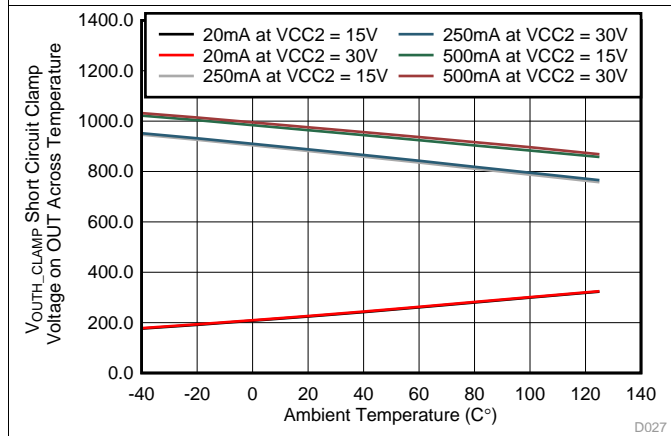


Figure 41. V_{OUTH_CLAMP} - Short Circuit Clamp Voltage on OUTH Across Temperature

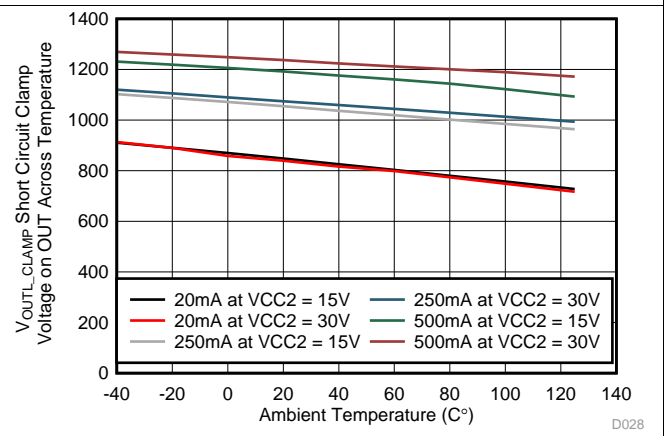
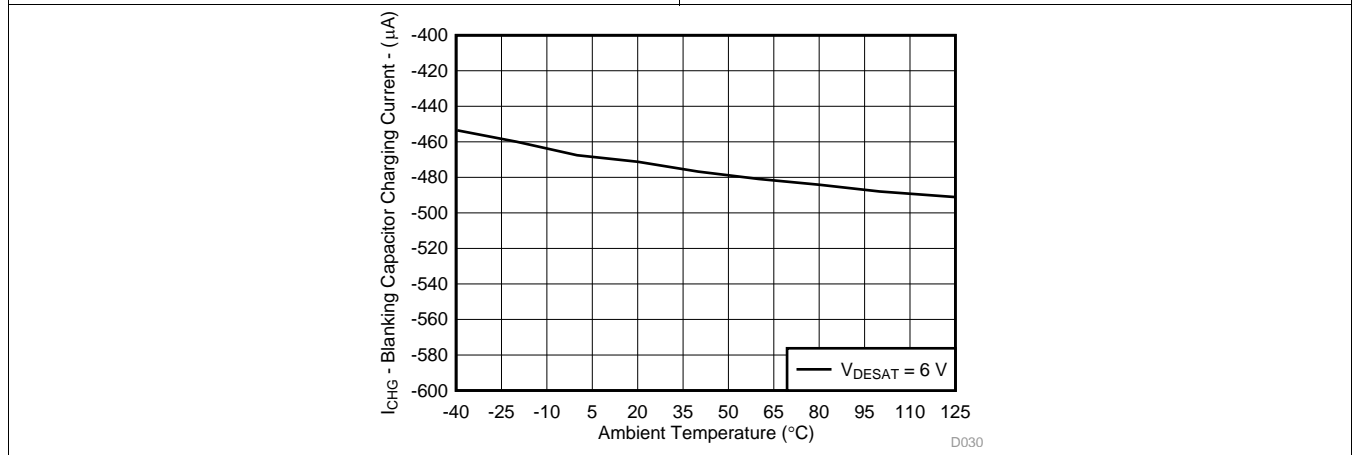


Figure 42. V_{OUTL_CLAMP} - Short Circuit Clamp Voltage on OUTL Across Temperature



$V_{CC2} = 15\text{ V}$

$DESAT = 6\text{ V}$

Figure 43. Blanking Capacitor Charging Current vs Temperature

8 Parameter Measurement Information

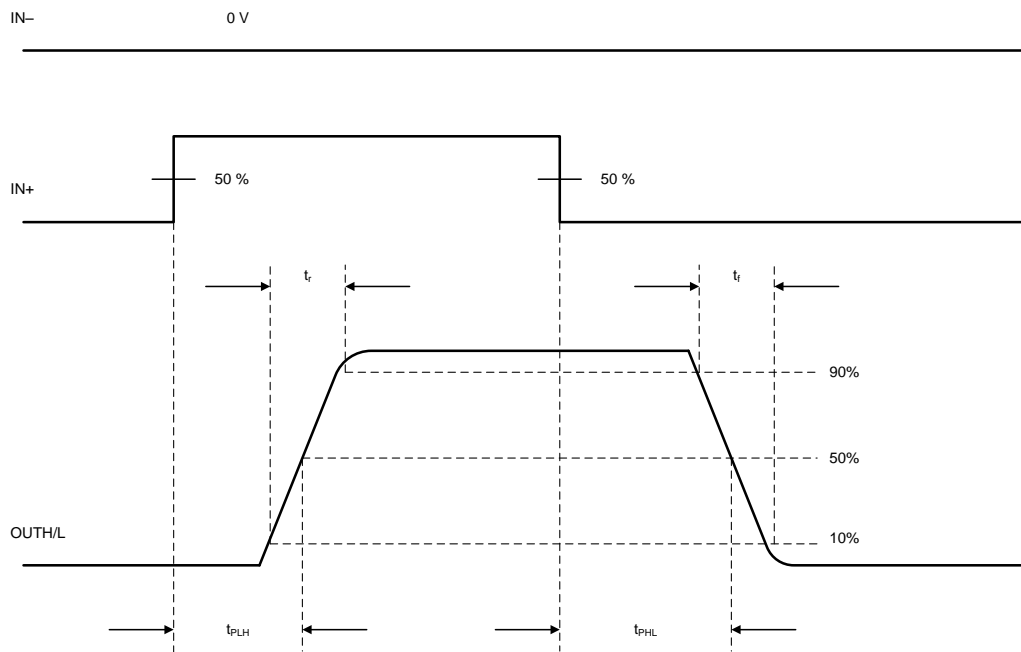


Figure 44. OUTH and OUTL Propagation Delay, Noninverting Configuration

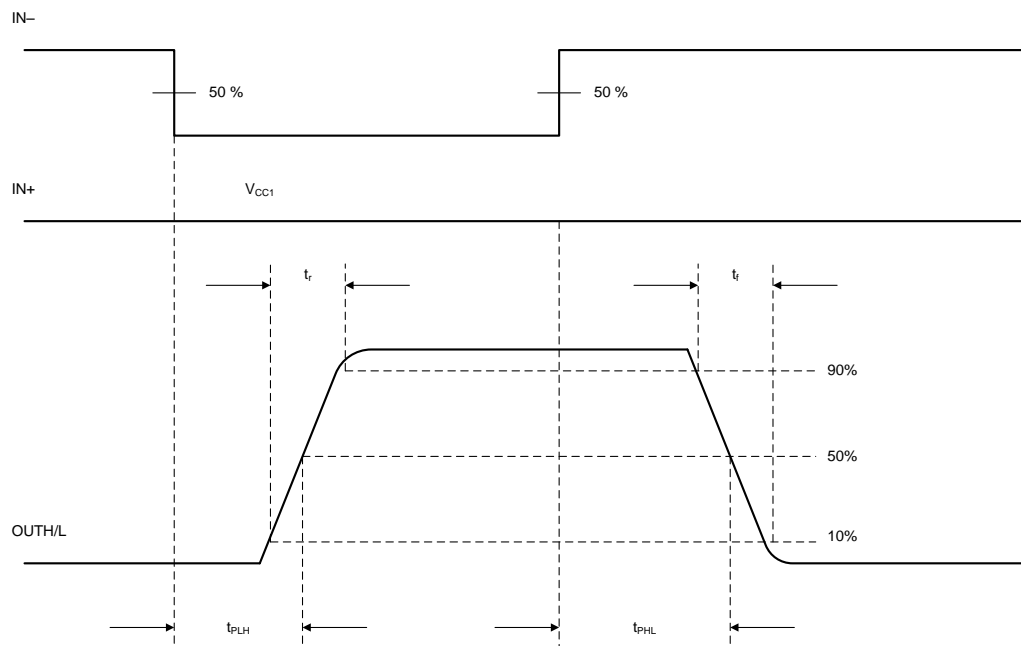


Figure 45. OUTH and OUTL Propagation Delay, Inverting Configuration

Parameter Measurement Information (continued)

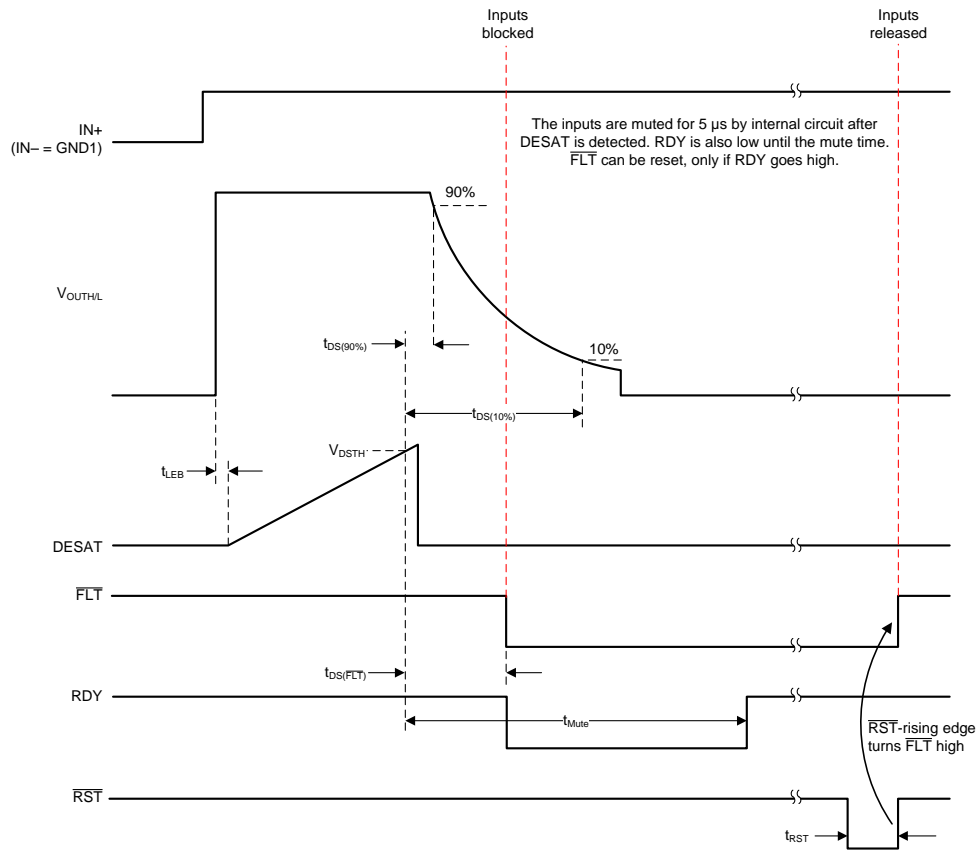
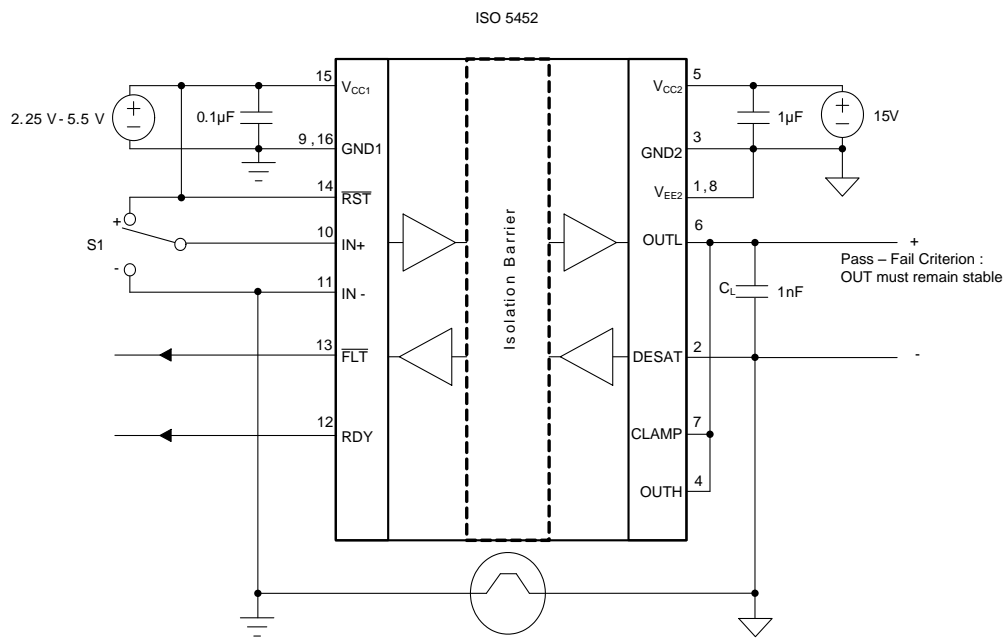


Figure 46. DESAT, OUTH, OUTL, FLT, RST Delay



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Figure 47. Common-Mode Transient Immunity Test Circuit

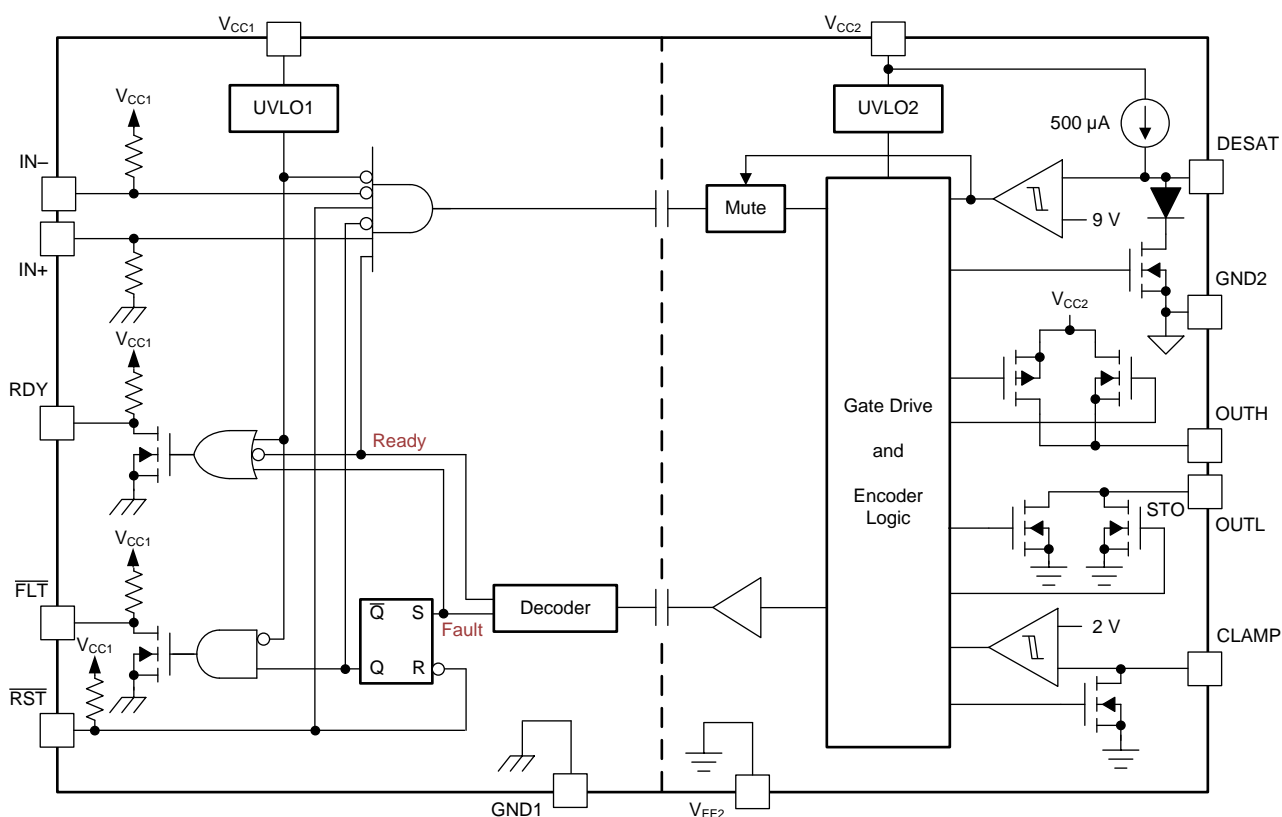
9 Detailed Description

9.1 Overview

The ISO5452 device is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a Silicon dioxide (SiO₂) capacitive isolation.

The IO circuitry on the input side interfaces with a microcontroller and consists of gate-drive control and RESET (RST) inputs, READY (RDY) and FAULT (FLT) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short-circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5452 device also has undervoltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5452 device also has an active Miller clamp function which can be used to prevent parasitic turnon of the external power transistor, because of Miller effect, for unipolar supply operation.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Supply and Active Miller Clamp

The ISO5452 device supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on the gate with respect to the emitter. This prevents the IGBT from unintentionally turning on because of current induced from the collector to the gate because Miller effect. In this condition connecting the CLAMP output of the gate driver to the IGBT gate is not necessary, but connecting the CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of V_{CC2} and V_{EE2} for bipolar operation are 15 V and –8 V with respect to GND2.

For operation with unipolar supply, typically, V_{CC2} is connected to 15 V with respect to GND2, and V_{EE2} is connected to GND2. In this use case, the IGBT can turn on because of additional charge from IGBT Miller capacitance caused by a high-voltage slew-rate transition on the IGBT collector. To prevent IGBT from turning on, the CLAMP pin is connected to IGBT gate and Miller current is sunk through a low-impedance CLAMP transistor.

Miller CLAMP is designed for miller current up to 2 A. When the IGBT is turned off and the gate voltage transitions below 2 V and the CLAMP current output is activated.

9.3.2 Active Output Pull-down

The active output pulldown feature ensures that the IGBT gate OUTH/L is clamped to V_{EE2} to ensure safe IGBT off-state, when the output side is not connected to the power supply.

9.3.3 Undervoltage Lockout (UVLO) with Ready (RDY) Pin Indication Output

Undervoltage lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned off, if the supply V_{CC1} drops below $V_{IT-(UVLO1)}$, irrespective of IN+, IN– and RST input until V_{CC1} goes above $V_{IT+(UVLO1)}$.

In similar manner, the IGBT is turned off if the supply V_{CC2} drops below $V_{IT-(UVLO2)}$, irrespective of IN+, IN– and RST input till V_{CC2} goes above $V_{IT+(UVLO2)}$.

The RDY pin indicates status of input and output side UVLO internal protection feature. If either side of device have insufficient supply (V_{CC1} or V_{CC2}), the RDY pin output goes low; otherwise, RDY pin output is high. The RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

9.3.4 Soft Turn-Off, Fault (\overline{FLT}) and Reset (\overline{RST})

During IGBT overcurrent condition, a mute logic initiates a soft-turn-off procedure which disables OUTH and pulls OUTL to low over a time span of 2 μ s. When desaturation is active, a fault signal is sent across the isolation barrier pulling the \overline{FLT} output at the input side low and blocking the isolator input. Mute logic is activated through the soft-turn-off period. The \overline{FLT} output condition is latched and can be reset only after RDY goes high, through a low-active pulse at the \overline{RST} input. \overline{RST} has an internal filter to reject noise and glitches. By asserting \overline{RST} for at least the specified minimum duration (800ns), device input logic can be enabled or disabled.

9.3.5 Short Circuit Clamp

Under short-circuit events currents can be induced back into the gate-driver OUTH/L and CLAMP pins because of parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUTH/L and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

9.4 Device Functional Modes

For OUTH/L of the ISO5452 device to follow IN+ in normal functional mode, the $\overline{\text{RST}}$ and RDY pins must be in the high state. [Table 1](#) lists the device functional modes

Table 1. Function Table⁽¹⁾

V_{CC1}	V_{CC2}	IN+	IN–	$\overline{\text{RST}}$	RDY	OUTH/L
PU	PD	X	X	X	Low	Low
PD	PU	X	X	X	Low	Low
PU	PU	X	X	Low	High	Low
PU	Open	X	X	X	Low	Low
PU	PU	Low	X	X	High	Low
PU	PU	X	High	X	High	Low
PU	PU	High	Low	High	High	High

(1) PU: Power Up ($V_{CC1} \geq 2.25\text{-V}$, $V_{CC2} \geq 13\text{-V}$), PD: Power Down ($V_{CC1} \leq 1.7\text{-V}$, $V_{CC2} \leq 9.5\text{-V}$), X: Irrelevant

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO5452 device is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. The device is intended for use in applications such as motor control, industrial inverters, and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a micro controller, and are at low voltage levels such as 2.5 V, 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 30 V (using unipolar output supply) to 15 V (using bipolar output supply), and require high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive must be applied with reference to the emitter of the IGBT (Source for MOSFET), and by construction, the emitter node in a gate drive system may swing between 0 to the DC bus voltage, that can be several 100s of volts in magnitude.

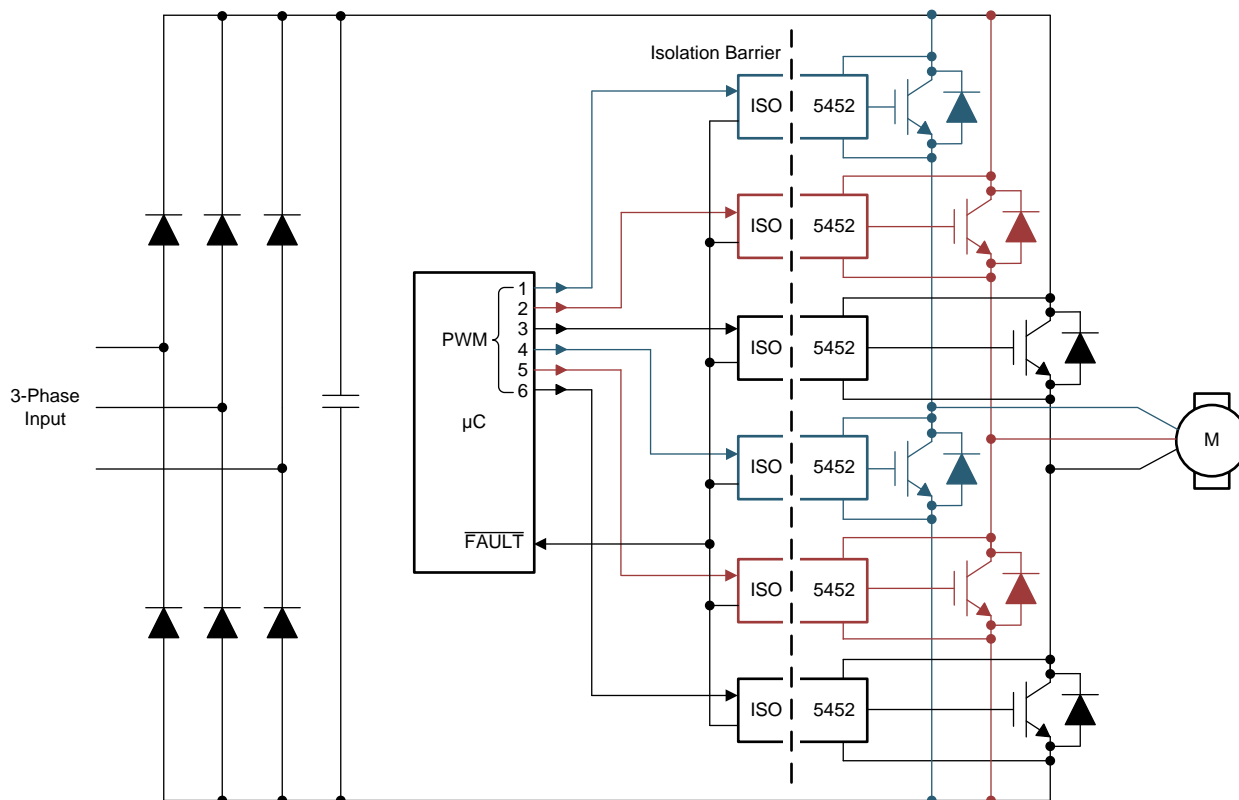
The ISO5452 device is therefore used to level shift the incoming 2.5-V, 3.3-V and 5-V control signals from the microcontroller to the 30 V (using unipolar output supply) to 15 V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

10.2 Typical Applications

[Figure 48](#) shows the typical application of a three-phase inverter using six ISO5452 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high power applications such as high-voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one SO5452. The switches are driven on and off at high switching frequency with specific patterns that to converter DC bus voltage to three-phase AC voltages.

Typical Applications (continued)



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Figure 48. Typical Motor Drive Application

10.2.1 Design Requirements

Unlike optocoupler-based gate drivers which require external current drivers and biasing circuitry to provide the input control signals, the input control to the ISO5452 device is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain FLT output signal and RST input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. Table 2 shows the allowed range for input and output supply voltage, and the typical current output available from the gate-driver.

Table 2. Design Parameters

PARAMETER	VALUE
Input supply voltage	2.25 V to 5.5 V
Unipolar output supply voltage ($V_{CC2} - GND2 = V_{CC2} - V_{EE2}$)	15 V to 30 V
Bipolar output supply voltage ($V_{CC2} - V_{EE2}$)	15 V to 30 V
Bipolar output supply voltage ($GND2 - V_{EE2}$)	0 V to 15 V
Output current	2.5 A

10.2.2 Detailed Design Procedure

10.2.2.1 Recommended ISO5452 Application Circuit

The ISO5452 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open-drain fault output suitable for wired-OR applications. The recommended application circuit in [Figure 49](#) shows a typical gate driver implementation with unipolar output supply and [Figure 50](#) shows a typical gate driver implementation with bipolar output supply using the ISO5452 device.

A 0.1- μF bypass capacitor, recommended at input supply pin V_{CC1} and 1- μF bypass capacitor, recommended at output supply pin V_{CC2} , provide the large transient currents necessary during a switching transition to ensure reliable operation. The 220-pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode (D_{DST}) and the 1-k Ω series resistor are external protection components. The R_G gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain $\overline{\text{FLT}}$ output and RDY output has a passive 10-k Ω pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and will not resume switching until the microcontroller applies a reset signal.

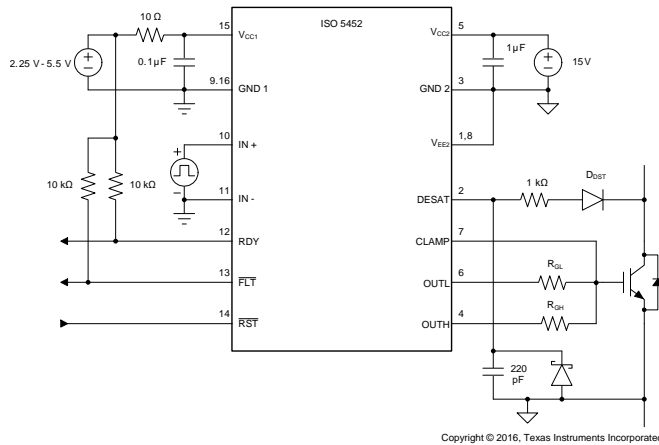


Figure 49. Unipolar Output Supply

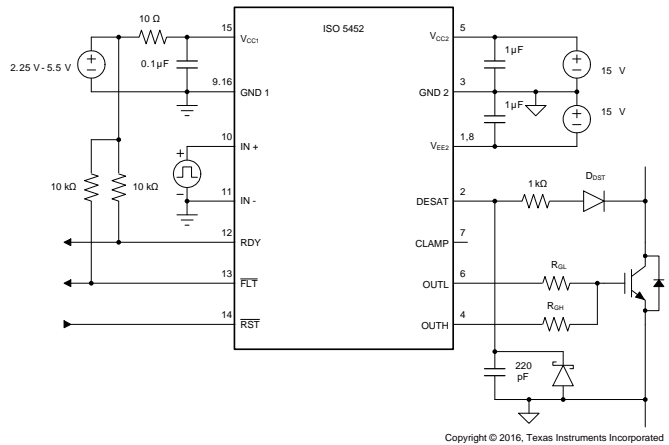
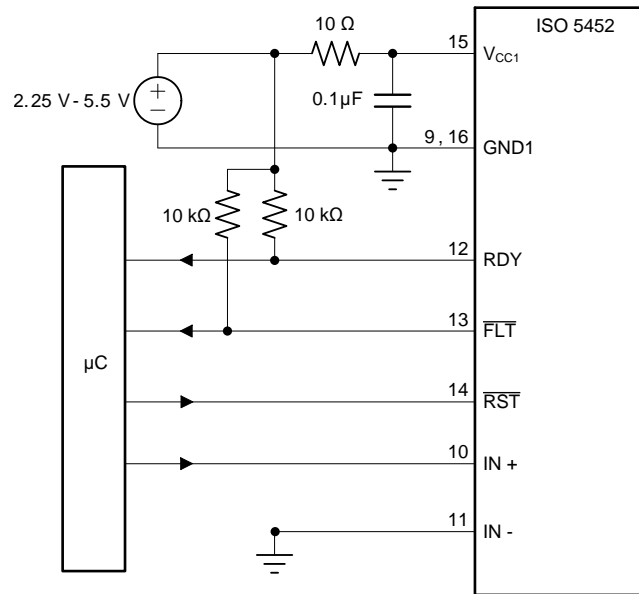


Figure 50. Bipolar Output Supply

10.2.2.2 $\overline{\text{FLT}}$ and RDY Pin Circuitry

A 50-k Ω pullup resistor is internally connected on the $\overline{\text{FLT}}$ and RDY pins. The $\overline{\text{FLT}}$ and RDY pins are an open-drain output. A 10-k Ω pullup resistor can be used to make it faster rise and to provide logic high when $\overline{\text{FLT}}$ and RDY is inactive, as shown in [Figure 51](#).

Fast common mode transients can inject noise and glitches on $\overline{\text{FLT}}$ and RDY pins because of parasitic coupling. This is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the $\overline{\text{FLT}}$ and RDY pins.



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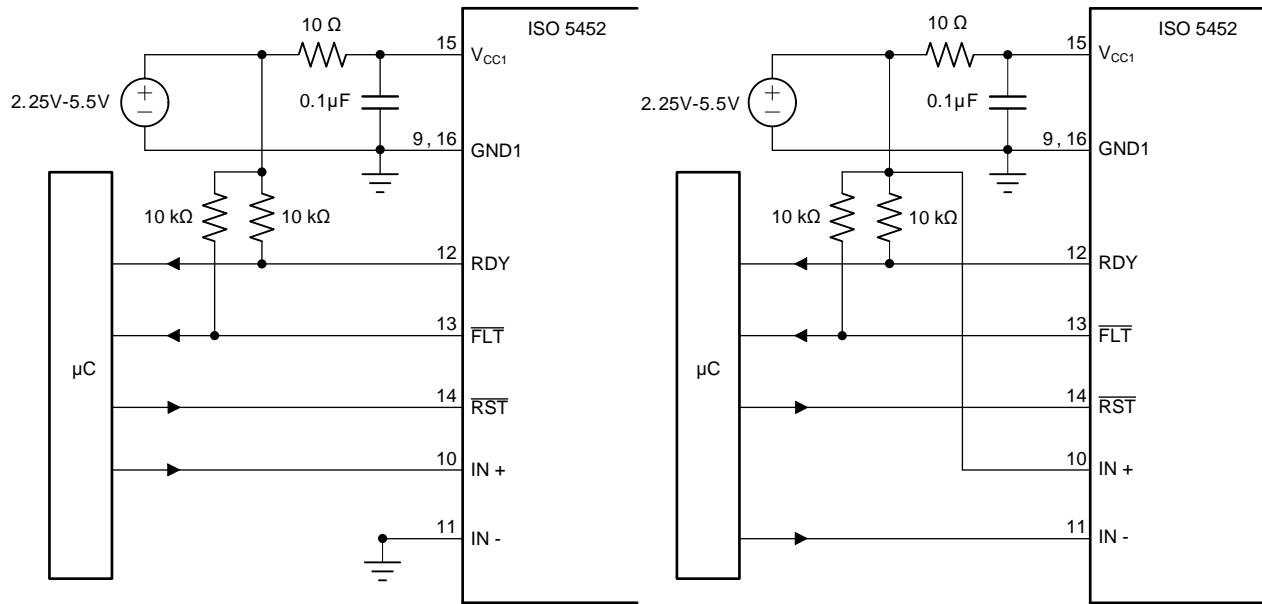
Figure 51. $\overline{\text{FLT}}$ and RDY Pin Circuitry for High CMTI

10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5452 device. For maximum CMTI performance, the digital control inputs, IN+ and IN–, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5452 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. A 20-ns glitch filter can filter a glitch up to 20 ns on IN+ or IN–.

10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the $\overline{\text{FLT}}$ output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.



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Figure 52. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)

10.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5452 device can be configured to shutdown automatically in the event of a fault condition by tying the FLT output to IN+. For high reliability drives, the open drain FLT outputs of multiple ISO5452 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low $\overline{\text{FLT}}$ output disables all six gate drivers simultaneously.

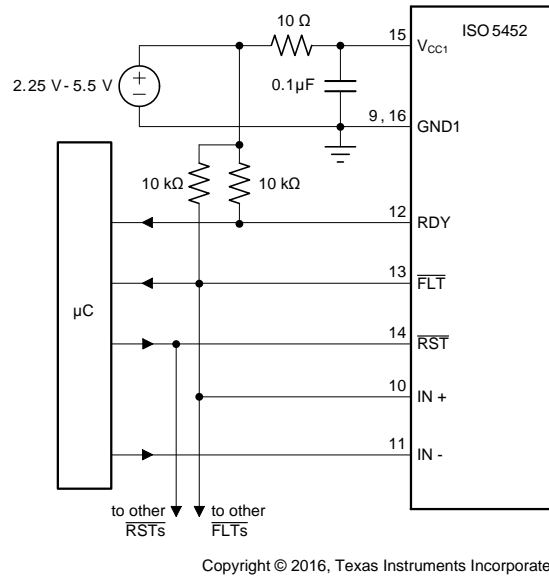


Figure 53. Global Shutdown With Inverting Input Configuration

10.2.2.6 Auto-Reset

In this case, the gate control signal at IN+ is also applied to the $\overline{\text{RST}}$ input to reset the fault latch every switching cycle. Incorrect $\overline{\text{RST}}$ makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the gate low state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before IN+ goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next on cycle.

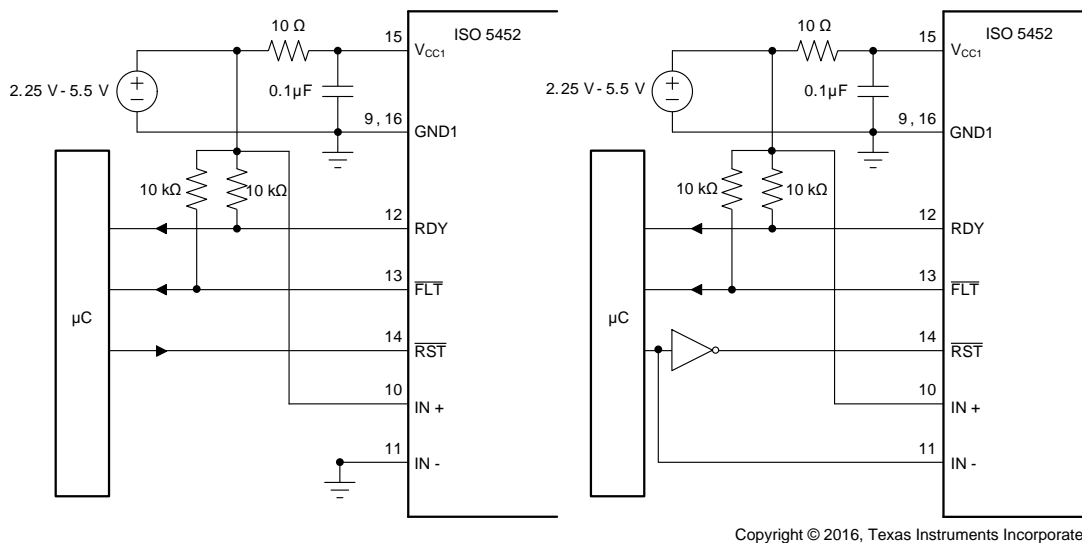


Figure 54. Auto Reset for Noninverting and Inverting Input Configuration

10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to GND2 potential at low voltage levels.

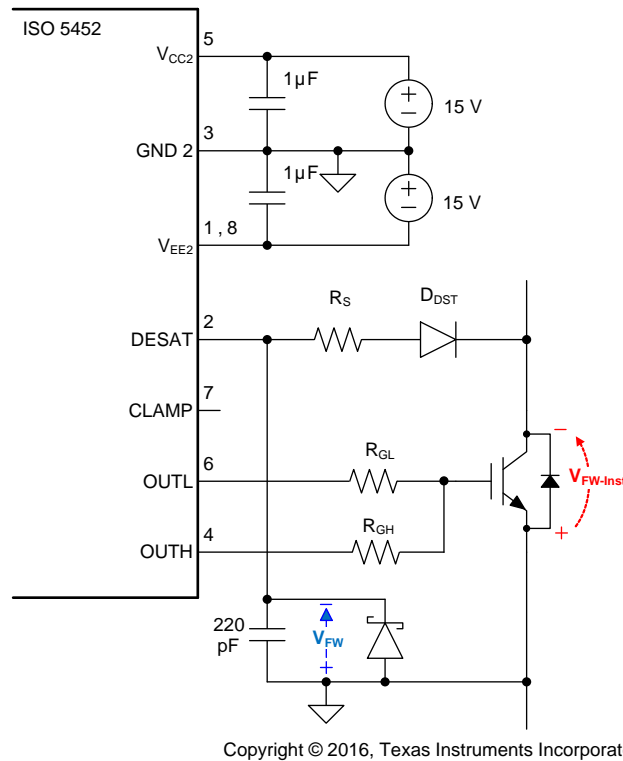


Figure 55. DESAT Pin Protection with Series Resistor and Schottky Diode

10.2.2.8 DESAT Diode and DESAT Threshold

The DESAT function of the diode is used to conduct forward current, allowing sensing of the saturated collector-to-emitter voltage of the IGBT, $V_{(DESAT)}$, (when the IGBT is on) and to block high voltages (when the IGBT is off). During the short transition time when the IGBT is switching, a commonly a high dV_{CE}/dt voltage ramp rate occurs across the IGBT. This results in a charging current $I_{CHARGE} = C_{(D-DESAT)} \times dV_{CE}/dt$, charging the blanking capacitor. $C_{(D-DESAT)}$ is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of $1 + C_{(BLANK)} / C_{(D-DESAT)}$.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{(DESAT)}$, the V_{CE} level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series as shown in Equation 1.

$$V_{CE-FAULT(TH)} = 9 V - n \times V_F$$

where

- n is the number of DESAT diodes (1)

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

10.2.2.9 Determining the Maximum Available, Dynamic Output Power, P_{OD-max}

The ISO5452 maximum allowed total power consumption of $P_D = 251$ mW consists of the total input power, P_{ID} , the total output power, P_{OD} , and the output power under load, P_{OL} :

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (2)$$

With:

$$P_{ID} = V_{CC1-max} \times I_{CC1-max} = 5.5 \text{ V} \times 4.5 \text{ mA} = 24.75 \text{ mW} \quad (3)$$

and:

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{CC2-max} = (15\text{V} - (-8\text{V})) \times 6 \text{ mA} = 138 \text{ mW} \quad (4)$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251 \text{ mW} - 24.75 \text{ mW} - 138 \text{ mW} = 88.25 \text{ mW} \quad (5)$$

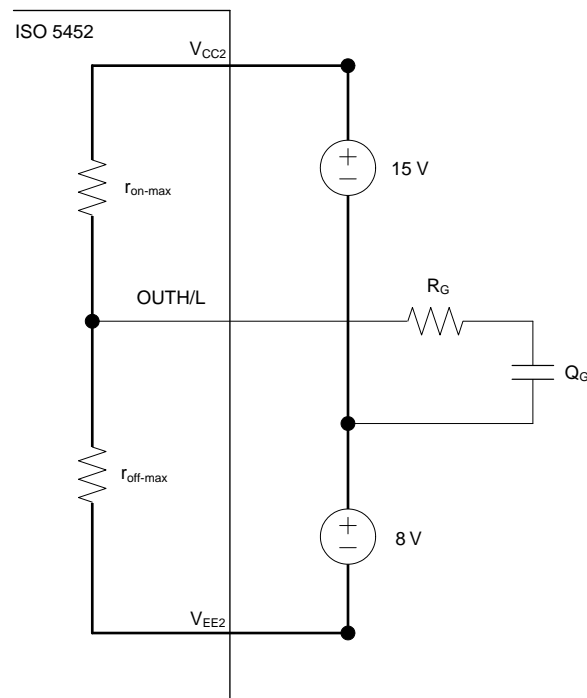
In comparison to P_{OL} , the actual dynamic output power under worst case condition, P_{OL-WC} , depends on a variety of parameters:

$$P_{OL-WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left(\frac{r_{on-max}}{r_{on-max} + R_G} + \frac{r_{off-max}}{r_{off-max} + R_G} \right)$$

where

- f_{INP} = signal frequency at the control input IN+
 - Q_G = power device gate charge
 - V_{CC2} = positive output supply with respect to GND2
 - V_{EE2} = negative output supply with respect to GND2
 - r_{on-max} = worst case output resistance in the on-state: 4 Ω
 - $r_{off-max}$ = worst case output resistance in the off-state: 2.5 Ω
 - R_G = gate resistor
- (6)

When R_G is determined, Equation 6 is to be used to verify whether $P_{OL-WC} < P_{OL}$. Figure 56 shows a simplified output stage model for calculating P_{OL-WC} .



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Figure 56. Simplified Output Model for Calculating P_{OL-WC}

10.2.2.10 Example

This examples considers an IGBT drive with the following parameters:

$$I_{ON-PK} = 2 \text{ A}, Q_G = 650 \text{ nC}, f_{INP} = 20 \text{ kHz}, V_{CC2} = 15\text{V}, V_{EE2} = -8 \text{ V} \tag{7}$$

Apply the value of the gate resistor $R_G = 10 \Omega$.

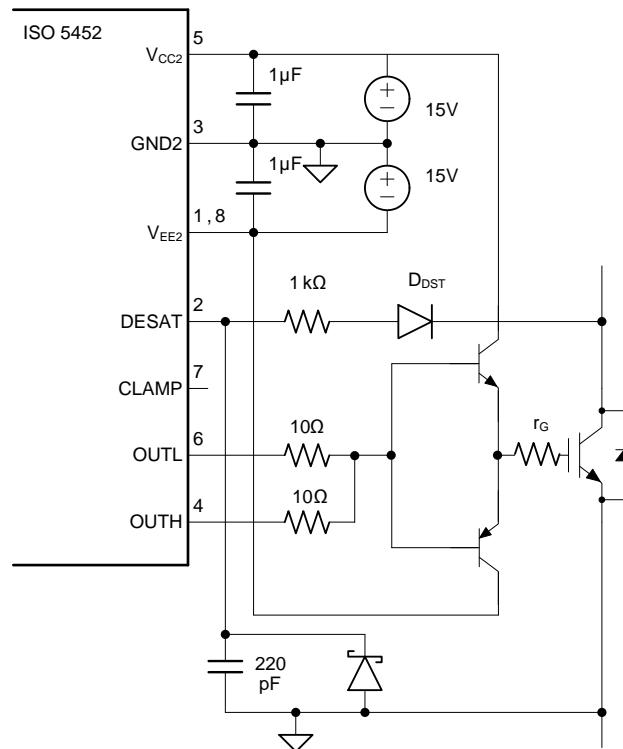
Then, calculating the worst-case output power consumption as a function of R_G , using Equation 6 r_{on-max} = worst case output resistance in the on-state: 4Ω , $r_{off-max}$ = worst case output resistance in the off-state: 2.5Ω , R_G = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20 \text{ kHz} \times 650 \text{ nC} \times (15 \text{ V} - (-8 \text{ V})) \times \left(\frac{4 \Omega}{4 \Omega + 10 \Omega} + \frac{2.5 \Omega}{2.5 \Omega + 10 \Omega} \right) = 72.61 \text{ mW} \tag{8}$$

Because $P_{OL-WC} = 72.61 \text{ mW}$ is less than the calculated maximum of $P_{OL} = 88.25 \text{ mW}$, the resistor value of $R_G = 10 \Omega$ is suitable for this application.

10.2.2.11 Higher Output Current Using an External Current Buffer

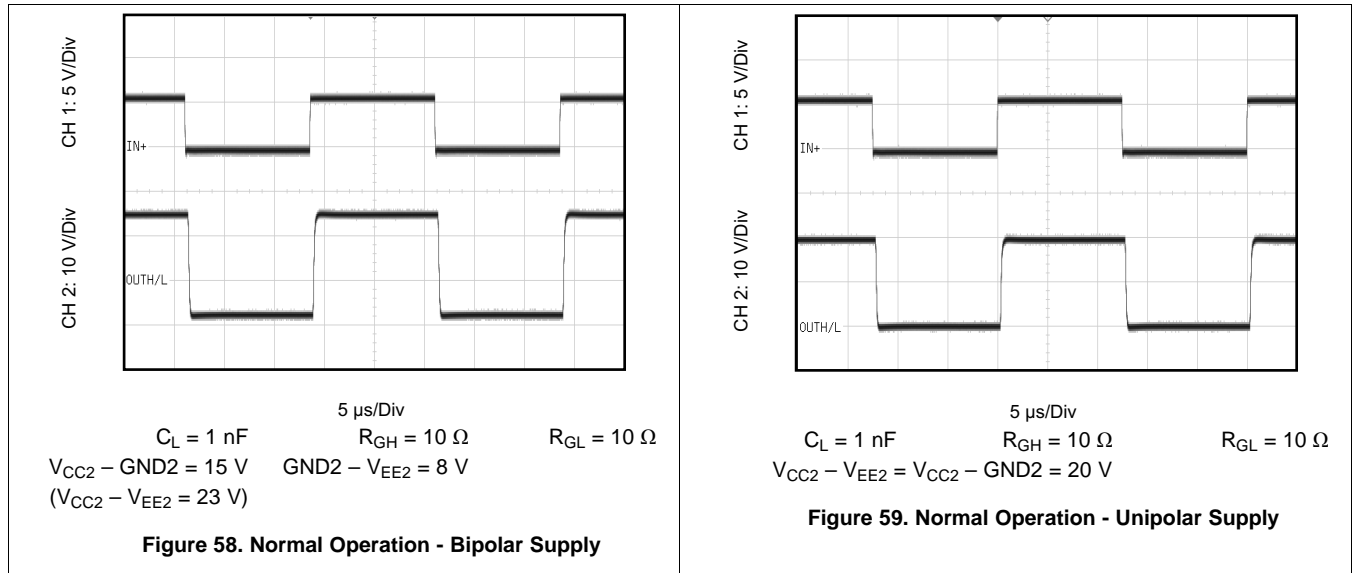
To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 57) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.



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Figure 57. Current Buffer for Increased Drive Current

10.2.3 Application Curves



11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a 0.1- μF bypass capacitor is recommended at the input supply pin, V_{CC1} , and 1- μF bypass capacitor is recommended at the output supply pin, V_{CC2} . The capacitors should be placed as close to the supply pins as possible. The recommended placement of capacitors is 2-mm (maximum) from input and output power supply pin (V_{CC1} and V_{CC2}).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 60](#)). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, gate driver output OUTH and OUTL, and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch². On the gate-driver V_{EE2} and V_{CC2} can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For detailed layout recommendations, see the [Digital Isolator Design Guide](#) (SLLA284).

12.2 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12.3 Layout Example

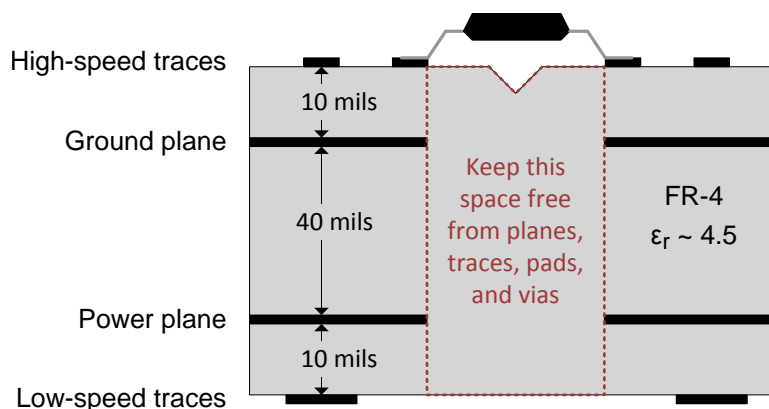


Figure 60. Recommended Layer Stack

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

相关文档如下：

- [《ISO5852S 评估模块 \(EVM\) 用户指南》](#)
- [数字隔离器设计指南](#)
- [隔离相关术语](#)

13.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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13.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

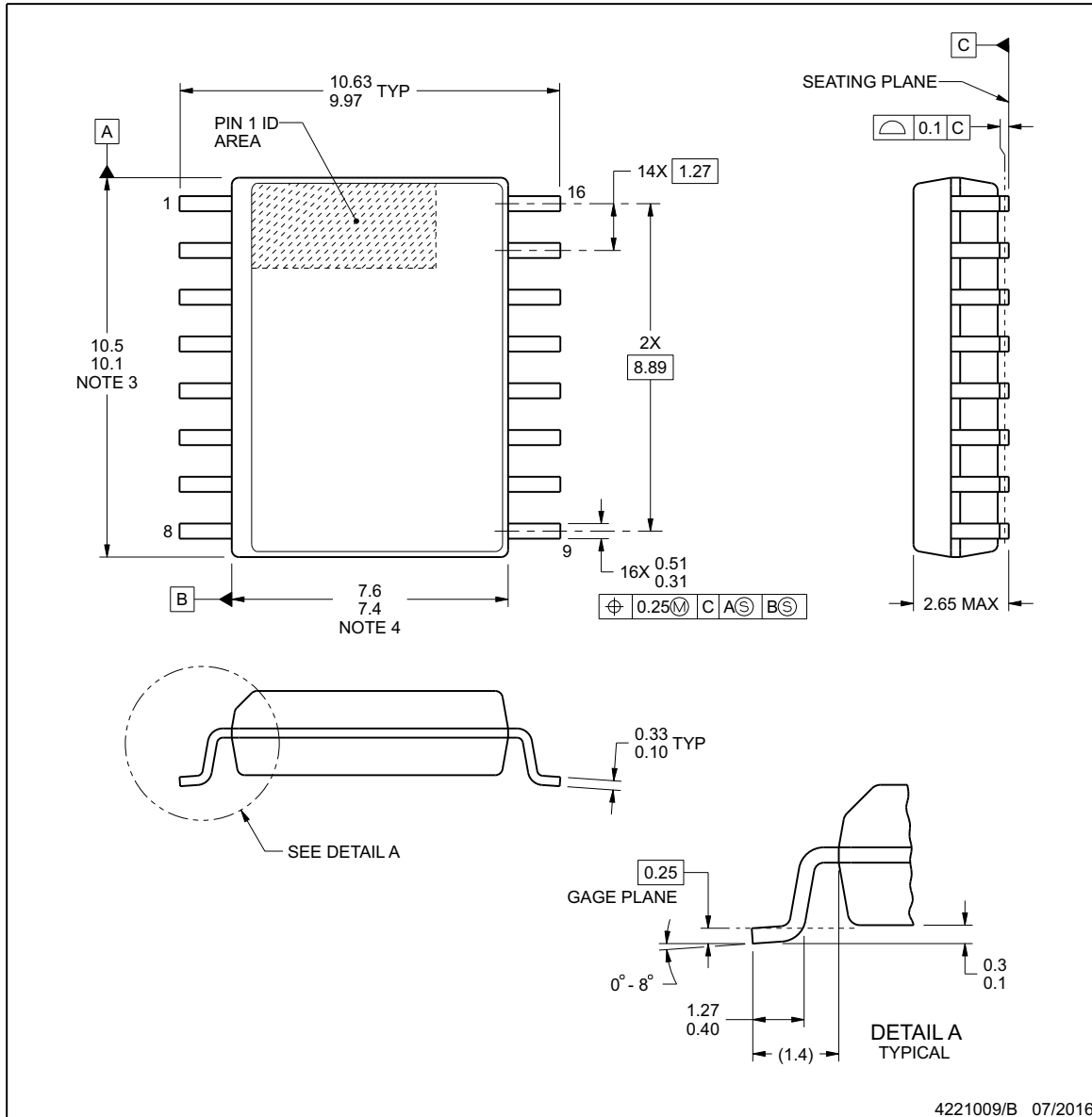


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

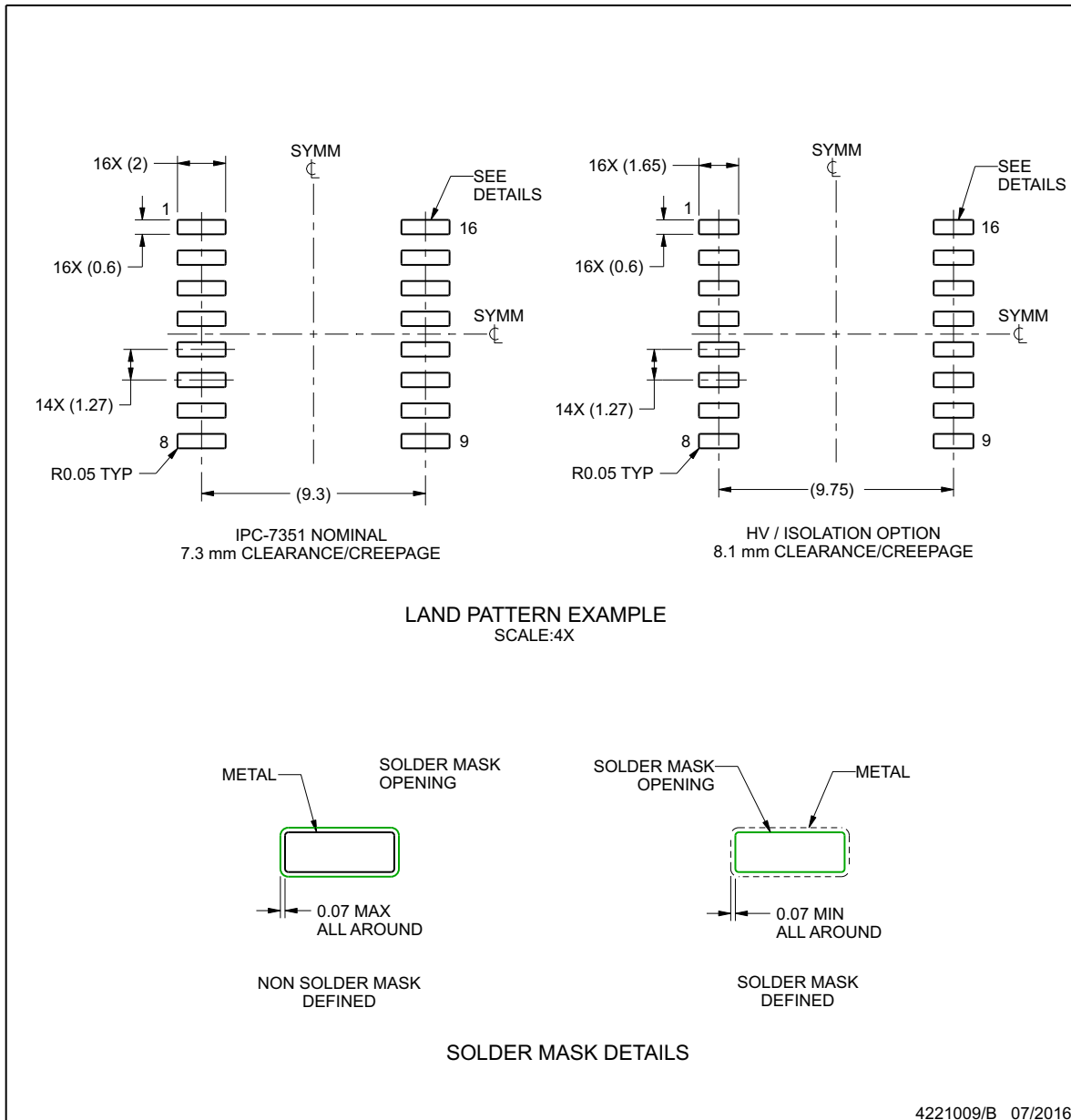
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

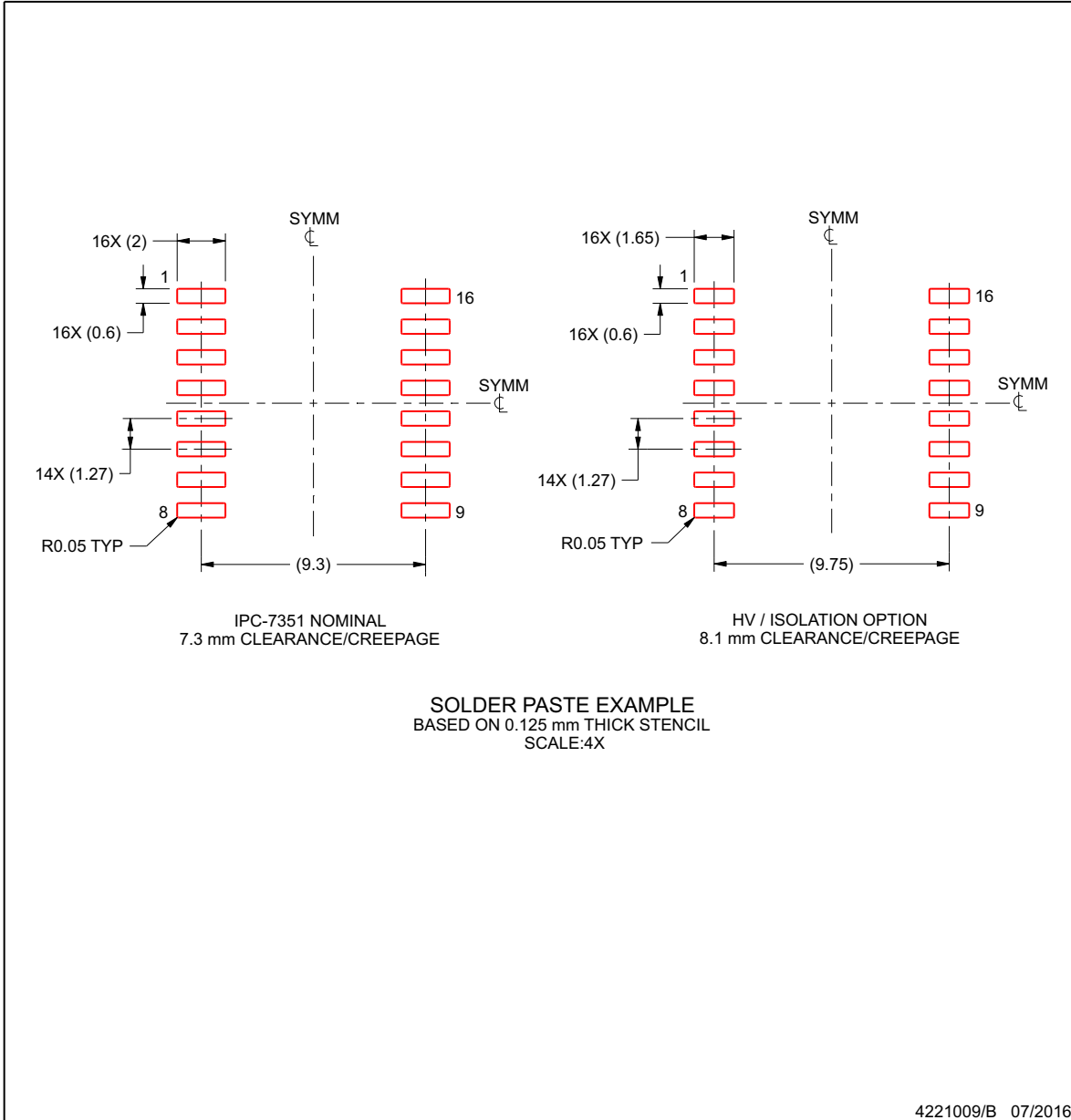
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO5452DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5452	Samples
ISO5452DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5452	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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