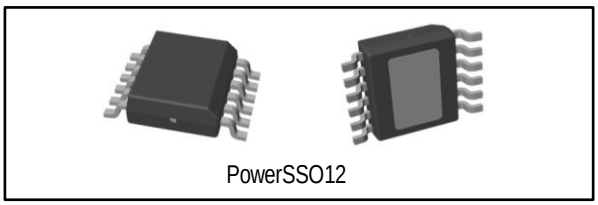
IPS160H

Single high-side switch

Datasheet - preliminary data



Features

$R_{DS(on)}$ max.	I_{OUT}	V_{CC}
0.060 Ω	2.5 A	65 V

- 8 V to 60 V operating voltage range
- Output current limitation: 2.5 A
- Non-dissipative short-circuit protection (cut-off)
- Programmable cut-off delay time using external capacitor
- Diagnostic signalization for: open load diagnostic in off-state, cut-off and junction thermal shutdown
- Fast demagnetization of inductive load
- Ground disconnection protection
- V_{CC} disconnection protection
- Undervoltage lock-out
- Designed to meet IEC 61131-2
- PSSO12 package

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- SIL applications

Description

The IPS160H is a monolithic device able to drive capacitive, resistive or inductive loads, with one side connected to ground; it is specifically designed to match safety integrity level (SIL) applications.

Built-in thermal shutdown protects the chip against overtemperature and short-circuit. In order to minimize the power dissipation, when the output is shorted a non-dissipative short-circuit protection is implemented, to limit the output average current value and to contain the device overheating. A fully diagnostic provides junction thermal shutdown, open load, and cut-off protection. A diagnostic pin provides information about the faults described above.

Cut-off delay time value can be programmed by an external capacitor.

Table 1: Device summary

Order code	Package	Packing
IPS160H	PowerSSO12	Tube
IPS160HTR	PowerSSO12	Tape and reel

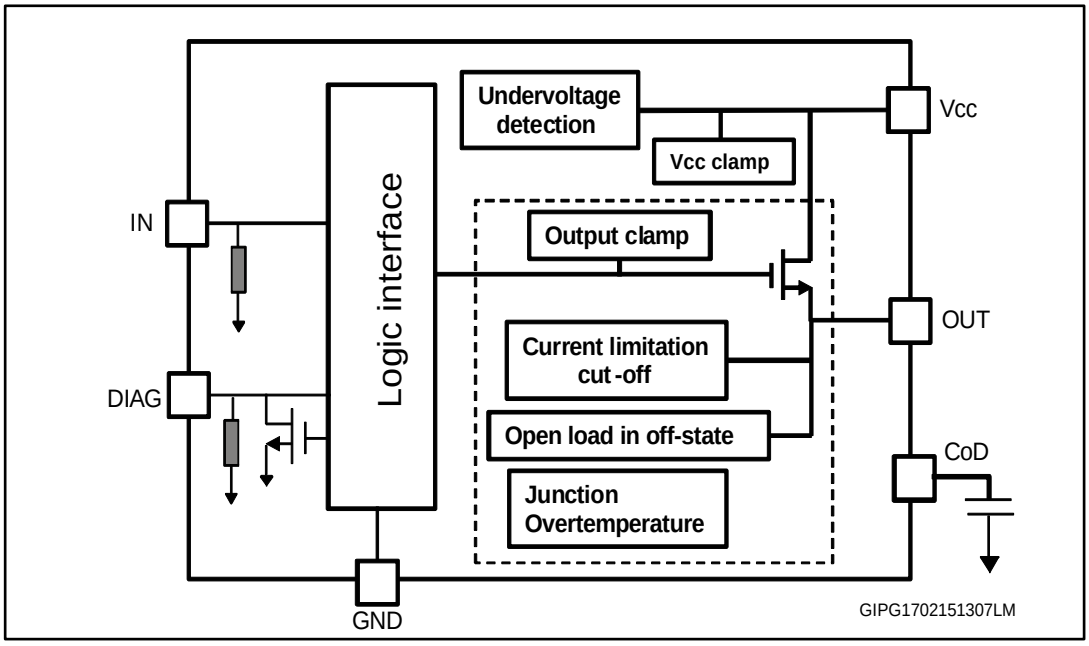
Contents

List of tables

List of figures

1 Block diagram

Figure 1: Block diagram



2 Pin description

Figure 2: Pin connection (top view)

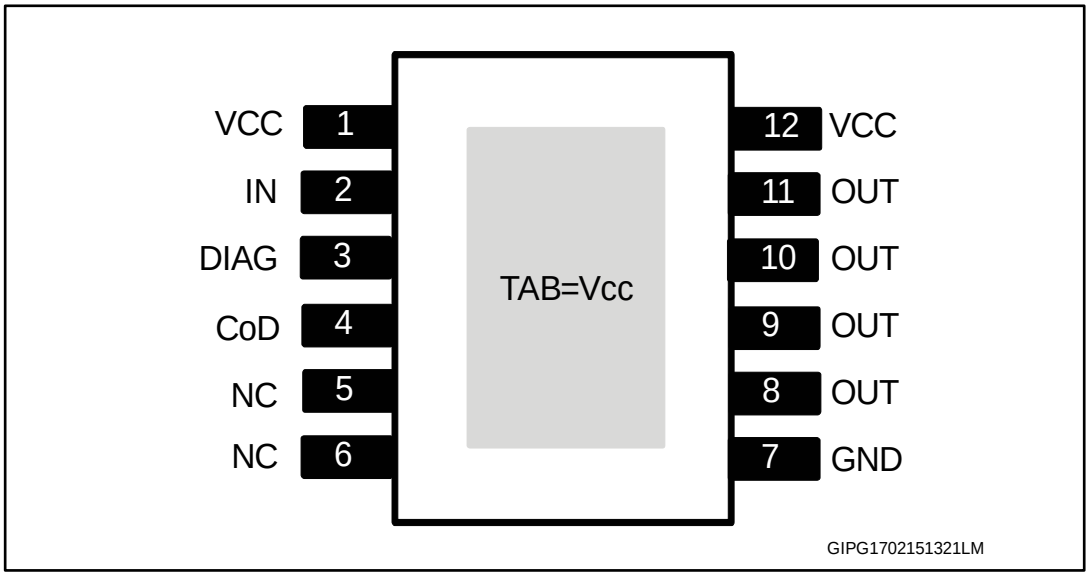


Table 2: Pin configuration

Number	Name	Function	Type
5,6	NC	Not connected	
2	IN	Channel input	Input
3	DIAG	Common diagnostic pin both for thermal shutdown, cut-off and open load	Output open drain
4	CoD	Programmable cut-off intervention delay during overcurrent operation. It cannot be left floating: it is connected by a 10 kΩ resistor to GND to disable the cut-off function or a capacitor has to be connected between CoD and GND to set delay	Input
7	GND	Device ground	Ground
8,9,10,11	OUT	Channel power stage output	Output
1,12 TAB	VCC	Device supply voltage	Supply

2.1 IN

This pin drives the output stage to pin OUT. IN pin has internal weak pull-down resistors, see *Table 8: "Logic inputs"*.

2.2 OUT

Output power transistor is in high-side configuration, with active clamp for fast demagnetization.

2.3 DIAG

This pin is used for diagnostic purpose and it is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown, cut-off, or open load in off-state.

2.4 CoD

This pin cannot be left floating and can be used to program the cut-off delay time t_{coff}, see*Table 9: "Protection and diagnostic"* through an external capacitor (C_{CoD}). The cut-off function can be completely disabled connecting the CoD pin to GND through 10 kΩ resistor: in this condition the output channel remains on in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered.

2.5 GND

IC ground.

2.6 VCC

IC supply voltage.

3 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 65	V
V_{OUT}	Output channel voltage	V_{cc}-V_{clamp} to V_{cc}+0.3	V
I_{IN}	Input current	-10/+10	mA
V_{IN}	IN voltage	V_{CC}	V
V_{COD}	Output cut-off voltage pin	5.5	V
I_{COD}	Input current on cut-off pin	-1/+10	mA
V_{DIAG}	Fault voltage	V_{CC}	V
I_{GND}	Ground disconnection	1	mA
I_{CC}	Maximum DC reverse current	-250	
I_{DIAG}	Fault current	-10/+10	
I_{OUT}	Output stage current	Internally limited	A
$-I_{OUT}$	Reverse output current	5	
E_{AS}	Single pulse avalanche energy per channel not simultaneously L = 1.15 H I_{OUT} = 0.5 A	TBD	mJ
P_{TOT}	Power dissipation at T_C = 25 °C ($T_{JSD(MAX)}$-25)/ $R_{th(JA)}$)	Internally limited	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature	-40 to 150	

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case per channel	TBD	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient		

Package mounted on a 4-layer board, CU thickness 35 micron, with 6 vias on the exposed pad copper area connected to an inner power plane. $R_{th(JA)}$ = … ºC/W without heatsink.

4 Electrical characteristics

(8 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 5: Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		V_{UVON}		60	
V_{UVON}	Undervoltage on threshold		6.9		8	
V_{UVOFF}	Undervoltage off threshold		6.5		7.8	
V_{UVH}	Undervoltage hysteresis		0.15	0.5		
I_S	Supply current in off-state	V_{CC} = 24 V		100	200	µA
	Supply current in on-state			0.7	1.4	mA

Table 6: Output stage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	On-state resistance	V_{CC} = 24 V I_{OUT} =1 A @ T_J = 25 °C		60		mΩ
		V_{CC} = 24 V I_{OUT} =1 A @ T_J = 125 °C			120	
$V_{OUT(OFF)}$	Off-state output voltage	V_{IN} = 0 V and I_{OUT} = 0 A			2	V
$I_{OUT(OFF)}$	Off-state output current	V_{IN} = 0 V, V_{OUT} = 0 V	5		5	µA
$I_{OUT(OFF-min)}$	Off-state output current	V_{IN} = 0 V, V_{OUT} = 4 V	-35		0	

Table 7: Switching

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r	Rise time	I_{OUT} = 1 A per channel		10		µs
t_f	Fall time	I_{OUT} = 1 A per channel		10		
$t_{PD(H-L)}$	Propagation delay time off	I_{OUT} = 1 A per channel		20		
$t_{PD(L-H)}$	Propagation delay time on	I_{OUT} = 1 A per channel		30		

Figure 3: t_{rise} and t_{fall}

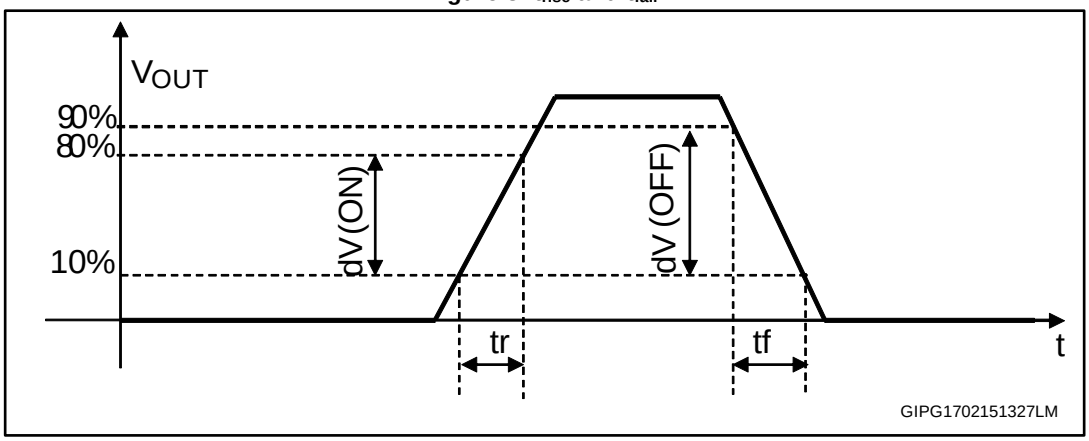


Figure 4: $t_{PD(H-L)}$ and $t_{PD(L-H)}$

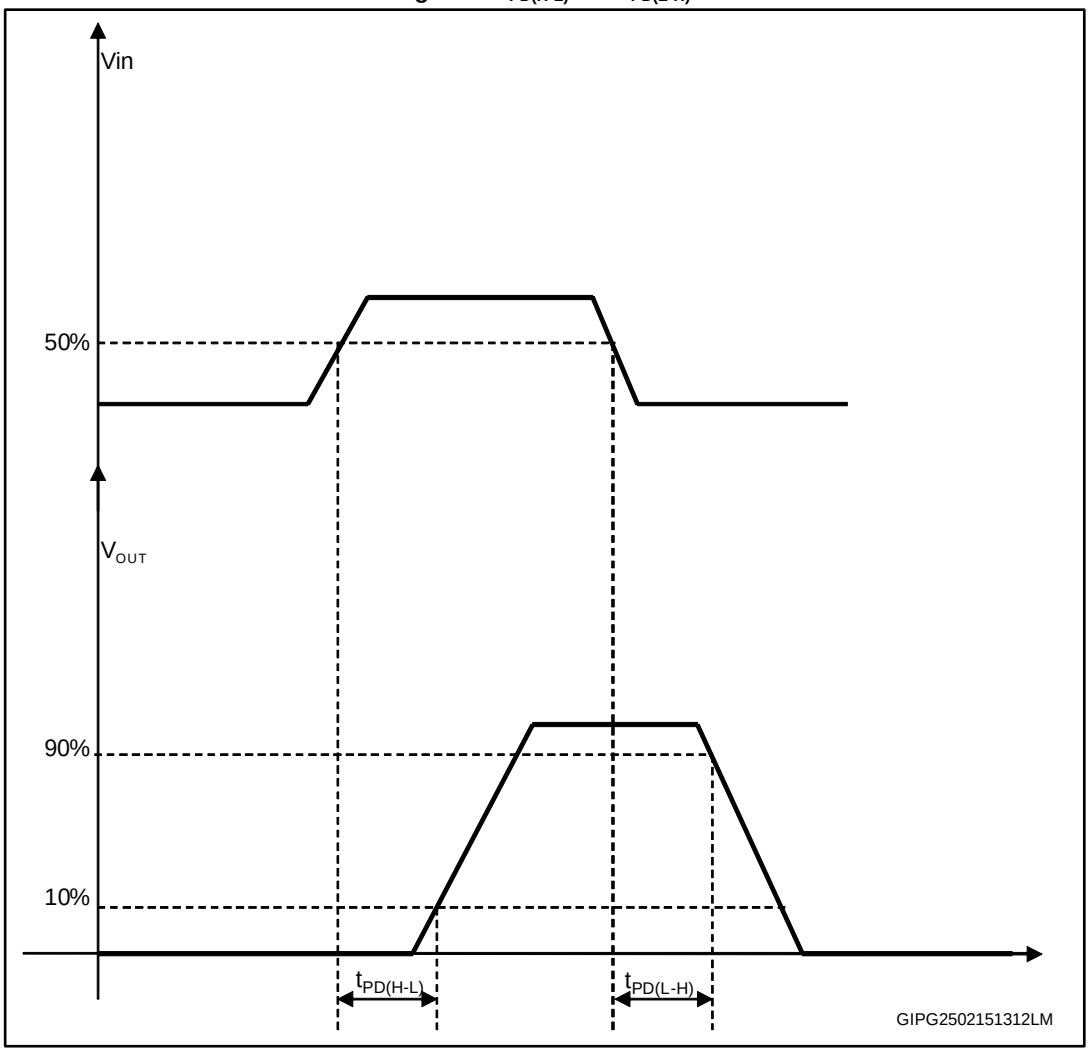


Table 8: Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.2			
$V_{I(HYST)}$	Input hysteresis voltage			0.4		
I_{IN}	Input current	V_{IN} = 36 V			200	µA

Table 9: Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{CC} active clamp	I_{CC} = 10 mA	65.5	68	70	V
V_{demag}	Demagnetization voltage	I_{OUT} =0.5 A; load =1 mH	V_{CC}-70	V_{CC}-68	V_{CC}-65	
V_{OLoff}	Open load (off-state) or short to V_{CC} detection threshold		2		4	
t_{BKT}	Open load blanking time				200	µA
V_{DIAG}	Voltage drop on DIAG	I_{DIAG}=4 mA			1	V
I_{DIAG}	DIAG pin leakage current	V_{CC} ≤ 36 V			60	µA
I_{LIM}	Output current limitation	R_{LOAD} ≤ 10 mΩ	2.6		4.2	A
t_{coff}	Cut-off current delay time	Programmable by external capacitor on CoD pin with capacitor in the range: 10 nF ≤ C_{COD} ≤ 100 nF	$(50x10^3xC_{COD})$ ± 35%			µs
		Cut-off disabled when CoD pin is connected to GND through 10 kΩ resistor	Output in current limitation without cut-off			
t_{res}	Output stage restart delay time		$32xt_{coff}$ ± 40%			
I_{GND}	GND disconnection output current	V_{IN} = V_{CC} = 24 V V_{OUT} = 0 V			1	mA
T_{JSD}	Junction temperature shutdown		150	170	190	°C
T_{JHYST}	Junction temperature thermal hysteresis			15		

5 Output logic

Table 10: Output stage truth table

Operation	IN	OUT	DIAG
Normal	L H	L H	H H
Cut-off	L H	L L	L L
Overtemperature	L H	L L	L L
Open load	L H	H (external pull-up resistor is used) H	L (external pull-up resistor is used) H
UVLO	X X	L L	X X

6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold. Normal operation restarts after V_{CC} exceeds the turn-on threshold. Turn-on and turn-off thresholds are defined in *Table 5: "Supply"*.

6.2 Overtemperature

The output stage of each channel turns off when its internal junction temperature (T_J) exceeds the shutdown threshold. Normal operation restarts when T_J comes back below the reset threshold, see *Table 9: "Protection and diagnostic"*. The internal fault signal is set when the channel is off due to thermal protection and it is reset when the junction triggers the reset threshold. This same behavior is reported on DIAG pin.

6.3 Cut-off

The output current of the power stage is internally limited and the fixed I_{LIM} threshold.

The IPS160H implements the cut-off feature which limits the duration of the current limitation condition.

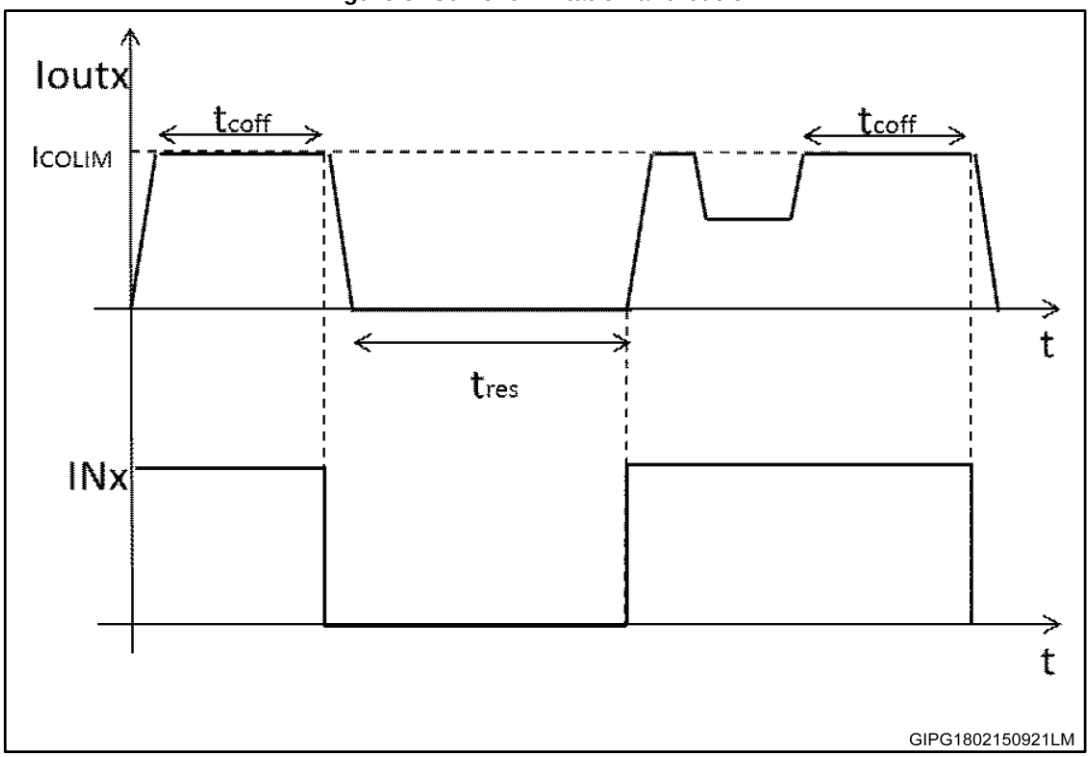
The duration of the current limitation condition (T_{coff}) can be set by a capacitor (C_{CoD}) placed between CoD and GND pins. The design rule for C_{CoD} is:

$T_{coff} = 50 \times 10^3 \times C_{COD}$

The above design rule is valid in the range 1 nF ≤ C_{CoD} ≤ 100 nF.

If I_{LIM} threshold is triggered, the output stage remains in the current limitation condition ($I_{OUT} = I_{LIM}$) at least for t_{coff}. If t_{coff} elapses, the output stage turns off and restarts after the t_{res} restart time.

Figure 5: Current limitation and cut-off



The fault condition is reported on the DIAG pin. The internal cut-off flag signal is latched at output switch-off and released after the time t_{res}, the same behavior is reported on DIAG pin.

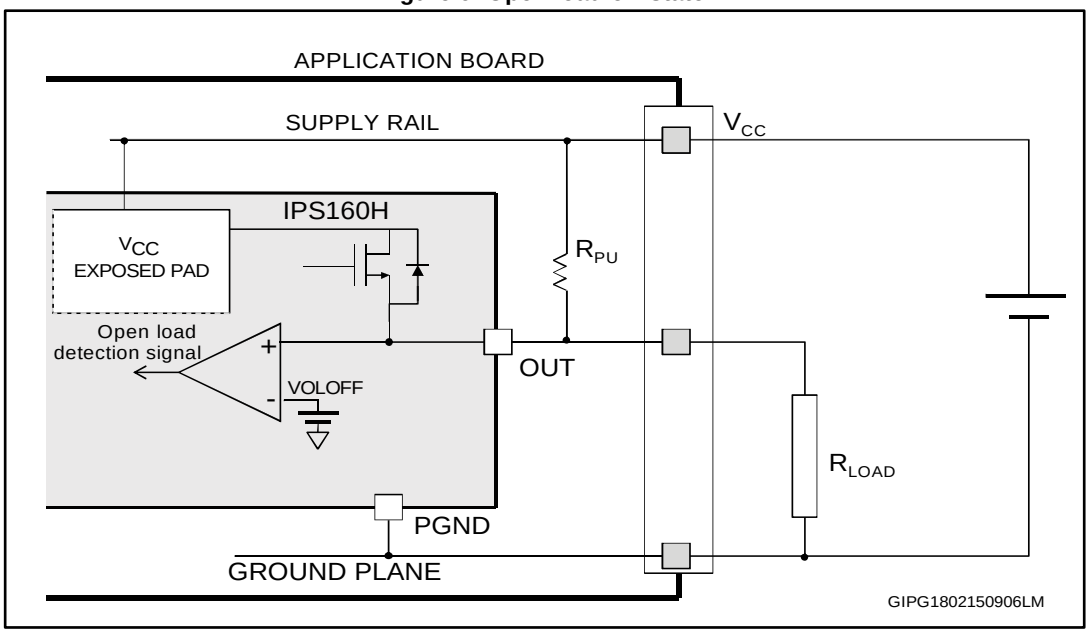
The status of the DIAG is independent on the IN pin status.

If CoD pin is connected to GND through 10 kΩ resistor (cut-off feature disabled), when the output channel triggers the limitation threshold, it remains on, in current limitation condition, until the input becomes LOW or the thermal protection threshold is triggered.

6.4 Open load in off-state

The IPS160H provides the open load detection feature which detects if the load is disconnected from the OUT pin. This feature can be activated by a resistor (RPU) between OUT and VCC pins.

Figure 6: Open load off-state



In case of wire break, the output voltage VOUT rises according to the external pull-up resistor and the internal resistance of the IC.

The $V_{OLoff(min)}$ (open load off-state detection voltage threshold) defines the maximum R_{LOAD} as follows:

$$R_{LOAD} < \frac{R_{PU} \times V_{OLmin}}{(V_{CC}-V_{OLmin})}$$

The $V_{OLoff(max)}$ and the $I_{OUToff(min)}$ define the maximum R_{PU} as follows:

$$R_{PU} < \frac{V_{CC} - V_{OLmin}}{I_{OUToff\ min}}$$

The fault condition is reported on the DIAG pin and the fault reset occurs when load is reconnected.

If the channel is switched on by IN pin, the fault condition is no longer detected.

When inductive load are driven, some ringing of the output voltage may be observed at the end of the demagnetization. In fact, the load is completely demagnetized when I_{LOAD} = 0 A and the OUT pin remains floating until next turn-on. In order to avoid a fake signalization of the open load event driving inductive loads, the open load signal is masked for t_{BKT}. So, the open load is reported on the DIAG pin with a delay of t_{BKT} and if the open load event is triggered for more than t_{BKT}.

6.5 V_{CC} disconnection protection

V_{CC} disconnection is the disconnection of the V_{CC} board supply. When this condition is detected, all the output channels turn off independently on the input status.

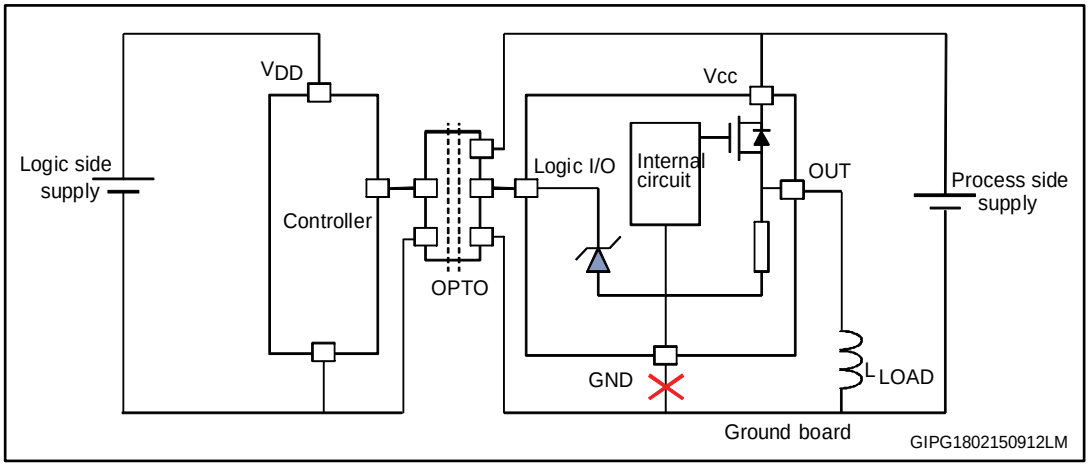
In case of inductive load, if V_{CC} is disconnected while one or more channels are active, the current flows through the power, which is active due to the active clamp as if the input has been deactivated.

6.6 GND disconnection protection

GND disconnection is the disconnection of the board supply ground. When this condition is detected, all output channels turn off independently on the input status.

The maximum steady-state current measured through a channel in short to GND is not greater than IGD, see *Table 9: "Protection and diagnostic"*. The same behavior is guaranteed when all channels are simultaneously in short to GND. In case of inductive load, if the GND is disconnected while the output channel is active, the current flows through the power, which is active due to the active clamp as if the input has been deactivated.

Figure 7: Ground disconnection

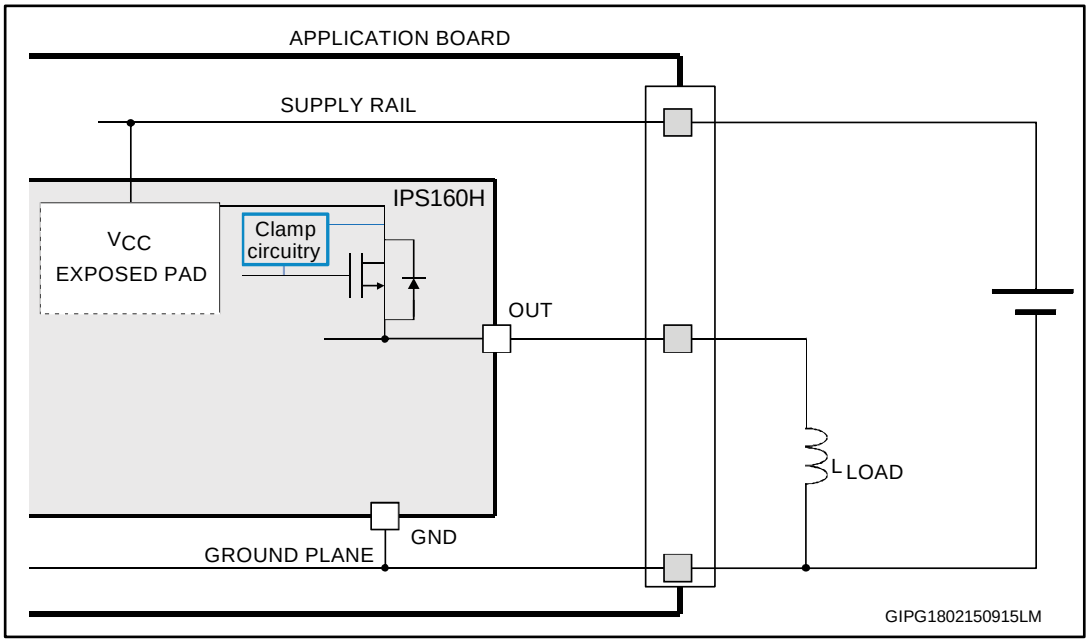


7 Active clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage on output is detected.

The OUT pin is pulled down to V_{demag}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at about V_{demag} until the load energy has been dissipated. The energy is dissipated both in IC internal switch and in load resistance.

Figure 8: Active clamp equivalent principle schematic



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 PowerSSO12 package information

Figure 9: PowerSSO12 package outline

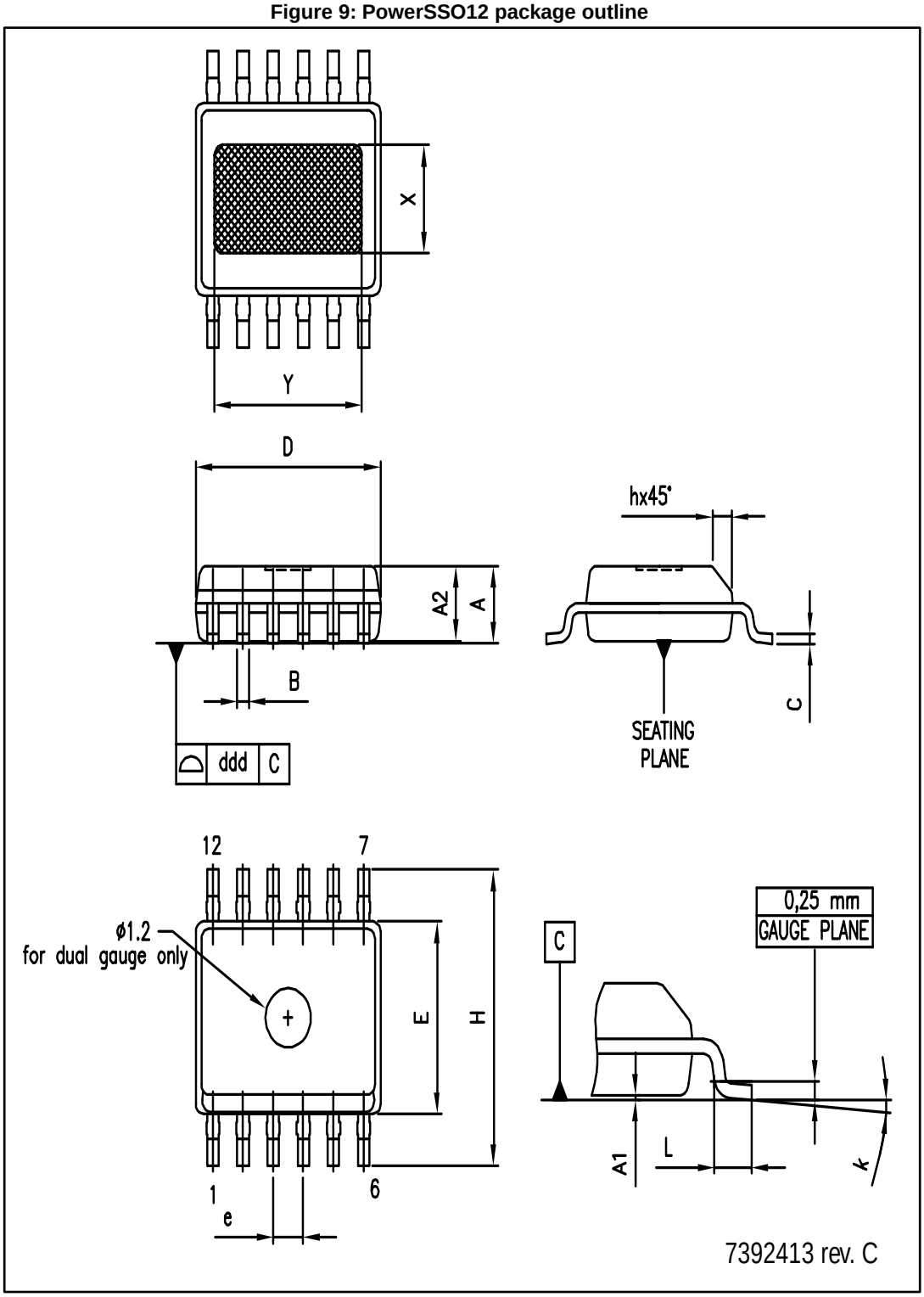


Table 11: PowerSSO12 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5000
E	3.800		4000
e		0.800	
H	5800		6.200
h	0.250		1.270
L	0.400	0.195	
k	0d	0.2	8d
X	1.900		2500
Y	3.600		4.200
ddd			0.100

Dimension D doesn't include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs don't exceed 0.15 mm in total both side.

9 Revision history

Table 12: Document revision history

Date	Revision	Changes
19-Mar-2015	1	Initial release.

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