

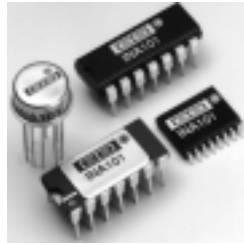
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Jameco Part Number 1340592



**INA101**

## High Accuracy INSTRUMENTATION AMPLIFIER

### FEATURES

- **LOW DRIFT:** 0.25 $\mu$ V/ $^{\circ}$ C max
- **LOW OFFSET VOLTAGE:** 25 $\mu$ V max
- **LOW NONLINEARITY:** 0.002%
- **LOW NOISE:** 13nV/ $\sqrt{\text{Hz}}$
- **HIGH CMR:** 106dB AT 60Hz
- **HIGH INPUT IMPEDANCE:** 10<sup>10</sup> $\Omega$
- **14-PIN PLASTIC, CERAMIC DIP, SOL-16, AND TO-100 PACKAGES**

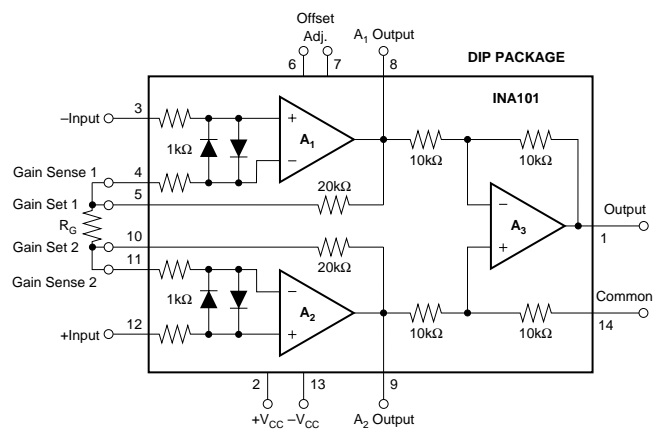
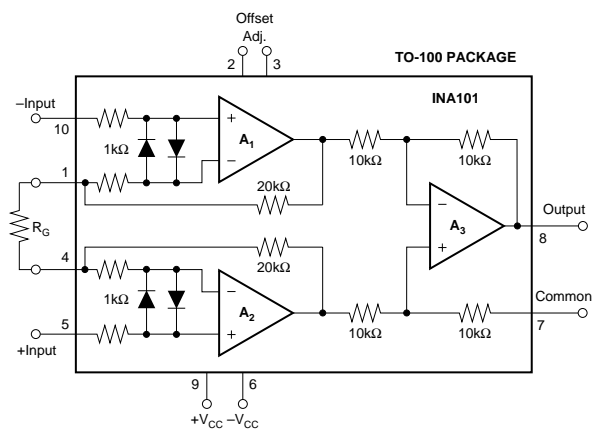
### APPLICATIONS

- **STRAIN GAGES**
- **THERMOCOUPLES**
- **RTDs**
- **REMOTE TRANSDUCERS**
- **LOW-LEVEL SIGNALS**
- **MEDICAL INSTRUMENTATION**

### DESCRIPTION

The INA101 is a high accuracy instrumentation amplifier designed for low-level signal amplification and general purpose data acquisition. Three precision op amps and laser-trimmed metal film resistors are integrated on a single monolithic integrated circuit.

The INA101 is packaged in TO-100 metal, 14-pin plastic and ceramic DIP, and SOL-16 surface-mount packages. Commercial, industrial and military temperature range models are available.



# SPECIFICATIONS

## ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 1, unless otherwise noted.

PARAMETER	INA101AM, AG			INA101SM, SG			INA101CM, CG			INA101HP, KU			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>GAIN</b>	1			*			*			*			V/V
Range of Gain			1000	*	*	*	*	*	*	*	*	*	V/V
Gain Equation		$G = 1 + (40k/R_G)$			*	*	*	*	*	*	*	*	%
Error from Equation, DC <sup>(1)</sup>		$\pm(0.04 + 0.00016G - 0.02/G)$	$\pm(0.1 + 0.0003G - 0.05/G)$		*	*	*	*	*	$\pm(0.1 + 0.00015G - 0.05/G)$	$\pm(0.3 + 0.0002G - 0.10/G)$	*	
Gain Temp. Coefficient <sup>(3)</sup>					*	*	*	*	*	*	*	*	ppm/°C
G = 1		2	5		*	*	*	*	*	*	*	*	ppm/°C
G = 10		20	100		*	*	*	*	*	*	*	*	ppm/°C
G = 100		22	110		*	*	*	*	*	*	*	*	ppm/°C
G = 1000		22	110		*	*	*	*	*	*	*	*	ppm/°C
Nonlinearity, DC <sup>(2)</sup>		$\pm(0.002 + 10^{-5} G)$	$\pm(0.005 + 2 \times 10^{-5} G)$		$\pm(0.001 + 10^{-5} G)$	$\pm(0.002 + 10^{-5} G)$		$\pm(0.001 + 10^{-5} G)$	$\pm(0.002 + 10^{-5} G)$		*	*	% of p-p FS
<b>RATED OUTPUT</b>													V
Voltage	±10	±12.5		*	*	*	*	*	*	*	*	*	V
Current	±5	±10		*	*	*	*	*	*	*	*	*	mA
Output Impedance		0.2			*	*		*	*		*	*	Ω
Capacitive Load		1000			*	*		*	*		*	*	pF
<b>INPUT OFFSET VOLTAGE</b>													μV
Initial Offset at +25°C		±(25 + 200/G)	±(50 + 400/G)		±10+100/G	±(25 + 200/G)		±(10+100/G)	±(25 + 200/G)		±(125 + 450/G)	±(250 + 900/G)	μV
vs Temperature			±(2 + 20/G)			±(0.75 + 10/G)			±(0.25 + 10/G)		±(2 + 20/G)		μV/°C
vs Supply		±(1 + 20/G)			*	*		*	*		*	*	μV/V
vs Time		±(1 + 20/G)			*	*		*	*		*	*	μV/mo
<b>INPUT BIAS CURRENT</b>													nA
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.2			*	*		*	*		*	*	nA/°C
vs Supply		±0.1			*	*		*	*		*	*	nA/V
Initial Offset Current		±15	±30		±10	*		±5	±20		*	*	nA
vs Temperature		±0.5			*	*		*	*		*	*	nA/°C
<b>INPUT IMPEDANCE</b>													Ω    pF
Differential		10 <sup>10</sup>    3			*	*		*	*		*	*	Ω    pF
Common-mode		10 <sup>10</sup>    3			*	*		*	*		*	*	Ω    pF
<b>INPUT VOLTAGE RANGE</b>													V
Range, Linear Response	±10	±12		*	*	*	*	*	*	*	*	*	V
CMR with 1kΩ Source Imbalance					*	*		*	*		*	*	dB
DC to 60Hz, G = 1	80	90			*	*		*	*	65	85		dB
DC to 60Hz, G = 10	96	106			*	*		*	*	90	95		dB
DC to 60Hz, G = 100 to 1000	106	110			*	*		*	*	100	105		dB
<b>INPUT NOISE</b>													μV, p-p
Input Voltage Noise					*	*		*	*		*	*	μV, p-p
f <sub>B</sub> = 0.01Hz to 10Hz		0.8			*	*		*	*		*	*	μV, p-p
Density, G = 1000					*	*		*	*		*	*	nV/√Hz
f <sub>O</sub> = 10Hz		18			*	*		*	*		*	*	nV/√Hz
f <sub>O</sub> = 100Hz		15			*	*		*	*		*	*	nV/√Hz
f <sub>O</sub> = 1kHz		13			*	*		*	*		*	*	nV/√Hz
Input Current Noise					*	*		*	*		*	*	pA, p-p
f <sub>B</sub> = 0.01Hz to 10Hz		50			*	*		*	*		*	*	pA, p-p
Density					*	*		*	*		*	*	pA/√Hz
f <sub>O</sub> = 10Hz		0.8			*	*		*	*		*	*	pA/√Hz
f <sub>O</sub> = 100Hz		0.46			*	*		*	*		*	*	pA/√Hz
f <sub>O</sub> = 1kHz		0.35			*	*		*	*		*	*	pA/√Hz
<b>DYNAMIC RESPONSE</b>													kHz
Small Signal, ±3dB Flatness					*	*		*	*		*	*	kHz
G = 1		300			*	*		*	*		*	*	kHz
G = 10		140			*	*		*	*		*	*	kHz
G = 100		25			*	*		*	*		*	*	kHz
G = 1000		2.5			*	*		*	*		*	*	kHz
Small Signal, ±1% Flatness					*	*		*	*		*	*	kHz
G = 1		20			*	*		*	*		*	*	kHz
G = 10		10			*	*		*	*		*	*	kHz
G = 100		1			*	*		*	*		*	*	Hz
G = 1000		200			*	*		*	*		*	*	Hz
Full Power, G = 1 to 100		6.4			*	*		*	*		*	*	kHz
Slew Rate, G = 1 to 100	0.2	0.4		*	*	*	*	*	*	*	*	*	V/μs
Settling Time (0.1%)					*	*		*	*		*	*	μs
G = 1		30	40		*	*		*	*		*	*	μs
G = 100		40	55		*	*		*	*		*	*	μs
G = 1000		350	470		*	*		*	*		*	*	μs
Settling Time (0.01%)					*	*		*	*		*	*	μs
G = 1		30	45		*	*		*	*		*	*	μs
G = 100		50	70		*	*		*	*		*	*	μs
G = 1000		500	650		*	*		*	*		*	*	μs
<b>POWER SUPPLY</b>													V
Rated Voltage		±15		*	*	*	*	*	*	*	*	*	V
Voltage Range	±5		±20	*	*	*	*	*	*	*	*	*	V
Current, Quiescent <sup>(2)</sup>		±6.7	±8.5		*	*		*	*		*	*	mA
<b>TEMPERATURE RANGE<sup>(6)</sup></b>													°C
Specification	-25		+85	-55		+125	*	*	*	0		+70	°C
Operation	-55		+125	*		*	*	*	*	-25		+85	°C
Storage	-65		+150	*		*	*	*	*	-40		+85	°C

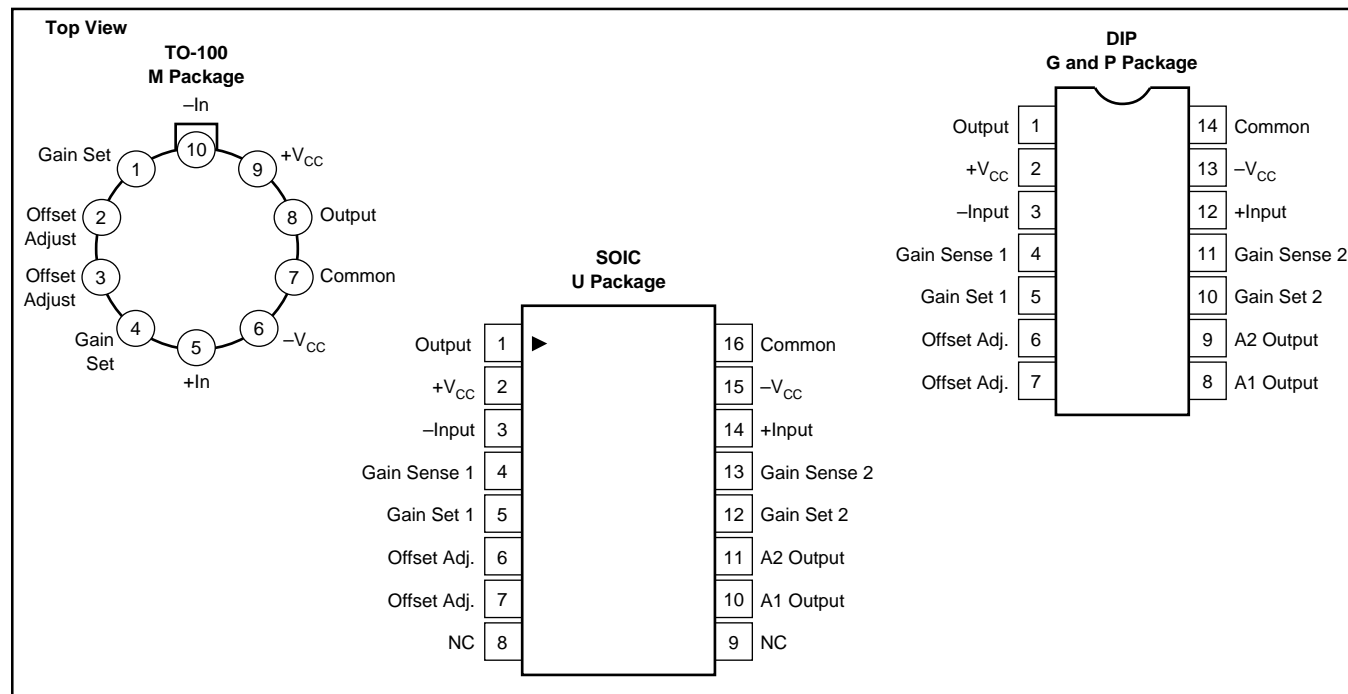
\* Specifications same as for INA101AM, AG.

NOTES: (1) Typically the tolerance of R<sub>G</sub> will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R<sub>G</sub>. (4) Adjustable to zero at any one gain. (5) θ<sub>IC</sub> output stage = 113°C/W, θ<sub>IC</sub> quiescent circuitry = 19°C/W, θ<sub>CA</sub> = 83°C/W.



INA101

## PIN CONFIGURATIONS



## ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
INA101AM	10-Pin Metal TO-100	-25°C to +85°C
INA101CM	10-Pin Metal TO-100	-25°C to +85°C
INA101AG	14-Pin Ceramic DIP	-25°C to +85°C
INA101CG	14-Pin Ceramic DIP	-25°C to +85°C
INA101HP	14-Pin Plastic DIP	0°C to +70°C
INA101KU	SOL-16 Surface-Mount	0°C to +70°C
INA101SG	14-Pin Ceramic DIP	-55°C to +125°C
INA101SM	10-Pin Metal TO-100	-55°C to +125°C

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	±20V
Power Dissipation .....	600mW
Input Voltage Range .....	±V <sub>CC</sub>
Output Short Circuit (to ground) .....	Continuous
Operating Temperature M, G Package .....	-55°C to +125°C
P, U Package .....	-25°C to +85°C
Storage Temperature M, G Package .....	-65°C to +150°C
P, U Package .....	-40°C to +85°C
Lead Temperature (soldering, 10s) M, G, P Package .....	+300°C
Lead Temperature (wave soldering, 3s) U Package .....	+260°C

## PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
INA101AM	10-Pin Metal TO-100	007
INA101CM	10-Pin Metal TO-100	007
INA101AG	14-Pin Ceramic DIP	169
INA101CG	14-Pin Ceramic DIP	169
INA101HP	14-Pin Plastic DIP	010
INA101KU	SOL-16 Surface-Mount	211
INA101SG	14-Pin Ceramic DIP	169
INA101SM	10-Pin Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



## ELECTROSTATIC DISCHARGE SENSITIVITY

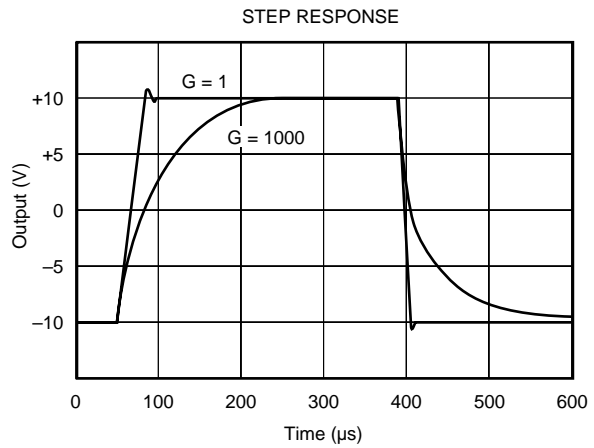
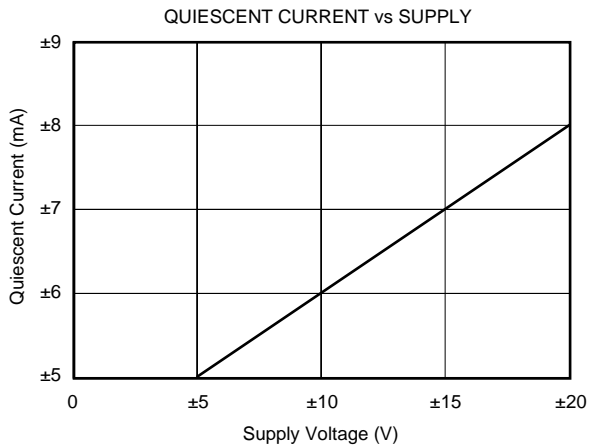
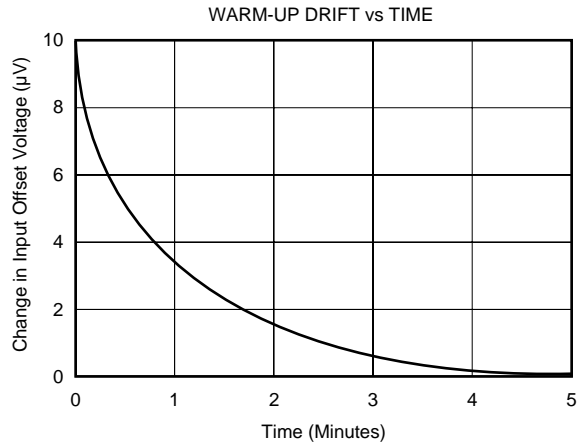
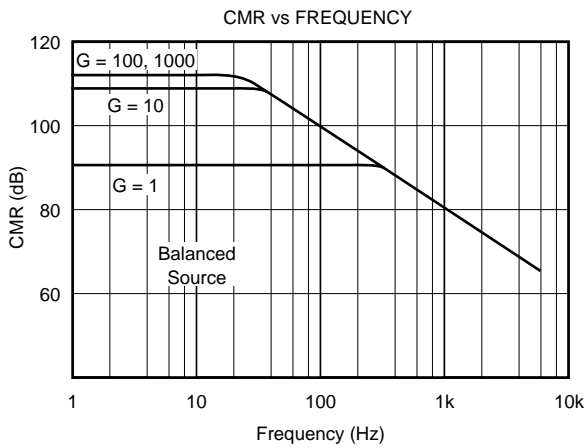
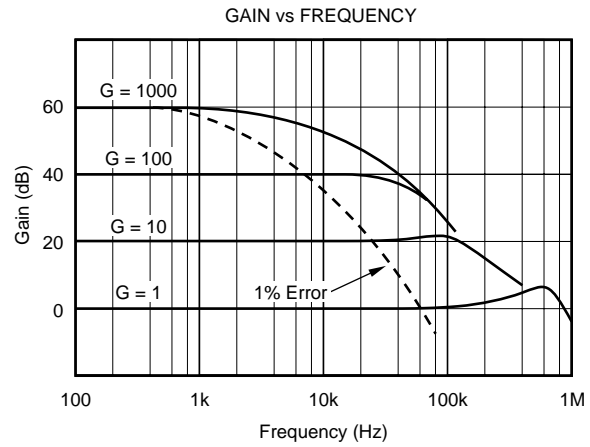
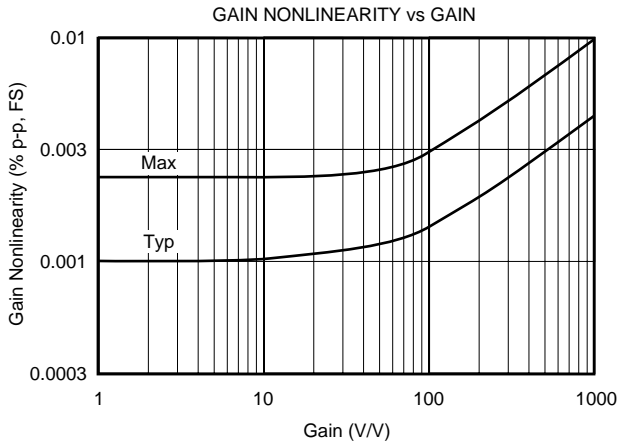
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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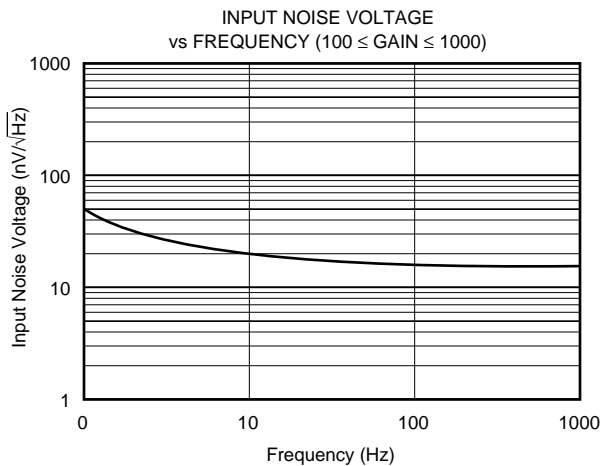
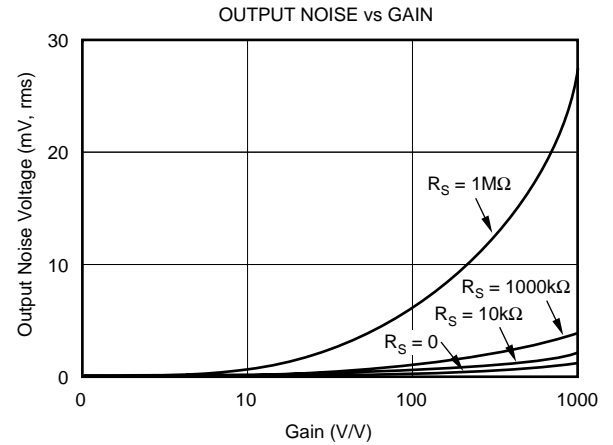
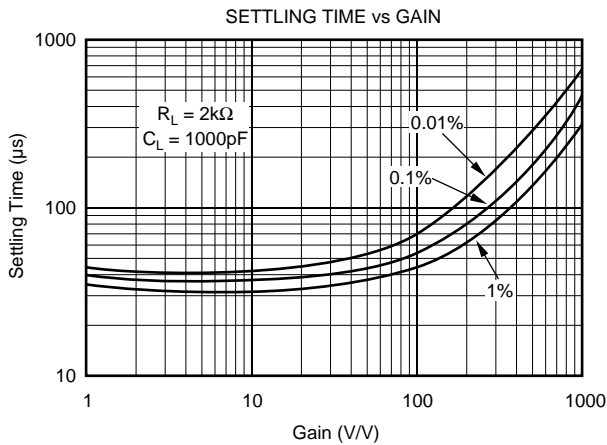
# TYPICAL PERFORMANCE CURVES

At +25°C,  $V_{CC} = \pm 15V$  unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At +25°C,  $V_{CC} = \pm 15V$  unless otherwise noted.



## APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA101. (Pin numbers shown are for the TO-100 metal package.) Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output Common terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance greater than  $0.1\Omega$  in series with the Common pin will cause common-mode rejection to fall below 106dB.

### SETTING THE GAIN

Gain of the INA101 is set by connecting a single external resistor,  $R_G$ :

$$G = 1 + \frac{40k\Omega}{R_G} \quad (1)$$

The  $40k\Omega$  term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA101.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. The gain sense connections on the DIP and SOL-16 packages (see Figure 2) reduce the gain error produced by wiring or socket resistance.

## OFFSET TRIMMING

The INA101 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows connection of an optional potentiometer connected to the Offset Adjust pins for trimming the input offset voltage. (Pin numbers shown are for the DIP package.) Use this adjustment to null the offset voltage in high gain ( $G \geq 100$ ) with both inputs connected to ground. Do not use this adjustment to null offset produced by the source or other system offset since this will increase the offset voltage drift by  $0.3\mu\text{V}/^\circ\text{C}$  per  $100\mu\text{V}$  of adjusted offset.

Offset of the output amplifier usually dominates when the INA101 is used in unity gain ( $G = 1$ ). The output offset

voltage can be adjusted with the optional trim circuit connected to the Common pin as shown in Figure 2. The voltage applied to Common terminal is summed with the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp connected as a buffer provides low impedance.

## THERMAL EFFECTS ON OFFSET VOLTAGE

To achieve lowest offset voltage and drift, prevent air currents from circulating near the INA101. Rapid changes in temperature will produce a thermocouple effect on the package leads that will degrade offset voltage and drift. A shield or cover that prevents air currents from flowing near the INA101 will assure best performance.

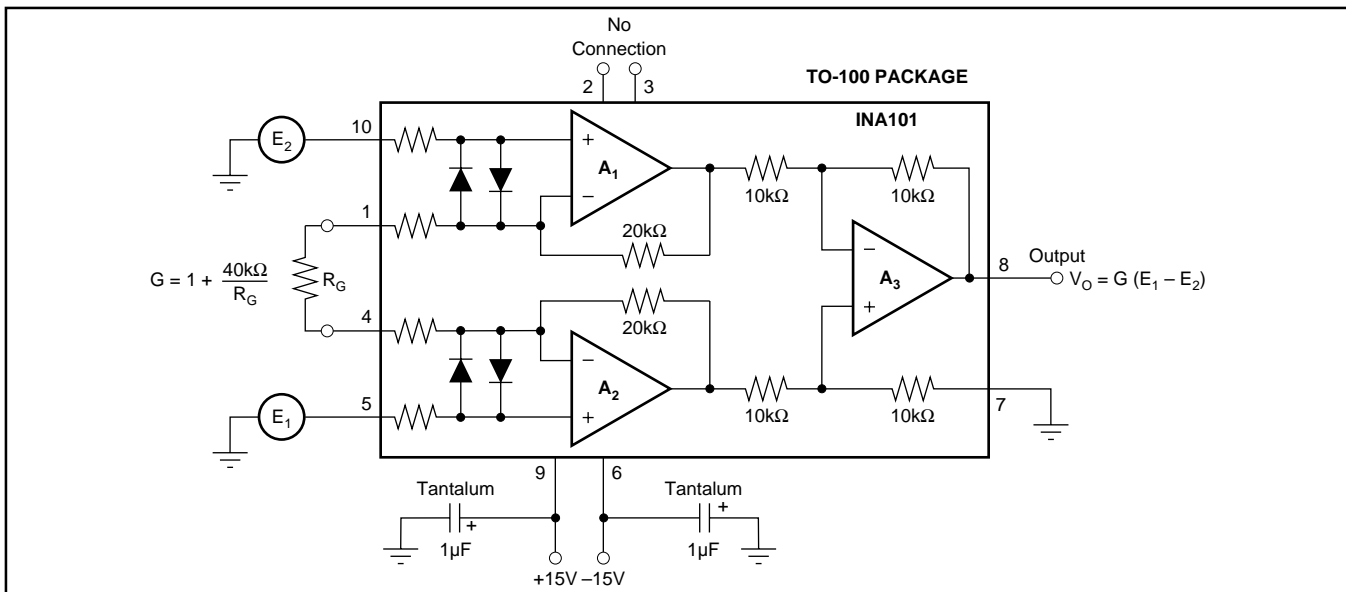


FIGURE 1. Basic Connections.

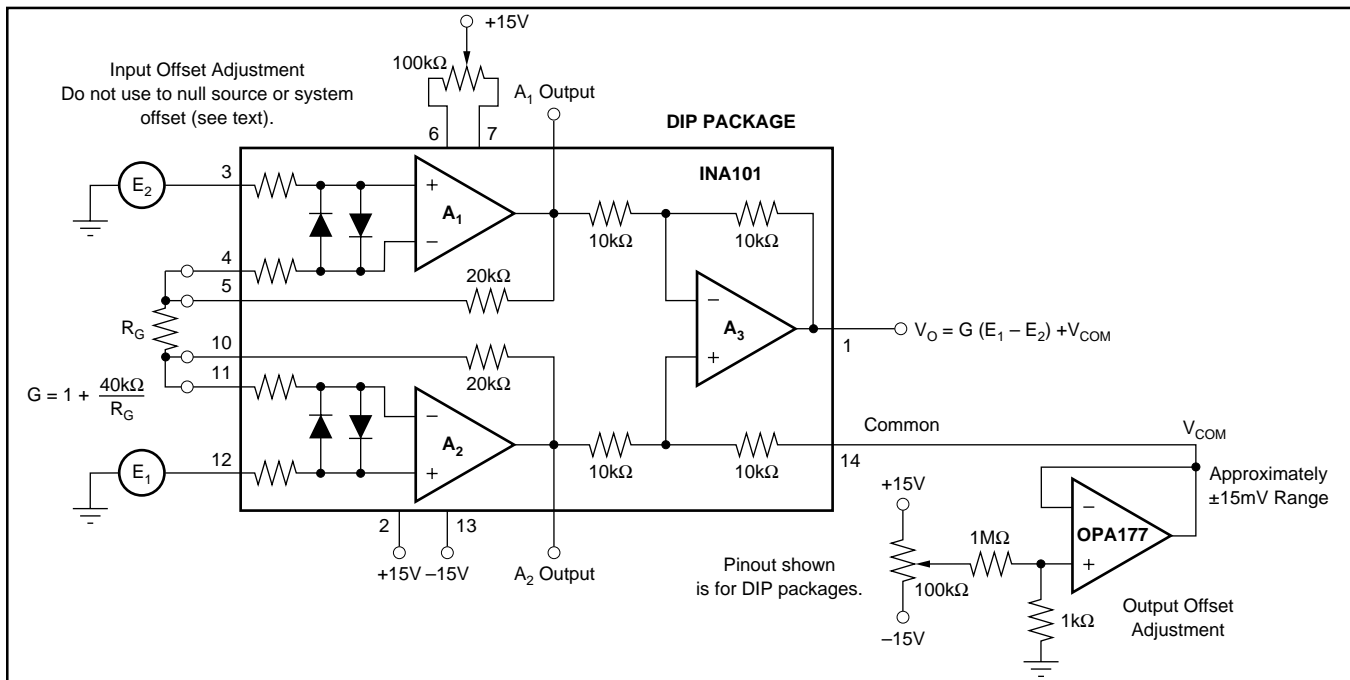


FIGURE 2. Optional Trimming of Input and Output Offset Voltage.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
INA101AG	NRND	CDIP SB	JD	14	27	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type
INA101AM	NRND	TO-100	LME	10	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
INA101AM2	OBSOLETE	TO-100	LME	10		TBD	Call TI	Call TI
INA101CM	NRND	TO-100	LME	10	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type
INA101CM1	OBSOLETE	TO-100	LME	10		TBD	Call TI	Call TI
INA101HP	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA101HPG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
INA101KU	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA101KU/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA101KU/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA101KUE4	ACTIVE	SOIC	DW	16	48	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA101SG1	OBSOLETE	TO-100	LME	10		TBD	Call TI	Call TI
INA101SM	NRND	TO-100	LME	10	20	Green (RoHS & no Sb/Br)	AU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

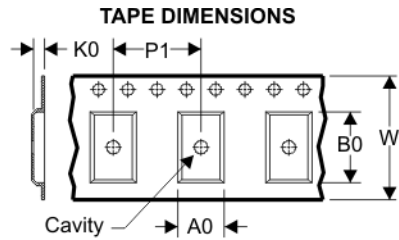
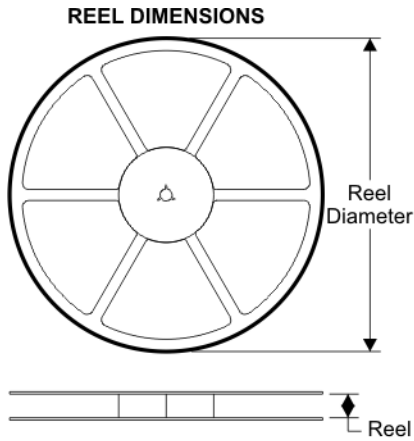
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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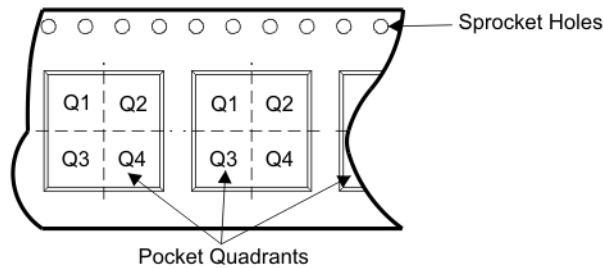
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**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA101KU/1K	DW	16	SITE 41	330	16	10.85	10.8	2.7	12	16	Q1

**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
INA101KU/1K	DW	16	SITE 41	346.0	346.0	33.0

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