ICM-20601

World's First Wide-Range 6-Axis MotionTracking Device for High Speed Applications

GENERAL DESCRIPTION

Many of today's wearable and sports solutions, which analyze the user's high speed motion, require higher full scale range (FSR) than currently available, to better ensure that critical data is not lost during high speed rotation. The ICM-20601 SoC offers the smallest size, lowest profile and lowest power in conjunction with industry leading high FSR.

With an extended FSR range of ±4000 dps for gyroscope and ±32*g* for accelerometer, the ICM-20601 enables precise motion tracking of high speed sports-related activity providing continuous sensor data throughout the motion, providing more accurate analysis.

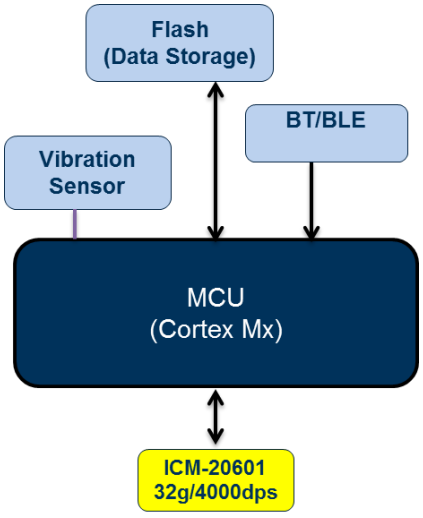
The ICM-20601 is the world's first wide-range 6-axis MotionTracking device for sports and other high speed applications. It is available in a 3 mm x 3 mm x 0.75 mm 16-pin LGA package.

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-20601†	−40°C to +85°C	16-Pin LGA

†Denotes RoHS and Green-Compliant Package

BLOCK DIAGRAM



Motion Analysis Pod Architecture

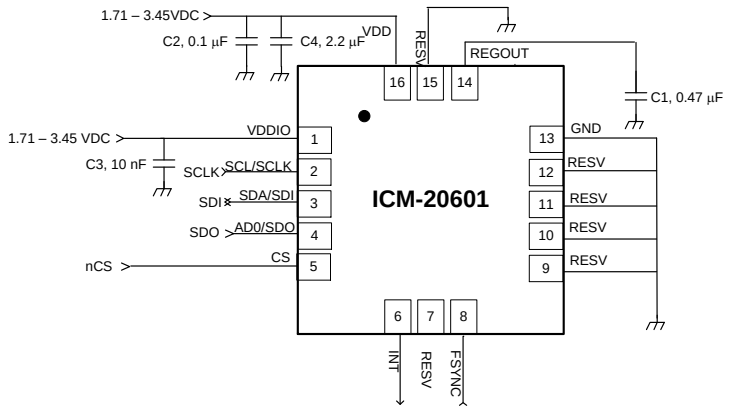
APPLICATIONS

- Sports
- Wearable Sensors

FEATURES

- 3-Axis Gyroscope with Programmable FSR of ±500dps, ±100dps, ±2000dps and ±4000dps
- 3-Axis Accelerometer with Programmable FSR of ±4*g*, ±8*g*, ±16*g*, and ±32*g*
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- 512 byte FIFO buffer enables the applications processor to read the data in bursts
- On-Chip 16-bit ADCs and Programmable Filters
- Host interface: 8 MHz SPI or 400k Hz Fast Mode I^2C
- Digital-output temperature sensor
- VDD operating range of 1.71 to 3.45V
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

TYPICAL OPERATING CIRCUIT



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1 GENERAL DESCRIPTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-20601™ MotionTracking device. The device is housed in a small 3 mm x 3 mm x 0.75 mm 16-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-20601 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 3 mm x 3 mm x 0.75 mm (16-pin LGA) package. It also features a 512 byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-20601, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range up to ±4000 dps. The accelerometer has a user-programmable accelerometer full-scale range up to ±32*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71V to 3.45V, and a separate digital IO supply, VDDIO from 1.71V to 3.45V. Communication with all registers of the device is performed using either I^2C at 400 kHz or SPI at 8 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3 mm x 3 mm x 0.75 mm (16-pin LGA), to provide a very small yet high---performance, low-cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- High Impact Sports
- Wearable Sensors

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-20601 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±500 dps, ±1000 dps, ±2000 dps, and ±4000 dps, and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-20601 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of ±4*g*, ±8*g*, ±16*g*, and ±32*g*, and integrated 16-bit ADCs
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The ICM-20601 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 3 mm x 3 mm x 0.75 mm (16-pin LGA)
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- 512 byte FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 10,000*g* shock tolerant
- 400 kHz Fast Mode I^2C for communicating with all registers
- 8 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL=0		±500		dps	3
	FS_SEL=1		±1000		dps	3
	FS_SEL=2		±2000		dps	3
	FS_SEL=3		±4000		dps	3
Gyroscope ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL=0		65.5		LSB/(dps)	3
	FS_SEL=1		32.8		LSB/(dps)	3
	FS_SEL=2		16.4		LSB/(dps)	3
	FS_SEL=3		8.2		LSB/(dps)	3
Sensitivity Scale Factor Tolerance	25°C		±2		%	2
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±3		%	1
Nonlinearity	Best fit straight line; 25°C		±0.3		%	1
Cross-Axis Sensitivity			±2		%	1
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±5		dps	2
ZRO Variation Over Temperature	-40°C to +85°C		±0.1		dps/°C	1
GYROSCOPE NOISE PERFORMANCE (FS_SEL=0)						
Noise Spectral Density			0.013		dps/√Hz	1
Gyroscope Mechanical Frequencies		25	27	29	KHz	2
Low Pass Filter Response	Programmable Range	5		250	Hz	3
Gyroscope Start-Up Time	From Sleep mode		35		ms	1
Output Data Rate	Standard (duty-cycled) mode	3.91		500	Hz	1
	Low-Noise (active) mode	4		8000	Hz	1

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	AFS_SEL=0			±4		*g*	3
	AFS_SEL=1			±8		*g*	3
	AFS_SEL=2			±16		*g*	3
	AFS_SEL=3			±32		*g*	3
ADC Word Length	Output in two's complement format			16		bits	3
Sensitivity Scale Factor	AFS_SEL=0			8,192		LSB/*g*	3
	AFS_SEL=1			4,096		LSB/*g*	3
	AFS_SEL=2			2,048		LSB/*g*	3
	AFS_SEL=3			1,024		LSB/*g*	3
Initial Tolerance	Component-level			±2		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C AFS_SEL=0 Component-level			±0.016		%/°C	1
Nonlinearity	Best Fit Straight Line			±0.5		%	1
Cross-Axis Sensitivity				±2		%	1
ZERO-G OUTPUT							
Initial Tolerance	Component-level, all axes			±60		m*g*	1
Zero-G Level Change vs. Temperature	-40°C to +85°C, Board-level	X and Y axes		±0.5		m*g*/°C	1
		Z axis		±1		m*g*/°C	1
NOISE PERFORMANCE							
Noise Spectral Density				390		µ*g*/√Hz	1
Low Pass Filter Response	Programmable Range		5		218	Hz	3
Intelligence Function Increment				4		mg/LSB	3
Accelerometer Startup Time	From Sleep mode			20		ms	1
	From Cold Start, 1 ms V_{DD} ramp			30		ms	1
Output Data Rate	Standard (duty-cycled) mode		0.24		500	Hz	1
	Low-Noise (active) mode		4		4000	Hz	

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.

3.3 ELECTRICAL SPECIFICATIONS

3.3.3 D.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	1
VDDIO		1.71	1.8	3.45	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-axis Gyroscope + Accelerometer		3		mA	1
	3-axis Gyroscope		2.6		mA	1
	3-axis Accelerometer, 4kHz ODR		390		µA	1
Accelerometer Standard Mode	100 Hz ODR, 1x averaging		57		µA	1
Gyroscope Standard Mode	100 Hz ODR, 1x averaging		1.6		mA	1
Gyroscope Standard Mode	10 Hz ODR, 1x averaging		1.3		mA	1
6-Axis Standard Mode (Gyroscope Standard Mode; Accelerometer Low-Noise Mode)	100 Hz ODR, 1x averaging		1.9		mA	1
Full-Chip Sleep Mode			6		µA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.3.4 Standard (Duty-Cycle) Mode Noise and Power Performance

The following tables contain Gyroscope and Accelerometer noise and current consumption values for standard (duty-cycle) mode, for various ODRs and averaging filter settings. Please refer to the ICM-20601 Register Map for further information about the registers referenced in the tables below.

FCHOICE_B		0	0	0	0	0	0	0	0
G_AVGCFG		0	1	2	3	4	5	6	7
Averages		1x	2x	4x	8x	16x	32x	64x	128x
Ton (ms)		1.73	2.23	3.23	5.23	9.23	17.23	33.23	65.23
Noise BW (Hz)		650.8	407.1	224.2	117.4	60.2	30.6	15.6	8.0
Noise (dps) TYP based on 0.013 dps/√Hz		0.33	0.26	0.19	0.14	0.10	0.07	0.05	0.04
SMPLRT_DIV	ODR (Hz)	Current Consumption (mA) TYP							
255	3.9	1.3	1.3	1.3	1.3	1.4	1.4	1.5	1.8
99	10.0	1.3	1.3	1.4	1.4	1.5	1.6	1.9	2.5
64	15.4	1.4	1.4	1.4	1.5	1.6	1.8	2.2	N/A
32	30.3	1.4	1.4	1.5	1.6	1.8	2.2	N/A	
19	50.0	1.5	1.5	1.6	1.8	2.1	2.8		
9	100.0	1.6	1.7	1.9	2.2	3.0	N/A		
7	125.0	1.7	1.8	2.0	2.5	N/A			
4	200.0	1.9	2.1	2.5	N/A				
3	250.0	2.1	2.3	2.7					
2	333.3	2.3	2.6	N/A					
1	500.0	2.9	N/A						

Table 4. Gyroscope Noise and Current Consumption

ACCEL_FCHOICE_B		1	0	0	0	0
A_DLPF_CFG		x	7	7	7	7
DEC2_CFG		x	0	1	2	3
Averages		1x	4x	8x	16x	32x
Ton (ms)		1.084	1.84	2.84	4.84	8.84
Noise BW (Hz)		1100.0	441.6	235.4	121.3	61.5
Noise (mg) TYP based on 390 µg/√Hz		12.9	8.2	6.0	4.3	3.1
SMPLRT_DIV	ODR (Hz)	Current Consumption (µA) TYP				
255	3.9	8.4	9.4	10.8	13.6	19.2
127	7.8	9.8	11.9	14.7	20.3	31.4
63	15.6	12.8	17.0	22.5	33.7	55.9
31	31.3	18.7	27.1	38.2	60.4	104.9
15	62.5	30.4	47.2	69.4	113.9	202.8
7	125.0	57.4	87.5	132.0	220.9	N/A
3	250.0	100.9	168.1	257.0	N/A	
1	500.0	194.9	329.3	N/A		

Table 5. Accelerometer Noise and Current Consumption

3.3.5 A.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Room Temperature Offset	25°C		0		°C	1
Sensitivity	Untrimmed		326.8		LSB/°C	1
POWER-ON RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01		100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
	From sleep			5	ms	1
I²C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, Low-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I²C I/O (SCL, SDA)						
V_{IL}, Low-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, High-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, Low-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, Low-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B=1,2,3 SMPLRT_DIV=0		32		kHz	2
	FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	2

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
	FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL=0, 6 or gyro inactive; 25°C	-5		+5	%	1
	CLK_SEL=1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6 or gyro inactive	-10		+10	%	1
	CLK_SEL=1,2,3,4,5 and gyro active	-1		+1	%	1

Table 6. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.

3.3.6 Other Electrical Specifications

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low-Speed Characterization		100 ±10%		kHz	1
	High-Speed Characterization		1	8	MHz	1, 2
SPI Modes			Modes 0 and 3			
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 7. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 8 MHz operation.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 8. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

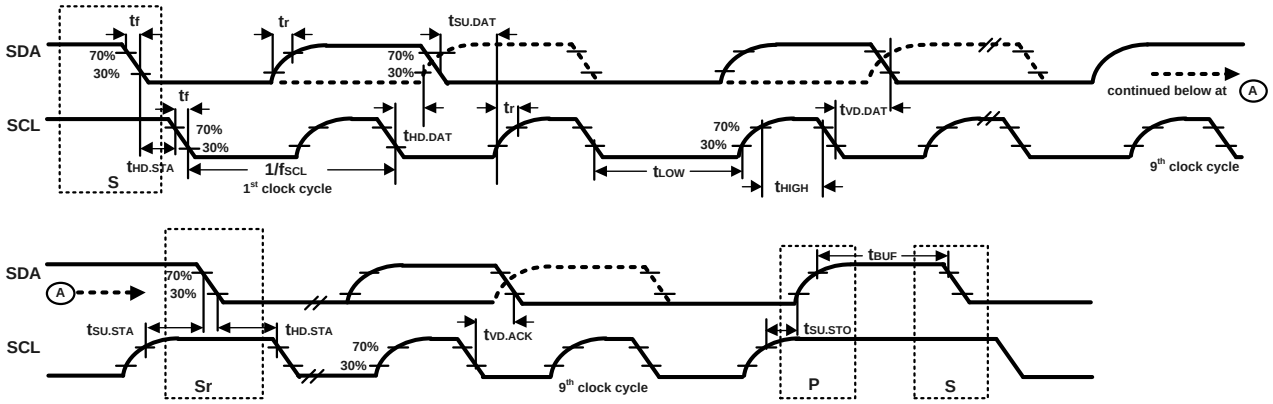


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				8	MHz	1
t_{LOW}, SCLK Low Period		56			ns	1
t_{HIGH}, SCLK High Period		56			ns	1
$t_{SU.CS}$, CS Setup Time		2			ns	1
$t_{HD.CS}$, CS Hold Time		63			ns	1
$t_{SU.SDI}$, SDI Setup Time		3			ns	1
$t_{HD.SDI}$, SDI Hold Time		7			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			40	ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1
t_{Fall}, SCLK Fall Time				6.5	ns	2
t_{Rise}, SCLK Rise Time				6.5	ns	2
$t_{DIS.SDO}$, SDO Output Disable Time				20	ns	1

Table 9. SPI Timing Characteristics (8 MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on calculation from other parameter values

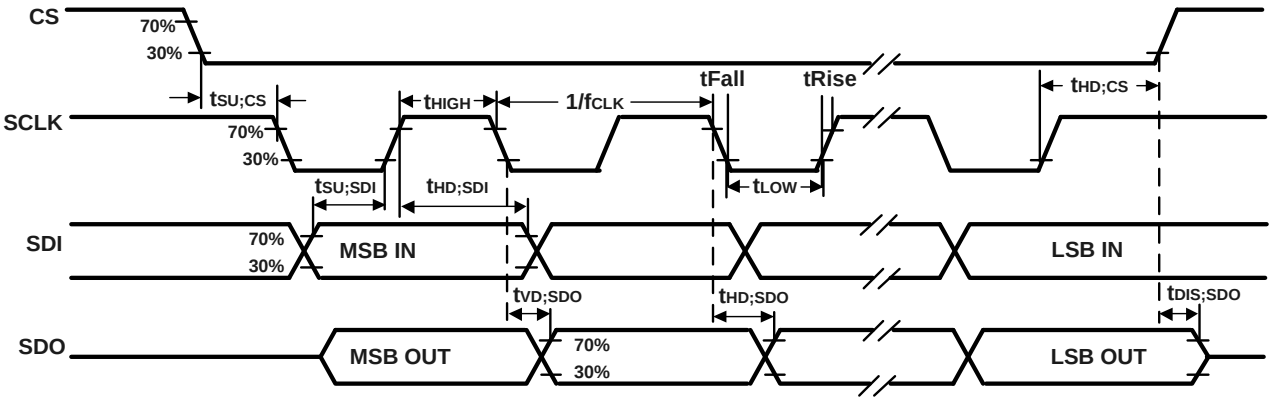


Figure 2. SPI Bus Timing Diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC, SCL, SDA)	-0.5V to VDD + 0.5V
Acceleration (Any Axis, unpowered)	10,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 10. Absolute Maximum Ratings

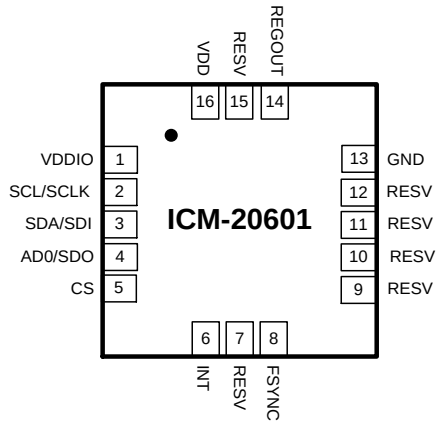
4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

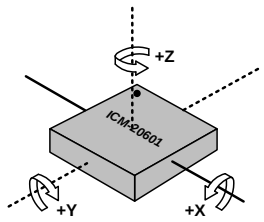
PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage
2	SCL/SCLK	I²C serial clock (SCL); SPI serial clock (SCLK)
3	SDA/SDI	I²C serial data (SDA); SPI serial data input (SDI)
4	AD0/SDO	I²C slave address LSB (AD0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I²C mode)
6	INT	Interrupt digital output (totem pole or open-drain)
7	RESV	Reserved. Do not connect.
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused.
9	RESV	Reserved. Connect to GND.
10	RESV	Reserved. Connect to GND.
11	RESV	Reserved. Connect to GND.
12	RESV	Reserved. Connect to GND.
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND.
16	VDD	Power Supply

Table 11. Signal Descriptions

Note: VDD, VDDIO, SCL/SCLK and CS pins must be correctly managed at power-up to guarantee proper device start-up. Please refer to sections 4.18 and 4.19 for detailed power-up instructions.



LGA Package (Top View)
16-pin, 3mm x 3mm x 0.75mm
Typical Footprint and thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for ICM-20601 3 mm x 3 mm x 0.75 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

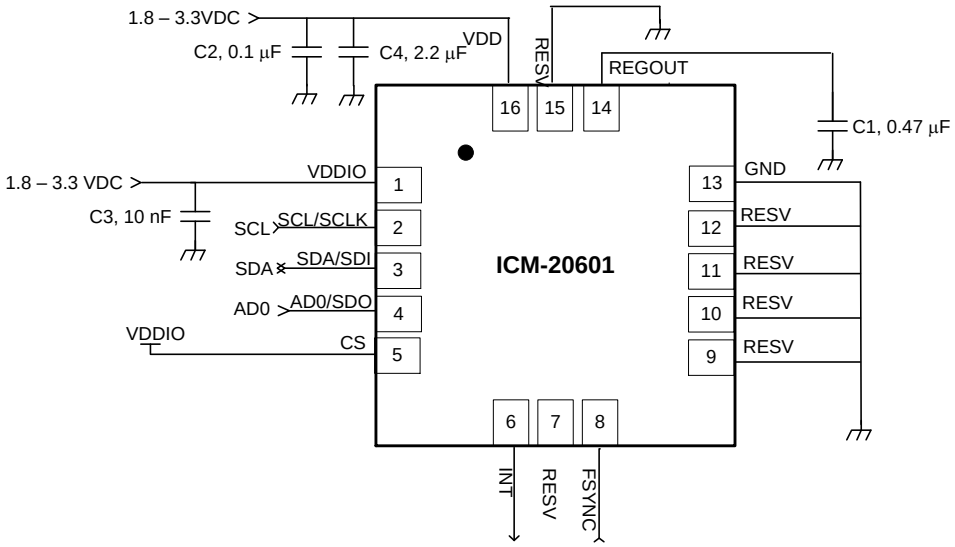


Figure 4. ICM-20601 I²C Operation Application Schematic

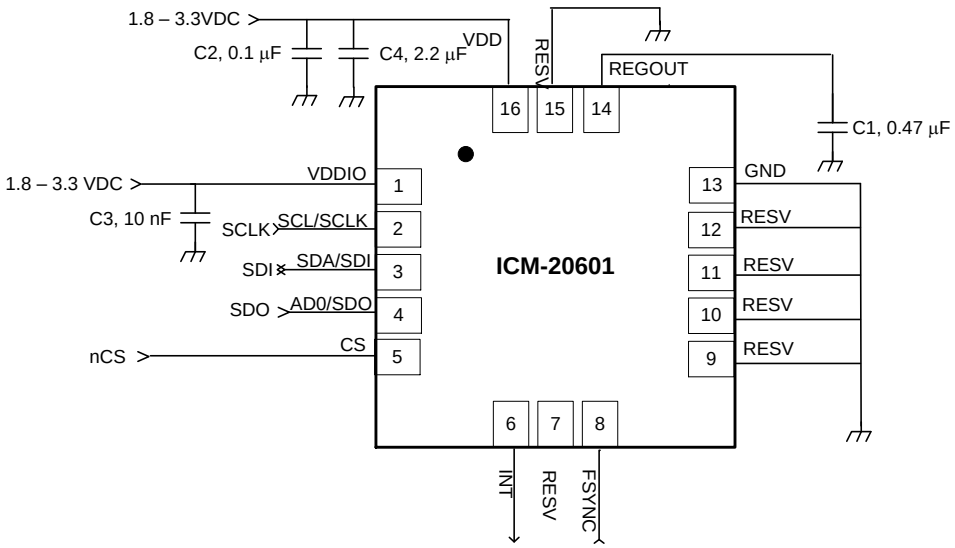


Figure 5. ICM-20601 SPI Operation Application Schematic

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
REGOUT Capacitor	C1	Ceramic, X7R, 0.47 µF ±10%, 2V	1
VDD Bypass Capacitors	C2	Ceramic, X7R, 0.1 µF ±10%, 4V	1
	C4	Ceramic, X7R, 2.2 µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10 nF ±10%, 4V	1

Table 11. Bill of Materials

4.4 BLOCK DIAGRAM

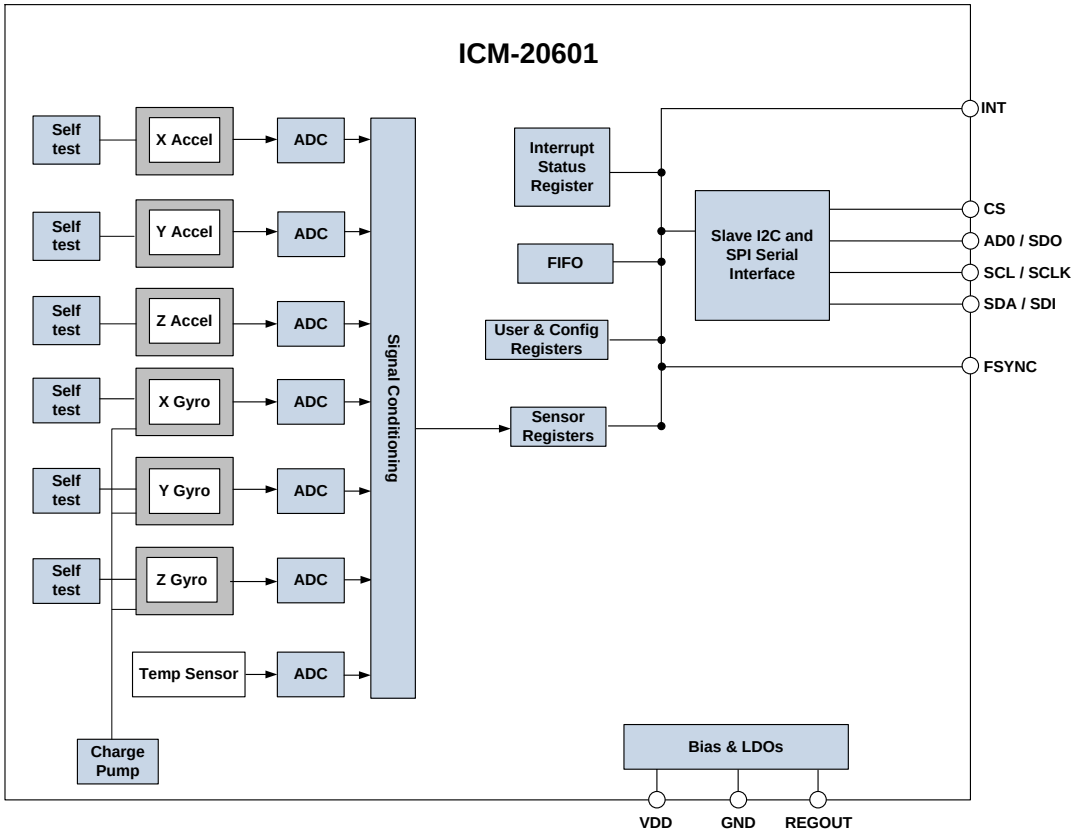


Figure 6. ICM-20601 Block Diagram

4.5 OVERVIEW

The ICM-20601 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20601 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±500, ±1000, ±2000, or ±4000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20601's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20601's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±4*g*, ±8*g*, ±16*g*, or ±32*g*.

4.8 I^2C AND SPI SERIAL COMMUNICATIONS INTERFACES

The ICM-20601 communicates to a system processor using either a SPI or an I^2C serial interface. The ICM-20601 always acts as a slave when communicating to the system processor. The LSB of the I^2C slave address is set by pin 4 (AD0).

4.8.1 ICM-20601 Solution Using I2C Interface

In Figure 7, the system processor is an I^2C master to the ICM-20601.

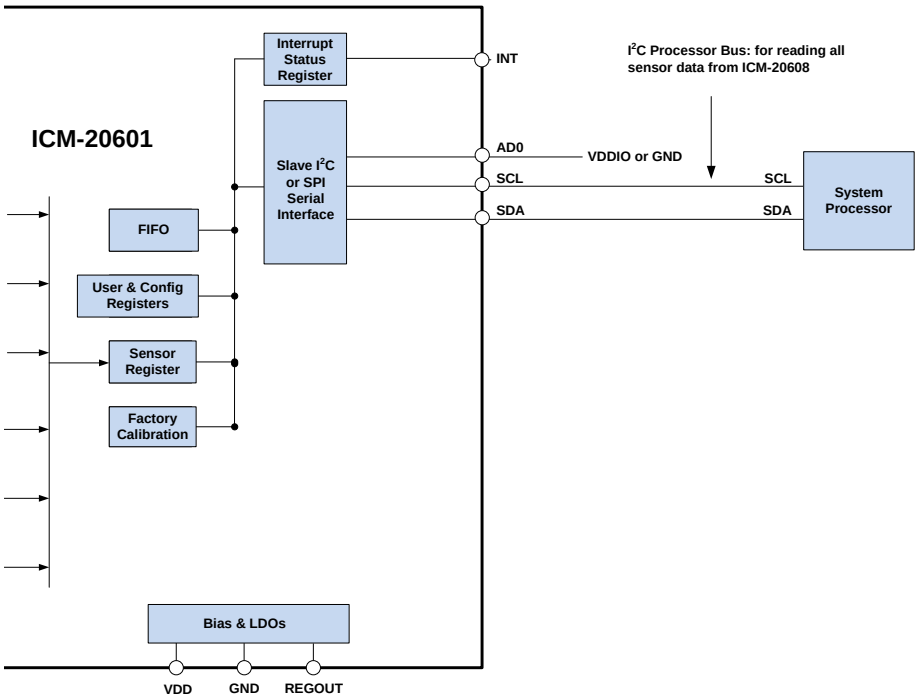


Figure 7. ICM-20601 Solution Using I²C Interface

4.8.2 ICM-20601 Solution Using SPI Interface

In Figure 8, the system processor is an SPI master to the ICM-20601. Pins 2, 3, 4, and 5 are used to support the SCLK, SDI, SDO, and CS signals for SPI communications.

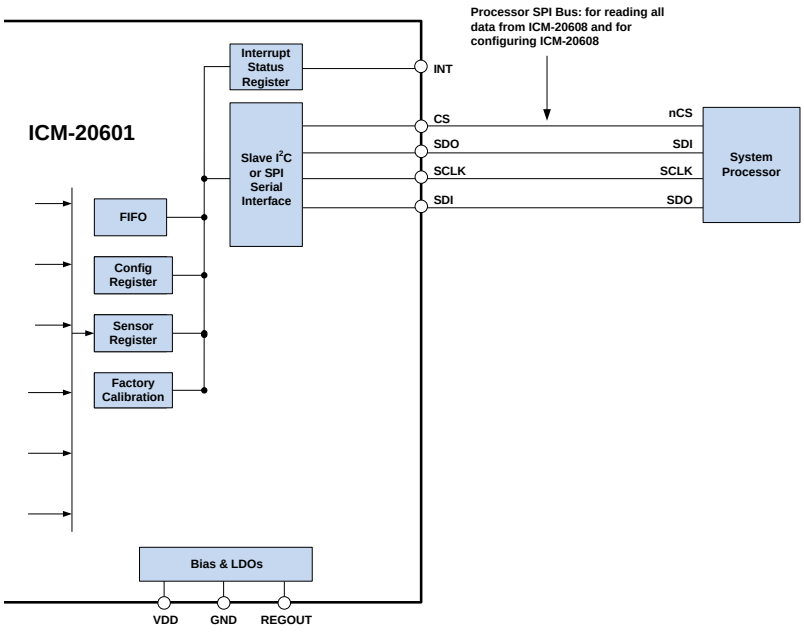


Figure 8. ICM-20601 Solution Using SPI Interface

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

SELF-TEST RESPONSE = SENSOR OUTPUT WITH SELF-TEST ENABLED – SENSOR OUTPUT WITH SELF-TEST DISABLED

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test. It is recommended to use InvenSense MotionApps software for executing self-test.

4.10 CLOCKING

The ICM-20601 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator

b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). Use of option b) is recommended.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 FIFO

The ICM-20601 contains a 512 byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

The ICM-20601 allows FIFO read in standard (duty cycle) accelerometer mode.

4.13 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.14 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-20601 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.15 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20601. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.16 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.17 POWER MODES

The following table lists the user-accessible power modes for ICM-20601.

MODE	NAME	GYRO	ACCEL
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Standard Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Standard Mode	Duty-Cycled	Off
6	Gyroscope Low-Noise Mode	On	Off
7	6-Axis Low-Noise Mode	On	On
8	6-Axis Standard Mode	Duty-Cycled	On

Table 12. Power Modes for ICM-20601

4.18 POWER-UP SEQUENCE

When applying VDD, the power voltage ramp is detected and a power-on-reset sequence is triggered inside the component. During this phase the device starts operating and internal logic levels are defined. For proper component initialization the power-up should be performed with both CS and SCL/SCLK low, ensuring that CS and SCL pins are not in an undetermined state during the VDD ramp. If starting in I^2C mode (CS at logic high), power-up should be performed with SCL/SCLK low. Power-up with SCL/SCLK high is not a supported case and must be avoided.

It is worth noting that if the I/O pins (e.g. CS, SCL/SCLK) are between V_{IL} and V_{IH} when the power-on-reset sequence is triggered, their value is undetermined and the internal logic levels may not be properly defined. It should also be noted that V_{IL} and V_{IH} are related to VDDIO and their value changes at power-up according to the applied VDDIO voltage ramp.

Power-up sequences that do not respect the conditions above may not lead to proper digital interface initialization. In this case a preliminary soft reset operation (PWR_MGMT_1 register set 0x81) must be performed to reset the digital interface, as soon as both VDD and VDDIO are stable at their final voltage. Since the digital interface may not be properly initialized, the device may not provide the acknowledge signal if the I^2C protocol is used.

4.19 SENSOR INITIALIZATION AND CLOCK SOURCE SELECTION

When power-up sequence is completed (as per section 4.18), a soft reset is required to initialize the sensor and let the device select the best clock source. The soft reset must be performed by setting the register PWR_MGMT_1 (address 0x6B) to 0x81, prior to registers initialization.

Soft reset must be performed as first operation after the power-up sequence to ensure the proper component registers setting. Correct WHOAMI value is ensured only after the soft reset has been completed.

5 PROGRAMMABLE INTERRUPTS

The ICM-20601 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

INTERRUPT NAME	MODULE
Motion Detection	Motion
FIFO Overflow	FIFO
Data Ready	Sensor Registers

Table 13. Table of Interrupt Sources

5.1 WAKE-ON-MOTION INTERRUPT

The ICM-20601 provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

Step 1: Ensure that Accelerometer is running

- In PWR_MGMT_1 register (0x6B) set CYCLE = 0, SLEEP = 0, and GYRO_STANDBY = 0
- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1

Step 2: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 0 and A_DLPF_CFG[2:0] = 1 (b001)

Step 3: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_INT_EN = 111 to enable motion interrupt

Step 4: Set Motion Threshold

- Set the motion threshold in ACCEL_WOM_THR register (0x1F)

Step 5: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = ACCEL_INTEL_MODE = 1; Ensure that bit 0 is set to 0.

Step 6: Set Frequency of Wake-Up

- In Standard Mode Configuration register (0x1E) set LPOSC_CLKSEL[3:0] for a sample rate as indicated in the register map

Step 7: Enable Cycle Mode (Accelerometer Standard Mode)

- In PWR_MGMT_1 register (0x6B) set CYCLE = 1

6 DIGITAL INTERFACE

6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-20601 can be accessed using either I²C at 400 kHz or SPI at 8 MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VDDIO	Digital I/O supply voltage.
4	AD0 / SDO	I²C Slave Address LSB (AD0); SPI serial data output (SDO)
2	SCL / SCLK	I²C serial clock (SCL); SPI serial clock (SCLK)
3	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

Table 14. Serial Interface

Note: To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in section 3.3.3.

6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20601 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20601 is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AD0. This allows two ICM-20601s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

6.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

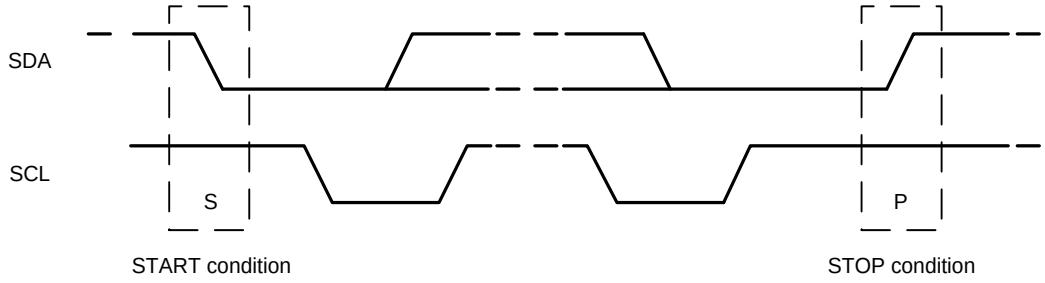


Figure 9. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

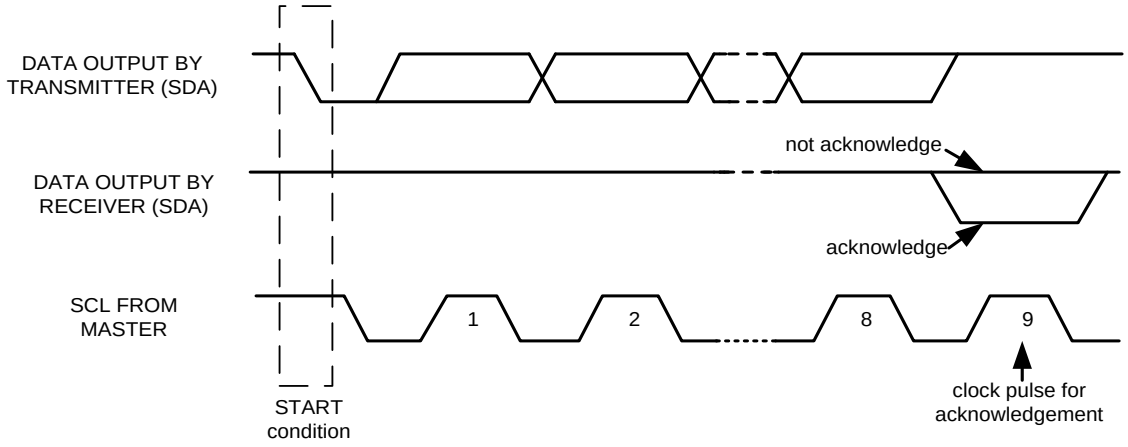


Figure 10. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

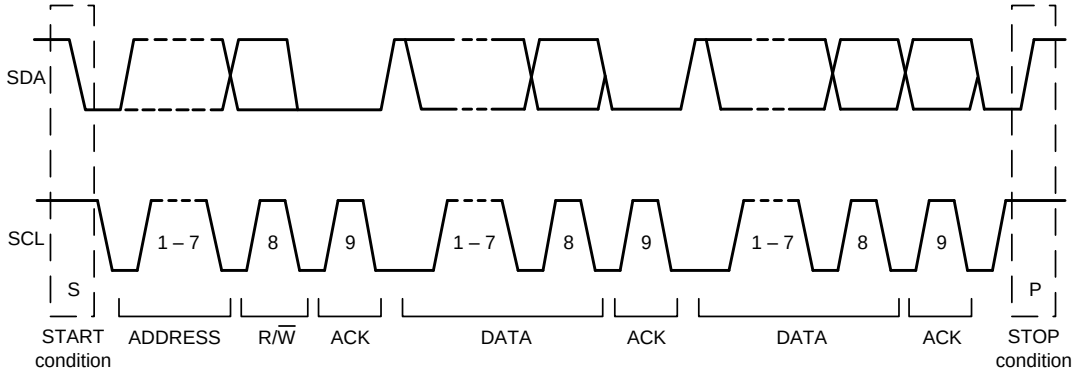


Figure 11. Complete I²C Data Transfer

To write the internal ICM-20601 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-20601 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-20601 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-20601 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-20601 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-20601, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-20601 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I²C TERMS

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-20601 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 15. I²C Terms

6.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICM-20601 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 8MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

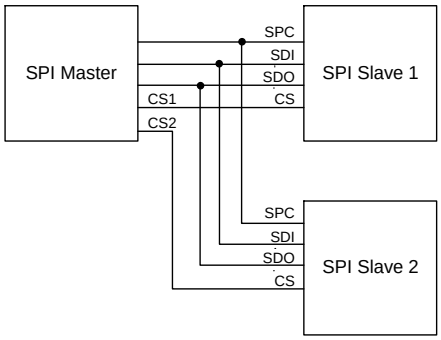


Figure 12. Typical SPI Master/Slave Configuration

7 REGISTER MAP

The following table lists the register map for the ICM-20601.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Accessible (writable) in Sleep Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	SELF_TEST_X_GYRO	R/W	N	XG_ST_DATA[7:0]							
01	01	SELF_TEST_Y_GYRO	R/W	N	YG_ST_DATA[7:0]							
02	02	SELF_TEST_Z_GYRO	R/W	N	ZG_ST_DATA[7:0]							
0D	13	SELF_TEST_X_ACCEL	R/W	N	XA_ST_DATA[7:0]							
0E	14	SELF_TEST_Y_ACCEL	R/W	N	YA_ST_DATA[7:0]							
0F	15	SELF_TEST_Z_ACCEL	R/W	N	ZA_ST_DATA[7:0]							
13	19	XG_OFFS_USRH	R/W	N	X_OFFS_USR [15:8]							
14	20	XG_OFFS_USRL	R/W	N	X_OFFS_USR [7:0]							
15	21	YG_OFFS_USRH	R/W	N	Y_OFFS_USR [15:8]							
16	22	YG_OFFS_USRL	R/W	N	Y_OFFS_USR [7:0]							
17	23	ZG_OFFS_USRH	R/W	N	Z_OFFS_USR [15:8]							
18	24	ZG_OFFS_USRL	R/W	N	Z_OFFS_USR [7:0]							
19	25	SMPLRT_DIV	R/W	N	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	N	-	FIFO_ MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	R/W	N	XG_ST	YG_ST	ZG_ST	FS_SEL [1:0]		-	FCHOICE_B[1:0]	
1C	28	ACCEL_CONFIG	R/W	N	XA_ST	YA_ST	ZA_ST	ACCEL_FS_SEL[1:0]		-		
1D	29	ACCEL_CONFIG 2	R/W	N	-		DEC2_CFG		ACCEL_FCHOICE_B	A_DLPF_CFG		
1E	30	LP_MODE_CFG	R/W	N	GYRO_CYCLE	G_AVGCFG[2:0]			-	LPOSC_CLKSEL		
1F	31	ACCEL_WOM_THR	R/W	N	WOM_THR[7:0]							
23	35	FIFO_EN	R/W	N	TEMP _FIFO_EN	XG_FIFO_EN	YG_FIFO_EN	ZG_FIFO_EN	ACCEL_FIFO_ EN	-	-	-
36	54	FSYNC_INT	R/C	N	FSYNC_INT	-	-	-	-	-	-	-
37	55	INT_PIN_CFG	R/W	Y	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_INT_LEVEL	FSYNC _INT_MODE_ EN	-	-
38	56	INT_ENABLE	R/W	Y	WOM_INT_EN[7:5]			FIFO _OFLOW _EN	-	GDRIVE_INT_ EN	-	DATA_RDY_INT_EN
3A	58	INT_STATUS	R/C	N	WOM_INT[7:5]			FIFO _OFLOW _INT	-	GDRIVE_INT	-	DATA _RDY_INT
3B	59	ACCEL_XOUT_H	R	N	ACCEL_XOUT_H[15:8]							
3C	60	ACCEL_XOUT_L	R	N	ACCEL_XOUT_L[7:0]							
3D	61	ACCEL_YOUT_H	R	N	ACCEL_YOUT_H[15:8]							
3E	62	ACCEL_YOUT_L	R	N	ACCEL_YOUT_L[7:0]							
3F	63	ACCEL_ZOUT_H	R	N	ACCEL_ZOUT_H[15:8]							
40	64	ACCEL_ZOUT_L	R	N	ACCEL_ZOUT_L[7:0]							
41	65	TEMP_OUT_H	R	N	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	R	N	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	R	N	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	R	N	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	R	N	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	R	N	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT_H	R	N	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT_L	R	N	GYRO_ZOUT[7:0]							
68	104	SIGNAL_PATH_RESET	R/W	N	-	-	-	-	-	-	ACCEL _RST	TEMP _RST
69	105	ACCEL_INTEL_CTRL	R/W	N	ACCEL_INTEL_EN	ACCEL_INTEL _MODE	-					
6A	106	USER_CTRL	R/W	N	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RST	-	SIG_COND _RST
6B	107	PWR_MGMT_1	R/W	Y	DEVICE_RESET	SLEEP	ACCEL_CYCLE	GYRO_ STANDBY	TEMP_DIS	CLKSEL[2:0]		

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Accessible (writable) in Sleep Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6C	108	PWR_MGMT_2	R/W	Y	FIFO_LP_EN	-	STBY_XA	STBY_YA	STBY_ZA	STBY_XG	STBY_YG	STBY_ZG
72	114	FIFO_COUNTH	R	N	-			FIFO_COUNT[12:8]				
73	115	FIFO_COUNTL	R	N	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	R/W	N	FIFO_DATA[7:0]							
75	117	WHO_AM_I	R	N	WHOAMI[7:0]							
77	119	XA_OFFSET_H	R/W	N	XA_OFFS [14:7]							
78	120	XA_OFFSET_L	R/W	N	XA_OFFS [6:0]							-
7A	122	YA_OFFSET_H	R/W	N	YA_OFFS [14:7]							
7B	123	YA_OFFSET_L	R/W	N	YA_OFFS [6:0]							-
7D	125	ZA_OFFSET_H	R/W	N	ZA_OFFS [14:7]							
7E	126	ZA_OFFSET_L	R/W	N	ZA_OFFS [6:0]							-

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the ACCEL_XOUT_H register (Register 59) contains the 8 most significant bits, *ACCEL_XOUT*[15:8], of the 16-bit X-Axis accelerometer measurement, *ACCEL_XOUT*.

The reset value is 0x00 for all registers other than the registers below, also the self-test registers contain pre-programmed values and will not be 0x00 after reset.

- Register 107 (0x40) Power Management 1
- Register 117 (0xAC) WHO_AM_I

8 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the ICM-20601.

Note: The device will come up in sleep mode upon power-up.

8.1 REGISTERS 0 TO 2 – GYROSCOPE SELF-TEST REGISTERS

Register Name: SELF_TEST_X_GYRO, SELF_TEST_Y_GYRO, SELF_TEST_Z_GYRO

Type: READ/WRITE

Register Address: 00, 01, 02 (Decimal); 00, 01, 02 (Hex)

REGISTER	BIT	NAME	FUNCTION
SELF_TEST_X_GYRO	[7:0]	XG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_GYRO	[7:0]	YG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_GYRO	[7:0]	ZG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (1310/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round(\frac{log(ST\_FAC/(1310/2^{FS}))}{log(1.01)}) + 1$$

8.2 REGISTERS 13 TO 15 – ACCELEROMETER SELF-TEST REGISTERS

Register Name: SELF_TEST_X_ACCEL, SELF_TEST_Y_ACCEL, SELF_TEST_Z_ACCEL

Type: READ/WRITE

Register Address: 13, 14, 15 (Decimal); 0D, 0E, 0F (Hex)

REGISTER	BITS	NAME	FUNCTION
SELF_TEST_X_ACCEL	[7:0]	XA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Y_ACCEL	[7:0]	YA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.
SELF_TEST_Z_ACCEL	[7:0]	ZA_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

The equation to convert self-test codes in OTP to factory self-test measurement is:

$$ST\_OTP = (1310/2^{FS}) * 1.01^{(ST\_code-1)} \text{ (lsb)}$$

where ST_OTP is the value that is stored in OTP of the device, FS is the Full Scale value, and ST_code is based on the Self-Test value (ST_ FAC) determined in InvenSense's factory final test and calculated based on the following equation:

$$ST\_code = round(\frac{log(ST\_FAC/(1310/2^{FS}))}{log(1.01)}) + 1$$

8.3 REGISTERS 19 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: XG_OFFS_USRH

Register Type: READ/WRITE

Register Address: 19 (Decimal); 13 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. Gyroscope offset cancellation step size: 0.0305dps/LSB

8.4 REGISTERS 20 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: XG_OFFS_USRL

Register Type: READ/WRITE

Register Address: 20 (Decimal); 14 (Hex)

BIT	NAME	FUNCTION
[7:0]	X_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of X gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. Gyroscope offset cancellation step size: 0.0305dps/LSB

8.5 REGISTERS 21 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: YG_OFFS_USRH

Register Type: READ/WRITE

Register Address: 21 (Decimal); 15 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. Gyroscope offset cancellation step size: 0.0305dps/LSB

8.6 REGISTERS 22 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: YG_OFFS_USRL

Register Type: READ/WRITE

Register Address: 22 (Decimal); 16 (Hex)

BIT	NAME	FUNCTION
[7:0]	Y_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Y gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. Gyroscope offset cancellation step size: 0.0305dps/LSB

8.7 REGISTERS 23 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: ZG_OFFS_USRH

Register Type: READ/WRITE

Register Address: 23 (Decimal); 17 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[15:8]	Bits 15 to 8 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. Gyroscope offset cancellation step size: 0.0305dps/LSB

8.8 REGISTER 24 – GYRO OFFSET ADJUSTMENT REGISTER

Register Name: ZG_OFFS_USRL

Register Type: READ/WRITE

Register Address: 24 (Decimal); 18 (Hex)

BIT	NAME	FUNCTION
[7:0]	Z_OFFS_USR[7:0]	Bits 7 to 0 of the 16-bit offset of Z gyroscope (2's complement). This register is used to remove DC bias from the sensor output. The value in this register is added to the gyroscope sensor value before going into the sensor register. Gyroscope offset cancellation step size: 0.0305dps/LSB

8.9 REGISTER 25 – SAMPLE RATE DIVIDER

Register Name: SMPLRT_DIV

Register Type: READ/WRITE

Register Address: 25 (Decimal); 19 (Hex)

BIT	NAME	FUNCTION
[7:0]	SMPLRT_DIV[7:0]	Divides the internal sample rate (see register CONFIG) to generate the sample rate that controls sensor data output rate, FIFO sample rate. **NOTE:** This register is only effective when FCHOICE_B register bits are 2'b00, and (0 < DLPF_CFG < 7). This is the update rate of the sensor register: SAMPLE_RATE = INTERNAL_SAMPLE_RATE / (1 + SMPLRT_DIV) Where INTERNAL_SAMPLE_RATE = 1 kHz

8.10 REGISTER 26 – CONFIGURATION

Register Name: CONFIG

Register Type: READ/WRITE

Register Address: 26 (Decimal); 1A (Hex)

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>[7]</td><td>-</td><td>Always set to 0</td></tr>
<tr><td>[6]</td><td>FIFO_MODE</td><td>When set to '1', when the FIFO is full, additional writes will not be written to FIFO.
When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.</td></tr>
<tr><td>[5:3]</td><td>EXT_SYNC_SET[2:0]</td><td>Enables the FSYNC pin data to be sampled.
<table>
<tr><th>EXT_SYNC_SET</th><th>FSYNC bit location</th></tr>
<tr><td>0</td><td>function disabled</td></tr>
<tr><td>1</td><td>TEMP_OUT_L[0]</td></tr>
<tr><td>2</td><td>GYRO_XOUT_L[0]</td></tr>
<tr><td>3</td><td>GYRO_YOUT_L[0]</td></tr>
<tr><td>4</td><td>GYRO_ZOUT_L[0]</td></tr>
<tr><td>5</td><td>ACCEL_XOUT_L[0]</td></tr>
<tr><td>6</td><td>ACCEL_YOUT_L[0]</td></tr>
<tr><td>7</td><td>ACCEL_ZOUT_L[0]</td></tr>
</table>
FSYNC will be latched to capture short strobes. This will be done such that if FSYNC toggles, the latched value toggles, but won't toggle again until the new latched value is captured by the sample rate strobe.</td></tr>
<tr><td>[2:0]</td><td>DLPF_CFG[2:0]</td><td>For the DLPF to be used, FCHOICE_B[1:0] is 2'b00.
See the table below.</td></tr>
</table>

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B* [1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below.

FCHOICE_B		DLPF_CFG	Gyroscope			Temperature Sensor
<1>	<0>		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)	3-dB BW (Hz)
X	1	X	8173	8595.1	32	4000
1	0	X	3281	3451.0	32	4000
0	0	0	250	306.6	8	4000
0	0	1	176	177.0	1	188
0	0	2	92	108.6	1	98
0	0	3	41	59.0	1	42
0	0	4	20	30.5	1	20
0	0	5	10	15.6	1	10
0	0	6	5	8.0	1	5
0	0	7	3281	3451.0	8	4000

8.11 REGISTER 27 – GYROSCOPE CONFIGURATION

Register Name: GYRO_CONFIG

Register Type: READ/WRITE

Register Address: 27 (Decimal); 1B (Hex)

BIT	NAME	FUNCTION
[7]	XG_ST	X Gyro self-test
[6]	YG_ST	Y Gyro self-test
[5]	ZG_ST	Z Gyro self-test
[4:3]	FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±500 dps 01= ±1000 dps 10 = ±2000 dps 11 = ±4000 dps
[2]	-	Reserved
[1:0]	FCHOICE_B[1:0]	Used to bypass DLPF as shown in table 1 above.

8.12 REGISTER 28 – ACCELEROMETER CONFIGURATION

Register Name: ACCEL_CONFIG

Register Type: READ/WRITE

Register Address: 28 (Decimal); 1C (Hex)

BIT	NAME	FUNCTION
[7]	XA_ST	X Accel self-test
[6]	YA_ST	Y Accel self-test
[5]	ZA_ST	Z Accel self-test
[4:3]	ACCEL_FS_SEL[1:0]	Accel Full Scale Select: ±4g (00), ±8g (01), ±16g (10), ±32g (11)
[2:0]	-	Reserved

8.13 REGISTER 29 – ACCELEROMETER CONFIGURATION 2

Register Name: ACCEL_CONFIG2

Register Type: READ/WRITE

Register Address: 29 (Decimal); 1D (Hex)

BIT	NAME	FUNCTION
[7:6]	-	Reserved
[5:4]	DEC2_CFG[1:0]	Averaging filter settings for Low Power Accelerometer mode: 0 = Average 4 samples 1 = Average 8 samples 2 = Average 16 samples 3 = Average 32 samples
[3]	ACCEL_FCHOICE_B	Used to bypass DLPF as shown in the table below.
[2:0]	A_DLPF_CFG	Accelerometer low pass filter setting as shown in table 2 below.

Accelerometer Data Rates and Bandwidths (Low-Noise Mode)

ACCEL_FCHOICE_B	A_DLPF_CFG	Accelerometer		
		3-dB BW (Hz)	Noise BW (Hz)	Rate (kHz)
1	X	1046.0	1100.0	4
0	0	218.1	235.0	1
0	1	218.1	235.0	1
0	2	99.0	121.3	1
0	3	44.8	61.5	1
0	4	21.2	31.0	1
0	5	10.2	15.5	1
0	6	5.1	7.8	1
0	7	420.0	441.6	1

The data output rate of the DLPF filter block can be further reduced by a factor of 1/(1+SMPLRT_DIV), where SMPLRT_DIV is an 8-bit integer. Following is a small subset of ODRs that are configurable for the accelerometer in the low-noise mode in this manner (Hz):

3.91, 7.81, 15.63, 31.25, 62.50, 125, 250, 500, 1K

8.14 REGISTER 30 – LOW POWER MODE CONFIGURATION

Register Name: LP_MODE_CFG

Register Type: READ/WRITE

Register Address: 30 (Decimal); 1E (Hex)

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>[7]</td><td>GYRO_CYCLE</td><td>When set to ‘1’ low-power gyroscope mode is enabled. Default setting is ‘0’</td></tr>
<tr><td>[6:4]</td><td>G_AVGCFG[2:0]</td><td>Averaging filter configuration for low-power gyroscope mode. Default setting is ‘000’</td></tr>
<tr><td>[3:0]</td><td>LPOSC_CLKSEL</td><td>Sets the frequency of waking up the chip to take a sample of accel data – the low power accel Output Data Rate
<table>
<tr><th>LPOSC_CLKSEL</th><th>Output Frequency (Hz)</th></tr>
<tr><td>0</td><td>0.24</td></tr>
<tr><td>1</td><td>0.49</td></tr>
<tr><td>2</td><td>0.98</td></tr>
<tr><td>3</td><td>1.95</td></tr>
<tr><td>4</td><td>3.91</td></tr>
<tr><td>5</td><td>7.81</td></tr>
<tr><td>6</td><td>15.63</td></tr>
<tr><td>7</td><td>31.25</td></tr>
<tr><td>8</td><td>62.50</td></tr>
<tr><td>9</td><td>125</td></tr>
<tr><td>10</td><td>250</td></tr>
<tr><td>11</td><td>500</td></tr>
<tr><td>12-15</td><td>Reserved</td></tr>
</table></td></tr>
</table>

To operate in gyroscope low-power mode or 6-axis low-power mode, GYRO_CYCLE should be set to ‘1.’ Gyroscope filter configuration is determined by G_AVGCFG[2:0] that sets the averaging filter configuration. It is not dependent on DLPF_CFG[2:0].

The following table shows some example configurations for gyroscope low power mode.

<table>
<tr><td>FCHOICE_B</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>G_AVGCFG</td><td></td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td></tr>
<tr><td>Averages</td><td></td><td>1x</td><td>2x</td><td>4x</td><td>8x</td><td>16x</td><td>32x</td><td>64x</td><td>128x</td></tr>
<tr><td>Ton (ms)</td><td></td><td>1.73</td><td>2.23</td><td>3.23</td><td>5.23</td><td>9.23</td><td>17.23</td><td>33.23</td><td>65.23</td></tr>
<tr><td>Noise BW (Hz)</td><td></td><td>650.8</td><td>407.1</td><td>224.2</td><td>117.4</td><td>60.2</td><td>30.6</td><td>15.6</td><td>8.0</td></tr>
<tr><td>3-dB BW (Hz)</td><td></td><td>622</td><td>391</td><td>211</td><td>108</td><td>54</td><td>27</td><td>14</td><td>7</td></tr>
<tr><td>SMPLRT_DIV</td><td>ODR (Hz)</td><td colspan="8"></td></tr>
<tr><td>255</td><td>3.9</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>99</td><td>10.0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>65</td><td>15.2</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>64</td><td>15.4</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td rowspan="3">N/A</td></tr>
<tr><td>39</td><td>25.0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>33</td><td>29.4</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>32</td><td>30.3</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td colspan="2" rowspan="3">N/A</td></tr>
<tr><td>19</td><td>50.0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>17</td><td>55.6</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>16</td><td>58.8</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td colspan="3" rowspan="2">N/A</td></tr>
<tr><td>9</td><td>100.0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>8</td><td>111.1</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td><td colspan="4" rowspan="2">N/A</td></tr>
<tr><td>7</td><td>125.0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>4</td><td>200.0</td><td>Valid</td><td>Valid</td><td>Valid</td><td colspan="5" rowspan="2">N/A</td></tr>
<tr><td>3</td><td>250.0</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>2</td><td>333.3</td><td>Valid</td><td>Valid</td><td colspan="6">N/A</td></tr>
<tr><td>1</td><td>500.0</td><td>Valid</td><td colspan="7">N/A</td></tr>
</table>

8.15 REGISTER 31 – WAKE-ON MOTION THRESHOLD (ACCELEROMETER)

Register Name: ACCEL_WOM_THR

Register Type: READ/WRITE

Register Address: 31 (Decimal); 1F (Hex)

BIT	NAME	FUNCTION
[7:0]	WOM_THR[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for accelerometer.

8.16 REGISTER 35 – FIFO ENABLE

Register Name: FIFO_EN

Register Type: READ/WRITE

Register Address: 35 (Decimal); 23 (Hex)

BIT	NAME	FUNCTION
[7]	TEMP_FIFO_EN	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[6]	XG_FIFO_EN	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[5]	YG_FIFO_EN	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled **NOTE:** Enabling any one of the bits corresponding to the Gyros or Temp data paths, data is buffered into the FIFO even though that data path is not enabled.
[4]	ZG_FIFO_EN	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate; If enabled, buffering of data occurs even if data path is in standby. 0 – function is disabled
[3]	ACCEL_FIFO_EN	1 – write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate; 0 – function is disabled
[2:0]	-	Reserved

8.17 REGISTER 54 – FSYNC INTERRUPT STATUS

Register Name: FSYNC_INT

Register Type: READ to CLEAR

Register Address: 54 (Decimal); 36 (Hex)

BIT	NAME	FUNCTION
[7]	FSYNC_INT	This bit automatically sets to 1 when a FSYNC interrupt has been generated. The bit clears to 0 after the register has been read.

8.18 REGISTER 55 – INT/DRDY PIN / BYPASS ENABLE CONFIGURATION

Register Name: INT_PIN_CFG

Register Type: READ/WRITE

Register Address: 55 (Decimal); 37 (Hex)

BIT	NAME	FUNCTION
[7]	INT_LEVEL	1 – The logic level for INT/DRDY pin is active low. 0 – The logic level for INT/DRDY pin is active high.
[6]	INT_OPEN	1 – INT/DRDY pin is configured as open drain. 0 – INT/DRDY pin is configured as push-pull.
[5]	LATCH_INT_EN	1 – INT/DRDY pin level held until interrupt status is cleared. 0 – INT/DRDY pin indicates interrupt pulse's width is 50us.
[4]	INT_RD_CLEAR	1 – Interrupt status is cleared if any read operation is performed. 0 – Interrupt status is cleared only by reading INT_STATUS register
[3]	FSYNC_INT_LEVEL	1 – The logic level for the FSYNC pin as an interrupt is active low. 0 – The logic level for the FSYNC pin as an interrupt is active high.
[2]	FSYNC_INT_MODE_EN	When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by F*SYNC_INT_LEVEL*. When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.
[1]	-	Reserved
[0]	-	Always set to 0

8.19 REGISTER 56 – INTERRUPT ENABLE

Register Name: INT_ENABLE

Register Type: READ/WRITE

Register Address: 56 (Decimal); 38 (Hex)

BIT	NAME	FUNCTION
[7:5]	WOM_INT_EN[7:5]	111 – Enable WoM interrupt on accelerometer. 000 – Disable WoM interrupt on accelerometer.
[4]	FIFO_OFLOW_EN	1 – Enables a FIFO buffer overflow to generate an interrupt. 0 – Function is disabled.
[3]	-	Reserved
[2]	GDRIVE_INT_EN	Gyroscope Drive System Ready interrupt enable
[1]	-	Reserved
[0]	DATA_RDY_INT_EN	Data ready interrupt enable

8.20 REGISTER 58 – INTERRUPT STATUS

Register Name: INT_STATUS

Register Type: READ to CLEAR

Register Address: 58 (Decimal); 3A (Hex)

BIT	NAME	FUNCTION
[7:5]	WOM_INT	Accelerometer WoM interrupt status. Cleared on Read. 111 – WoM interrupt on accelerometer
[4]	FIFO_OFLOW_INT	This bit automatically sets to 1 when a FIFO buffer overflow has been generated. The bit clears to 0 after the register has been read.
[3]	-	Reserved.
[2]	GDRIVE_INT	Gyroscope Drive System Ready interrupt
[1]	-	Reserved.
[0]	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.

8.21 REGISTERS 59 TO 64 – ACCELEROMETER MEASUREMENTS

Register Name: ACCEL_XOUT_H

Register Type: READ only

Register Address: 59 (Decimal); 3B (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_H[15:8]	High byte of accelerometer x-axis data.

Register Name: ACCEL_XOUT_L

Register Type: READ only

Register Address: 60 (Decimal); 3C (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_XOUT_L[7:0]	Low byte of accelerometer x-axis data.

Register Name: ACCEL_YOUT_H

Register Type: READ only

Register Address: 61 (Decimal); 3D (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_H[15:8]	High byte of accelerometer y-axis data.

Register Name: ACCEL_YOUT_L

Register Type: READ only

Register Address: 62 (Decimal); 3E (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_YOUT_L[7:0]	Low byte of accelerometer y-axis data.

Register Name: ACCEL_ZOUT_H

Register Type: READ only

Register Address: 63 (Decimal); 3F (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_H[15:8]	High byte of accelerometer z-axis data.

Register Name: ACCEL_ZOUT_L

Register Type: READ only

Register Address: 64 (Decimal); 40 (Hex)

BIT	NAME	FUNCTION
[7:0]	ACCEL_ZOUT_L[7:0]	Low byte of accelerometer z-axis data.

8.22 REGISTERS 65 AND 66 – TEMPERATURE MEASUREMENT

Register Name: TEMP_OUT_H

Register Type: READ only

Register Address: 65 (Decimal); 41 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[15:8]	High byte of the temperature sensor output

Register Name: TEMP_OUT_L

Register Type: READ only

Register Address: 66 (Decimal); 42 (Hex)

BIT	NAME	FUNCTION
[7:0]	TEMP_OUT[7:0]	Low byte of the temperature sensor output **TEMP_degC** = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 25degC

8.23 REGISTERS 67 TO 72 – GYROSCOPE MEASUREMENTS

Register Name: GYRO_XOUT_H

Register Type: READ only

Register Address: 67 (Decimal); 43 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[15:8]	High byte of the X-Axis gyroscope output

Register Name: GYRO_XOUT_L

Register Type: READ only

Register Address: 68 (Decimal); 44 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_XOUT[7:0]	Low byte of the X-Axis gyroscope output **GYRO_XOUT =** Gyro_Sensitivity * X_angular_rate Nominal Conditions: FS_SEL = 0 Gyro_Sensitivity = 65.5 LSB/(dps)

Register Name: GYRO_YOUT_H

Register Type: READ only

Register Address: 69 (Decimal); 45 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[15:8]	High byte of the Y-Axis gyroscope output

Register Name: GYRO_YOUT_L

Register Type: READ only

Register Address: 70 (Decimal); 46 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_YOUT[7:0]	Low byte of the Y-Axis gyroscope output **GYRO_YOUT =** Gyro_Sensitivity * Y_angular_rate Nominal Conditions: FS_SEL = 0 Gyro_Sensitivity = 65.5 LSB/(dps)

Register Name: GYRO_ZOUT_H

Register Type: READ only

Register Address: 71 (Decimal); 47 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[15:8]	High byte of the Z-Axis gyroscope output

Register Name: GYRO_ZOUT_L

Register Type: READ only

Register Address: 72 (Decimal); 48 (Hex)

BIT	NAME	FUNCTION
[7:0]	GYRO_ZOUT[7:0]	Low byte of the Z-Axis gyroscope output **GYRO_ZOUT =** Gyro_Sensitivity * Z_angular_rate Nominal Conditions: FS_SEL = 0 Gyro_Sensitivity = 65.5 LSB/(dps)

8.24 REGISTER 104 – SIGNAL PATH RESET

Register Name: SIGNAL_PATH_RESET

Register Type: READ/WRITE

Register Address: 104 (Decimal); 68 (Hex)

BIT	NAME	FUNCTION
[7:2]	-	Reserved
[1]	ACCEL_RST	Reset accel digital signal path. **NOTE:** Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.
[0]	TEMP_RST	Reset temp digital signal path. **NOTE:** Sensor registers are not cleared. Use SIG_COND_RST to clear sensor registers.

8.25 REGISTER 105 – ACCELEROMETER INTELLIGENCE CONTROL

Register Name: ACCEL_INTEL_CTRL

Register Type: READ/WRITE

Register Address: 105 (Decimal); 69 (Hex)

BIT	NAME	FUNCTION
[7]	ACCEL_INTEL_EN	This bit enables the Wake-on-Motion detection logic
[6]	ACCEL_INTEL_MODE	0 – Do not use 1 – Compare the current sample with the previous sample
[5:0]	-	Reserved

8.26 REGISTER 106 – USER CONTROL

Register Name: USER_CTRL

Register Type: READ/WRITE

Register Address: 106 (Decimal); 6A (Hex)

BIT	NAME	FUNCTION
[7]	-	Reserved.
[6]	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register.
[5]	-	Reserved
[4]	I2C_IF_DIS	1 – Disable I^2C Slave module and put the serial interface in SPI mode only.
[3]	-	Reserved.
[2]	FIFO_RST	1 – Reset FIFO module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20 MHz clock.
[1]	-	Reserved
[0]	SIG_COND_RST	1 – Reset all gyro digital signal path, accel digital signal path, and temp digital signal path. This bit also clears all the sensor registers.

8.27 REGISTER 107 – POWER MANAGEMENT 1

Register Name: PWR_MGMT_1

Register Type: READ/WRITE

Register Address: 107 (Decimal); 6B (Hex)

BIT	NAME	FUNCTION
[7]	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. The bit automatically clears to 0 once the reset is done.
[6]	SLEEP	When set to 1, the chip is set to sleep mode. **NOTE:** The default value is 1, the chip comes up in Sleep mode
[5]	ACCEL_CYCLE	When set to 1, and SLEEP and STANDBY are not set to 1, the chip will cycle between sleep and taking a single accelerometer sample at a rate determined by SMPLRT_DIV **NOTE:** When all accelerometer axes are disabled via PWR_MGMT_2 register bits and cycle is enabled, the chip will wake up at the rate determined by the respective registers above, but will not take any samples.
[4]	GYRO_STANDBY	When set, the gyro drive and pll circuitry are enabled, but the sense paths are disabled. This is a low power mode that allows quick enabling of the gyros.
[3]	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
[2:0]	CLKSEL[2:0]	**Code** **Clock Source** 0 Internal 20 MHz oscillator 1 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 2 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 3 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 4 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 5 Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6 Internal 20 MHz oscillator 7 Stops the clock and keeps timing generator in reset

NOTE: The default value of CLKSEL[2:0] is 000. It is required that CLKSEL[2:0] be set to 001 to achieve full gyroscope performance.

8.28 REGISTER 108 – POWER MANAGEMENT 2

Register Name: PWR_MGMT_2

Register Type: READ/WRITE

Register Address: 108 (Decimal); 6C (Hex)

BIT	NAME	FUNCTION
[7]	FIFO_LP_EN	1 – Enable FIFO in low-power accelerometer mode. Default setting is 0.
[6]	-	Reserved.
[5]	STBY_XA	1 – X accelerometer is disabled 0 – X accelerometer is on
[4]	STBY_YA	1 – Y accelerometer is disabled 0 – Y accelerometer is on
[3]	STBY_ZA	1 – Z accelerometer is disabled 0 – Z accelerometer is on
[2]	STBY_XG	1 – X gyro is disabled 0 – X gyro is on
[1]	STBY_YG	1 – Y gyro is disabled 0 – Y gyro is on
[0]	STBY_ZG	1 – Z gyro is disabled 0 – Z gyro is on

8.29 REGISTER 114 AND 115 – FIFO COUNT REGISTERS

Register Name: FIFO_COUNTH

Register Type: READ Only

Register Address: 114 (Decimal); 72 (Hex)

BIT	NAME	FUNCTION
[7:5]	-	Reserved
[4:0]	FIFO_COUNT[12:8]	High Bits, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

Register Name: FIFO_COUNTL

Register Type: READ Only

Register Address: 115 (Decimal); 73 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_COUNT[7:0]	Low Bits, count indicates the number of written bytes in the FIFO. **NOTE:** Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

8.30 REGISTER 116 – FIFO READ WRITE

Register Name: FIFO_R_W

Register Type: READ/WRITE

Register Address: 116 (Decimal); 74 (Hex)

BIT	NAME	FUNCTION
[7:0]	FIFO_DATA[7:0]	Read/Write command provides Read or Write operation for the FIFO.

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 59 through 72 will be written in order at the Sample Rate.

The contents of the sensor data registers (Registers 59 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO unless register 26 CONFIG, bit[6] FIFO_MODE = 1.

If the FIFO buffer is empty, reading register FIFO_DATA will return a unique value of 0xFF until new data is available. Normal data is precluded from ever indicating 0xFF, so 0xFF gives a trustworthy indication of FIFO empty.

8.31 REGISTER 117 – WHO AM I

Register Name: WHO_AM_I

Register Type: READ only

Register Address: 117 (Decimal); 75 (Hex)

BIT	NAME	FUNCTION
[7:0]	WHOAMI	Register to indicate to user which device is being accessed.

This register is used to verify the identity of the device. The contents of *WHOAMI* is an 8-bit device ID. The default value of the register is 0xAC. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor. The I^2C address of the ICM-20601 is 0x68 or 0x69 depending upon the value driven on AD0 pin.

8.32 REGISTERS 119, 120, 122, 123, 125, 126 ACCELEROMETER OFFSET REGISTERS

Register Name: XA_OFFSET_H

Register Type: READ/WRITE

Register Address: 119 (Decimal); 77 (Hex)

BIT	NAME	FUNCTION
[7:0]	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation. ±32g Offset cancellation in all Full Scale modes, 15 bit 1.95-mg steps

Register Name: XA_OFFSET_L

Register Type: READ/WRITE

Register Address: 120 (Decimal); 78 (Hex)

BIT	NAME	FUNCTION
[7:1]	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation. ±32g Offset cancellation in all Full Scale modes, 15 bit 1.95-mg steps
[0]	-	Reserved

Register Name: YA_OFFSET_H

Register Type: READ/WRITE

Register Address: 122 (Decimal); 7A (Hex)

BIT	NAME	FUNCTION
[7:0]	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation. ±32g Offset cancellation in all Full Scale modes, 15 bit 1.95-mg steps

Register Name: YA_OFFSET_L

Register Type: READ/WRITE

Register Address: 123 (Decimal); 7B (Hex)

BIT	NAME	FUNCTION
[7:1]	YA_OFFS[6:0]	Lower bits of the Y accelerometer offset cancellation. ±32g Offset cancellation in all Full Scale modes, 15 bit 1.95-mg steps
[0]	-	Reserved

Register Name: ZA_OFFSET_H

Register Type: READ/WRITE

Register Address: 125 (Decimal); 7D (Hex)

BIT	NAME	FUNCTION
[7:0]	ZA_OFFS[14:7]	Upper bits of the Z accelerometer offset cancellation. ±32g Offset cancellation in all Full Scale modes, 15 bit 1.95-mg steps

Register Name: ZA_OFFSET_L

Register Type: READ/WRITE

Register Address: 126 (Decimal); 7E (Hex)

BIT	NAME	FUNCTION
[7:1]	ZA_OFFS[6:0]	Lower bits of the Z accelerometer offset cancellation. ±32g Offset cancellation in all Full Scale modes, 15 bit 1.95-mg steps
[0]	-	Reserved

9 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in LGA package.

9.1 ORIENTATION OF AXES

Figure 13 shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

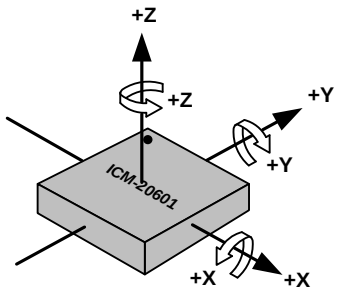
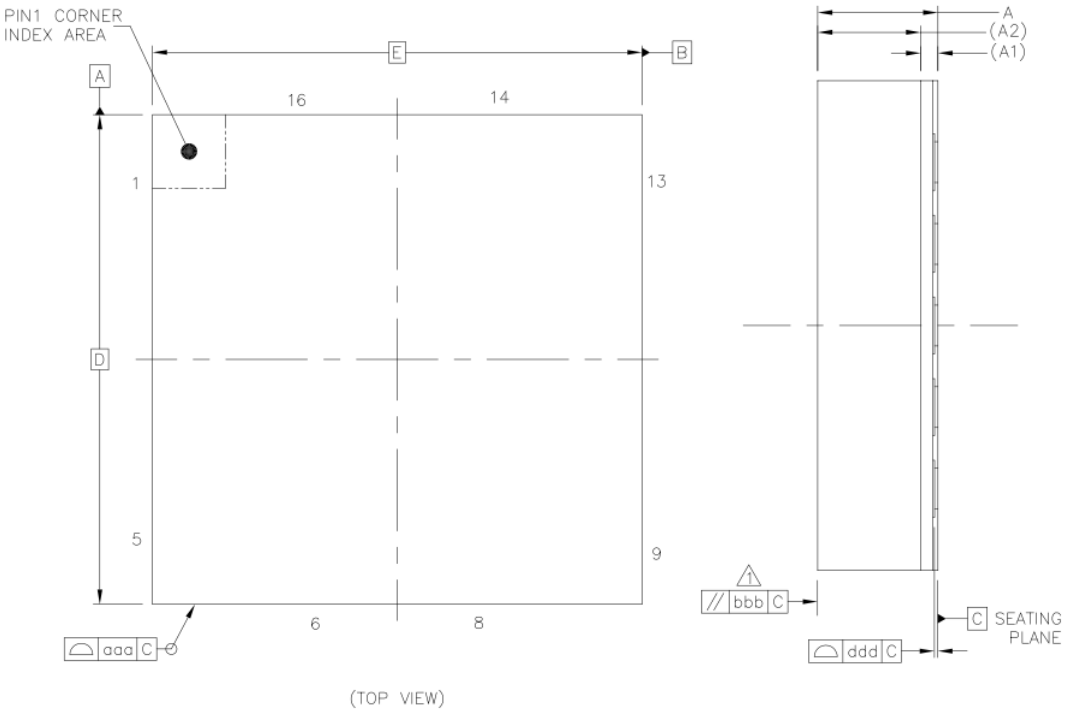


Figure 13. Orientation of Axes of Sensitivity and Polarity of Rotation

9.2 PACKAGE DIMENSIONS

16 Lead LGA (3x3x0.75) mm NiAu pad finish



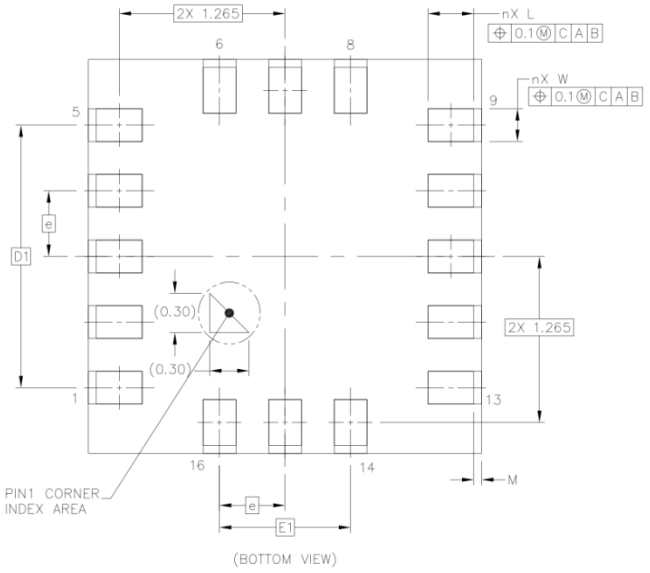


Figure 14. Package Dimensions

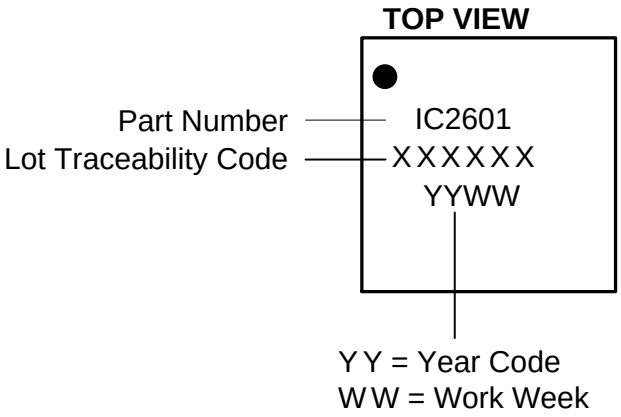
	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.7	0.75	0.8
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.63	REF
Body Size	D	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.3	0.35	0.4
Lead Pitch	e		0.5	BSC
Lead Count	n		16	
Edge Ball Center to Center	D1		2	BSC
	E1		1	BSC
Body Center to Contact Ball	SD		---	BSC
	SE		---	BSC
Ball Width	b	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	e1		---	
Ball Count	n1		---	
Pre-Solder		---	---	---
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		---	
Ball Offset (Ball)	fff		---	
Lead Edge to Package Edge	M	0.01	0.06	0.11

Table 16. Package Dimensions

10 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-20601 devices is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
ICM-20601	IC2601



11 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

12 REVISION HISTORY

REVISION DATE	REVISION NUMBER	DESCRIPTION
12/05/2016	1.0	Initial Release
02/18/2021	1.1	Added Note on page 19; Added Sections 4.18, 4.19
04/18/2021	1.2	Updated Table 6
10/01/2021	1.3	Updated self-test formulas (Sections 8.1 and 8.2); Added gyroscope offset cancellation step size (Sections 8.3 to 8.8); Update accelerometer offset cancellation step size (Section 8.32)

COMPLIANCE DECLARATION DISCLAIMER

InvenSense believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

TDK InvenSense