Data Sheet | August 2004 | FN3072.5

CMOS Voltage Converters

The Intersil ICL7660 and ICL7660A are monolithic CMOS power supply circuits which offer unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversions from positive to negative for an input range of +1.5V to +10.0V resulting in complementary output voltages of -1.5V to -10.0V and the ICL7660A does the same conversions with an input range of +1.5V to +12.0V resulting in complementary output voltages of -1.5V to -12.0V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 and ICL7660A can also be connected to function as voltage doublers and will generate output voltages up to +18.6V with a +10V input.

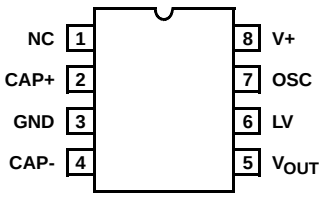
Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be overdriven by an external clock.

The “LV” terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V for the ICL7660 and +3.5V to +12.0V for the ICL7660A), the LV pin is left floating to prevent device latchup.

Pinouts

ICL7660, ICL7660A (PDIP, SOIC)
TOP VIEW



Features

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication (V_{OUT} = (-) nV_{IN})
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range
  - ICL7660 . . . . . 1.5V to 10.0V
  - ICL7660A . . . . . 1.5V to 12.0V
- ICL7660A 100% Tested at 3V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temp. and Voltage Range
- Pb-free available

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized μProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

Ordering Information

PART NO.	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ICL7660CBA*	0 to 70	8 Ld SOIC (N)	M8.15
ICL7660CBAZ* (See Note)	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660CBAZA* (See Note)	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660CPA	0 to 70	8 Ld PDIP	E8.3
ICL7660ACBA*	0 to 70	8 Ld SOIC (N)	M8.15
ICL7660ACBAZA* (See Note)	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660ACPA	0 to 70	8 Ld PDIP	E8.3
ICL7660AIBA*	-40 to 85	8 Ld SOIC (N)	M8.15
ICL7660AIBAZA* (See Note)	-40 to 85	8 Ld SOIC (N) (Pb-free)	M8.15

*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Absolute Maximum Ratings

Supply Voltage
- ICL7660 . . . . . +10.5V
- ICL7660A . . . . . +13.0V

LV and OSC Input Voltage . . . . . -0.3V to (V+ +0.3V) for V+ < 5.5V
(Note 2) . . . . . (V+ -5.5V) to (V+ +0.3V) for V+ > 5.5V
Current into LV (Note 2) . . . . . .20µA for V+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) . . . . . .Continuous

Operating Conditions

Temperature Range
- ICL7660C, ICL7660AC. . . . . 0^oC to 70^oC
- ICL7660AI . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	110	N/A
SOIC Package	160	N/A

Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering, 10s). . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

ICL7660 and ICL7660A, V+ = 5V, $T_A = 25^oC$, $C_{OSC} = 0$, Test Circuit Figure 11 Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7660			ICL7660A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	$R_L = \infty$	-	170	500	-	80	165	µA
Supply Voltage Range - Lo	V_L+	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GND	1.5	-	3.5	1.5	-	3.5	V
Supply Voltage Range - Hi	V_H+	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to Open	3.0	-	10.0	3	-	12	V
Output Source Resistance	R_{OUT}	I_{OUT} = 20mA, $T_A = 25^oC$	-	55	100	-	60	100	Ω
		I_{OUT} = 20mA, $0^oC \leq T_A \leq 70^oC$	-	-	120	-	-	120	Ω
		I_{OUT} = 20mA, $-55^oC \leq T_A \leq 125^oC$	-	-	150	-	-	-	Ω
		I_{OUT} = 20mA, $-40^oC \leq T_A \leq 85^oC$	-	-	-	-	-	120	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV to GND $0^oC \leq T_A \leq 70^oC$	-	-	300	-	-	300	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GND, $-55^oC \leq T_A \leq 125^oC$	-	-	400	-	-	-	Ω
Oscillator Frequency	f_{OSC}		-	10	-	-	10	-	kHz
Power Efficiency	P_{EF}	R_L = 5kΩ	95	98	-	96	98	-	%
Voltage Conversion Efficiency	$V_{OUT\ EF}$	$R_L = \infty$	97	99.9	-	99	99.9	-	%
Oscillator Impedance	Z_{OSC}	V+ = 2V	-	1.0	-	-	1	-	MΩ
		V = 5V	-	100	-	-	-	-	kΩ
ICL7660A, V+ = 3V, $T_A = 25^oC$, OSC = Free running, Test Circuit Figure 11, Unless Otherwise Specified									
Supply Current (Note 3)	I+	V+ = 3V, $R_L = \infty$, 25^oC	-	-	-	-	26	100	µA
		$0^oC < T_A < 70^oC$	-	-	-	-	-	125	µA
		$-40^oC < T_A < 85^oC$	-	-	-	-	-	125	µA
Output Source Resistance	R_{OUT}	V+ = 3V, I_{OUT} = 10mA	-	-	-	-	97	150	Ω
		$0^oC < T_A < 70^oC$	-	-	-	-	-	200	Ω
		$-40^oC < T_A < 85^oC$	-	-	-	-	-	200	Ω
Oscillator Frequency (Note 3)	f_{OSC}	V+ = 3V (same as 5V conditions)	-	-	-	5.0	8	-	kHz
		$0^oC < T_A < 70^oC$	-	-	-	3.0	-	-	kHz
		$-40^oC < T_A < 85^oC$	-	-	-	3.0	-	-	kHz

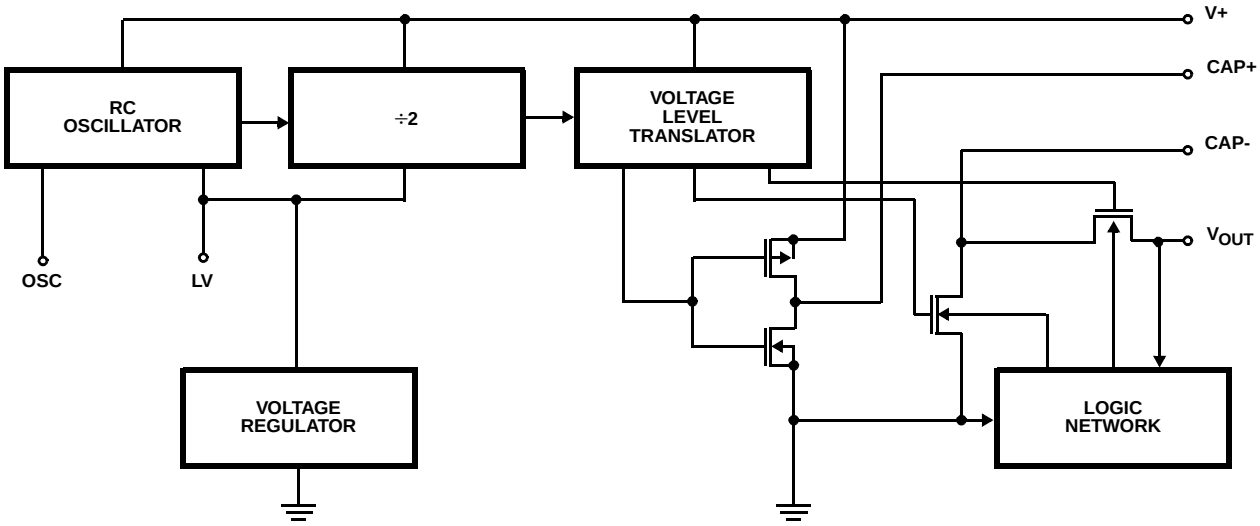
Electrical Specifications ICL7660 and ICL7660A, V+ = 5V, $T_A = 25^oC$, $C_{OSC} = 0$, Test Circuit Figure 11 Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7660			ICL7660A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Conversion Efficiency	$V_{OUT}EFF$	V+ = 3V, $R_L = \infty$	-	-	-	99	-	-	%
		$T_{MIN} < T_A < T_{MAX}$	-	-	-	99	-	-	%
Power Efficiency	P_{EFF}	V+ = 3V, $R_L = 5k\Omega$	-	-	-	96	-	-	%
		$T_{MIN} < T_A < T_{MAX}$	-	-	-	95	-	-	%

NOTES:

2. Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the ICL7660, ICL7660A.
3. Derate linearly above 50^oC by 5.5mW/^oC.
4. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
5. The Intersil ICL7660A can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

Functional Block Diagram



Typical Performance Curves (Test Circuit of Figure 11)

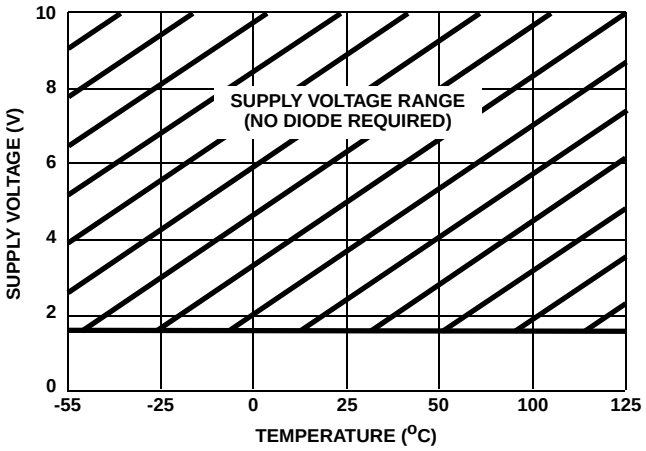


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

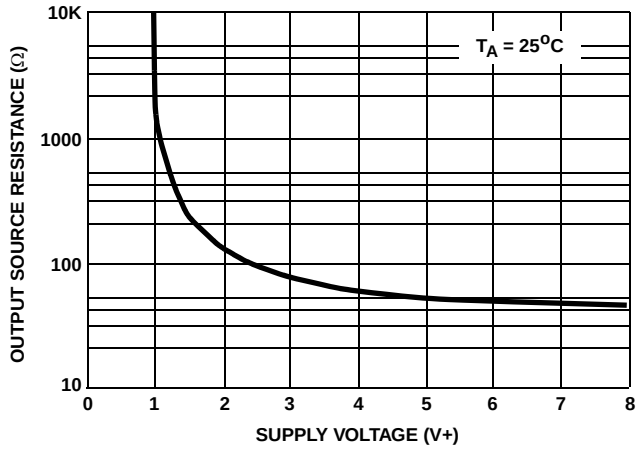


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves (Test Circuit of Figure 11) **(Continued)**

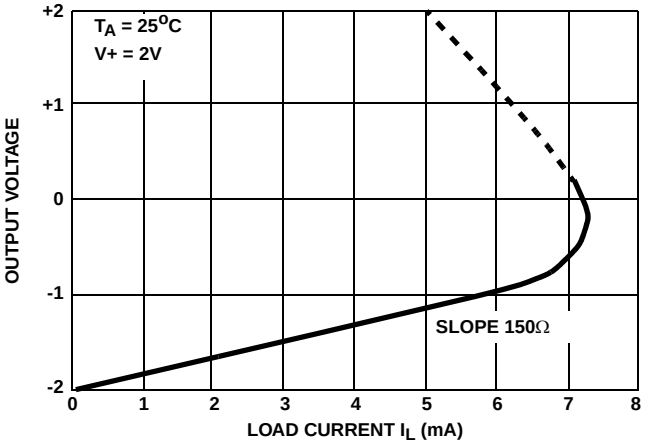


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

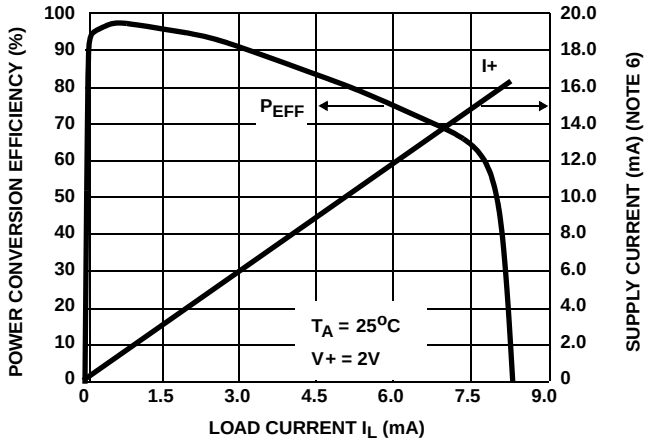
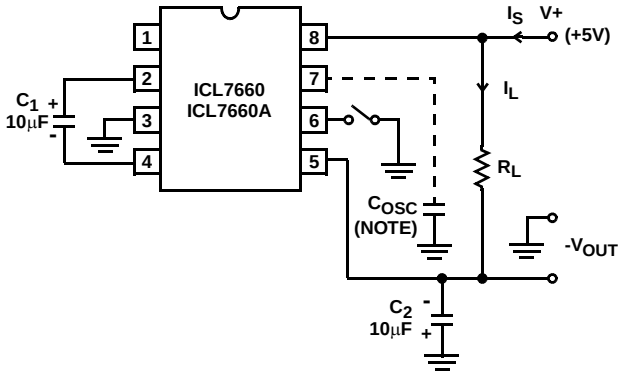


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

NOTE:

6. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 11). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660/ICL7660A, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.



NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C2 should be increased to 100µF.

FIGURE 11. ICL7660, ICL7660A TEST CIRCUIT

Detailed Description

The ICL7660 and ICL7660A contain all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 12, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660 and ICL7660A, the 4 switches of Figure 12 are MOS power switches; S_1 is a P-Channel device and S_2, S_3 and S_4 are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their “ON” resistances. In addition, at circuit start-up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 and ICL7660A by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 and ICL7660A is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the “LV” pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

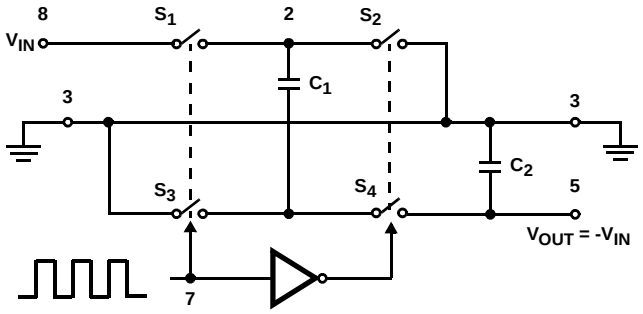


FIGURE 12. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met.

1. The driver circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 and ICL7660A approach these conditions for negative voltage conversion if large values of C_1 and C_2 are used.

ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS. The energy lost is defined by:

$$E = {}^1/_2\, C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 12) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do’s And Don’ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and ICL7660A and the + terminal of C_2 must be connected to GROUND.
5. If the voltage supply driving the ICL7660 and ICL7660A has a large source impedance (25Ω - 30Ω), then a 2.2μF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/μs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

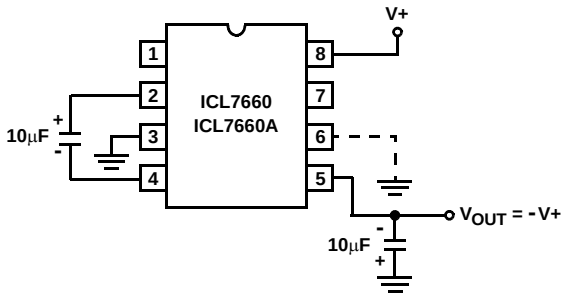


FIGURE 13A. CONFIGURATION

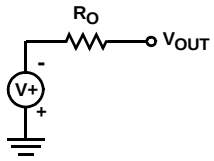


FIGURE 13B. THEVENIN EQUIVALENT

FIGURE 13. SIMPLE NEGATIVE CONVERTER